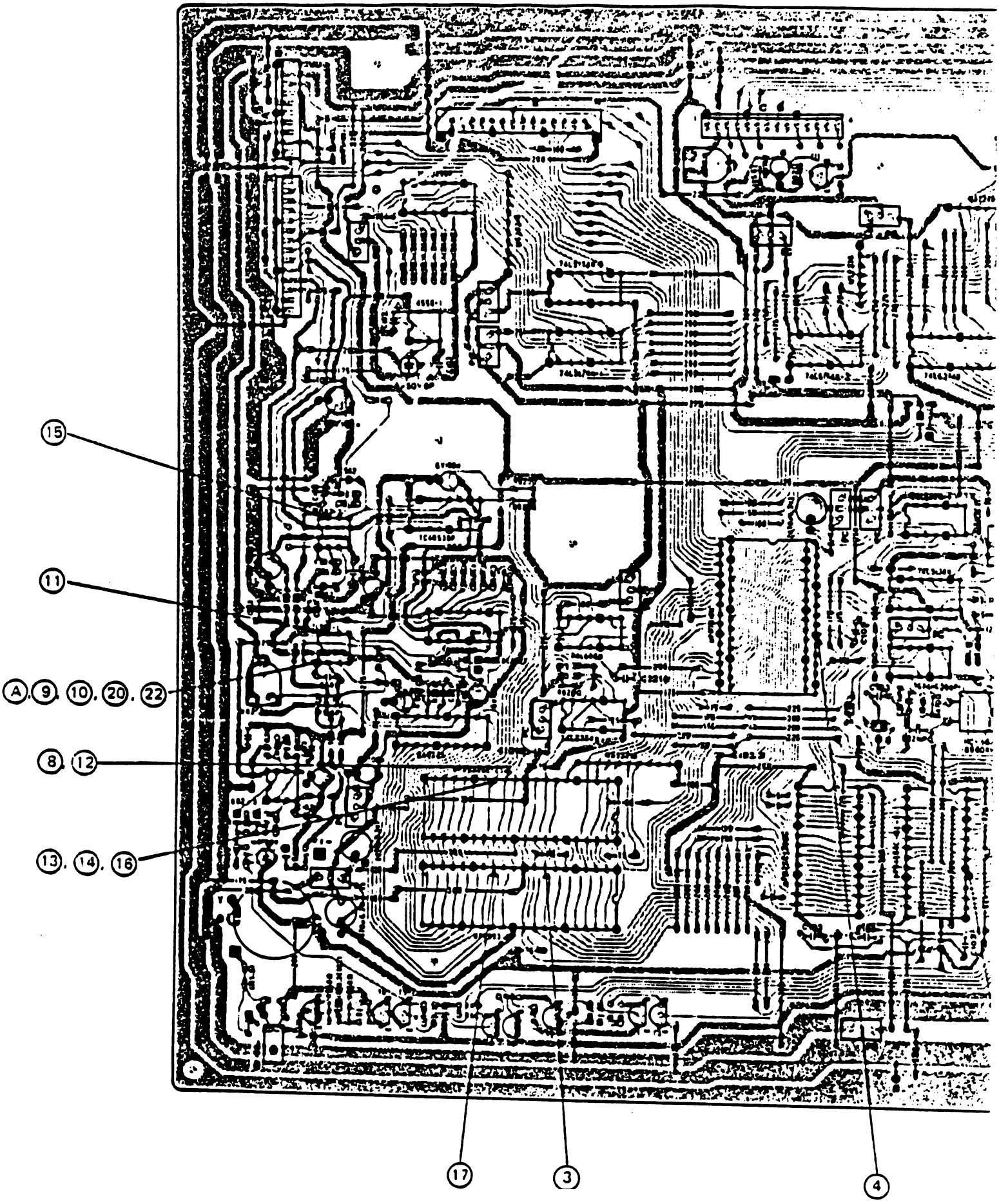
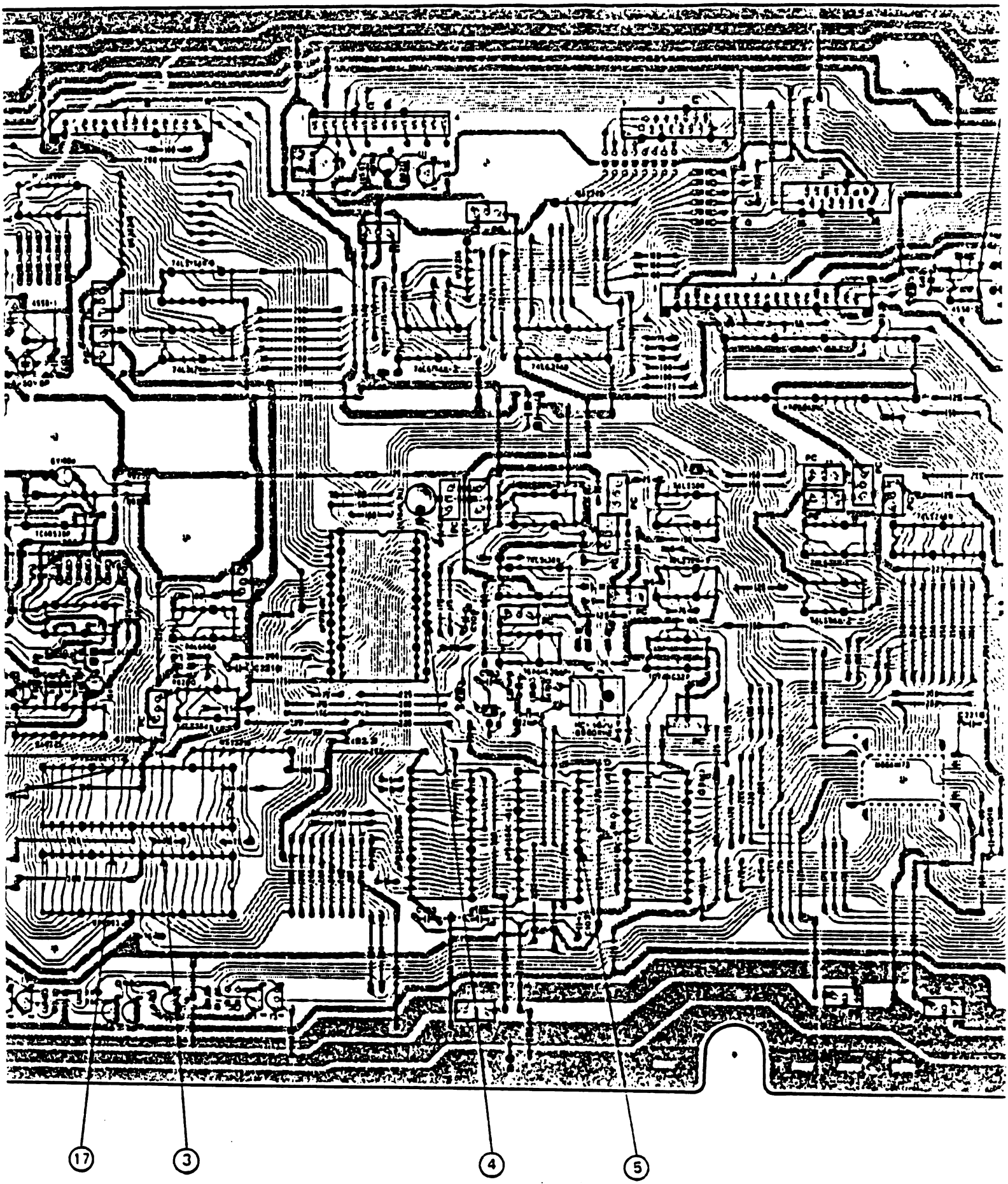
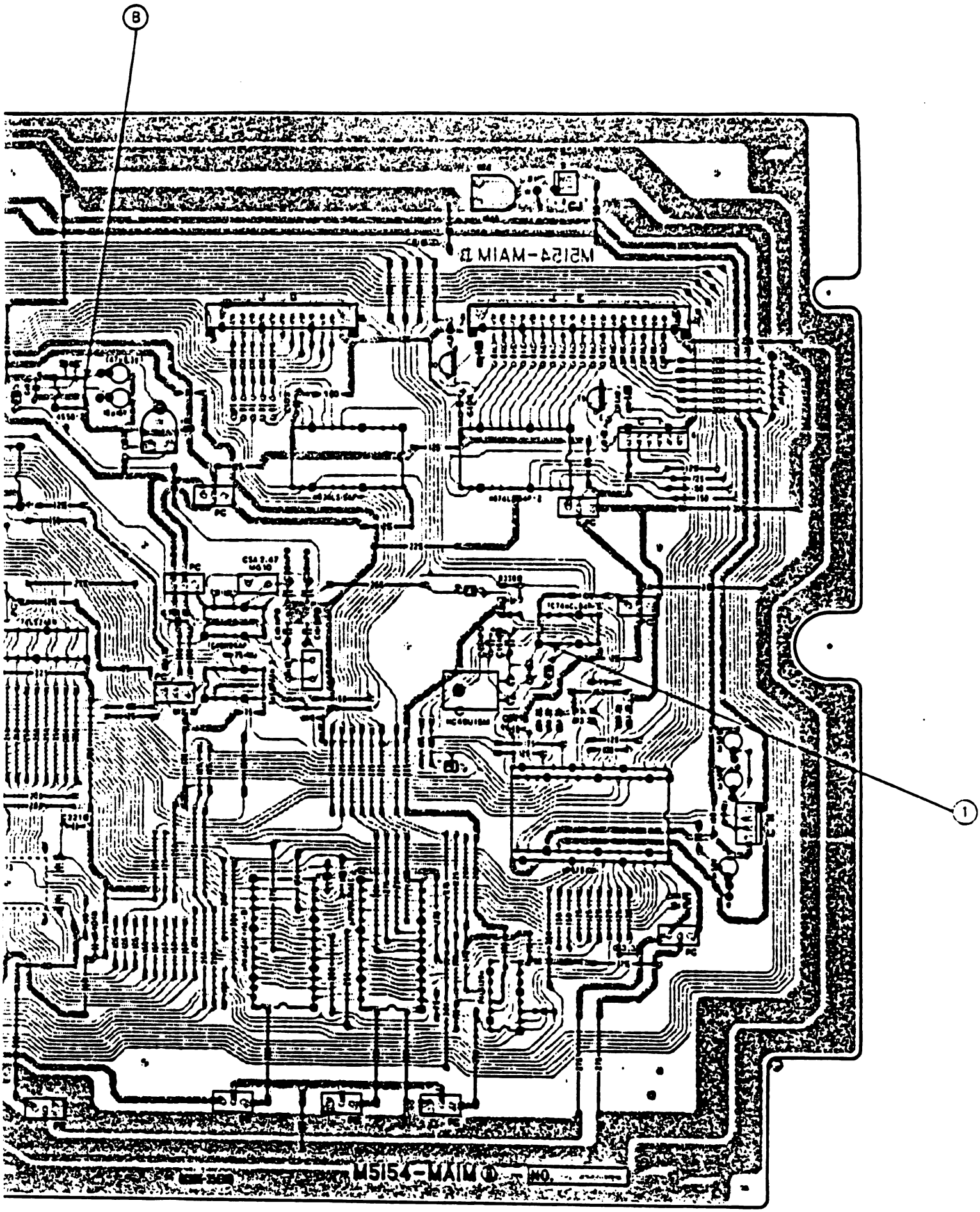
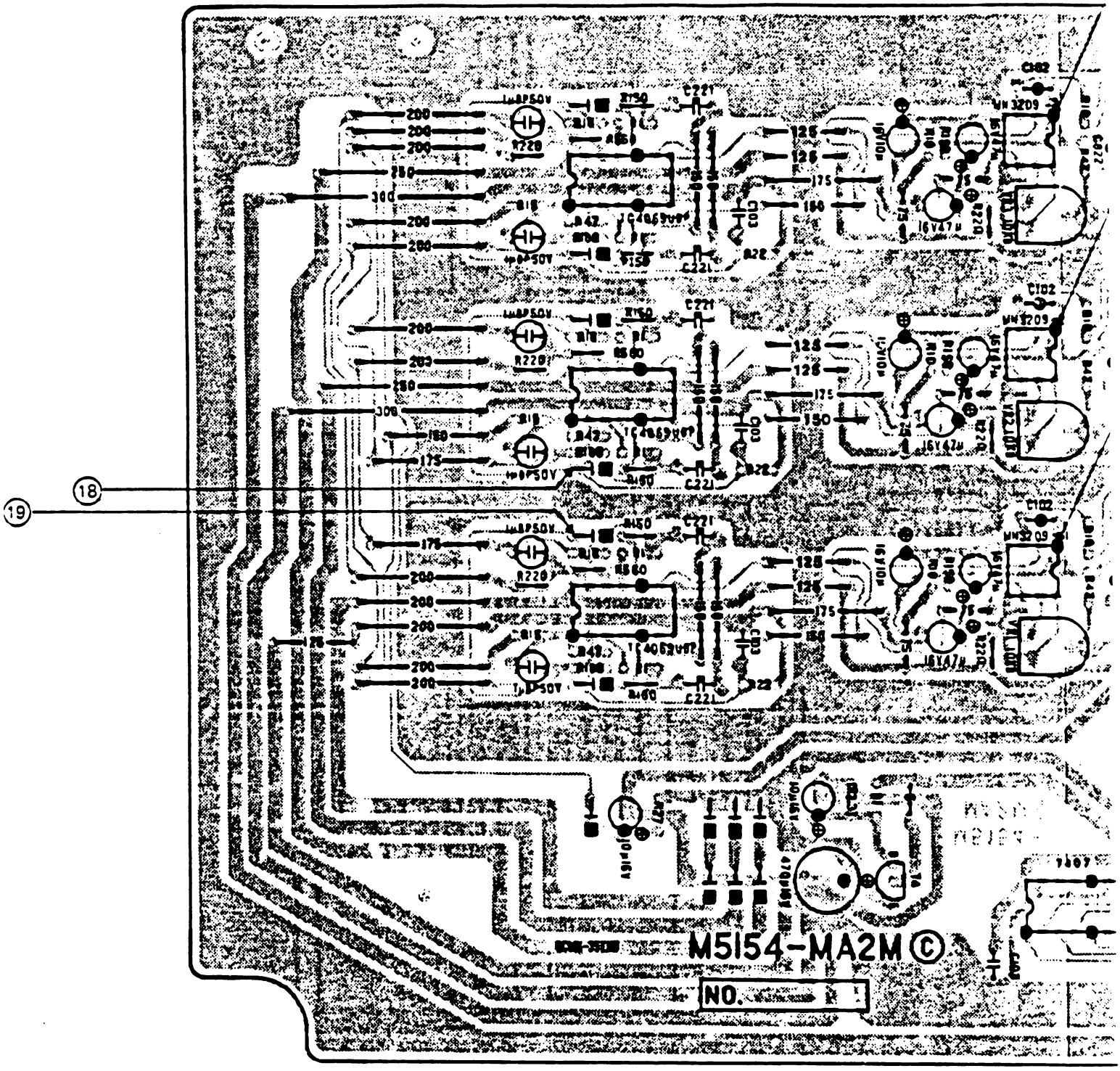
3. PCB VIEW & MAJOR CHECKPOINTS

3-1. PCB M5154-MA1M

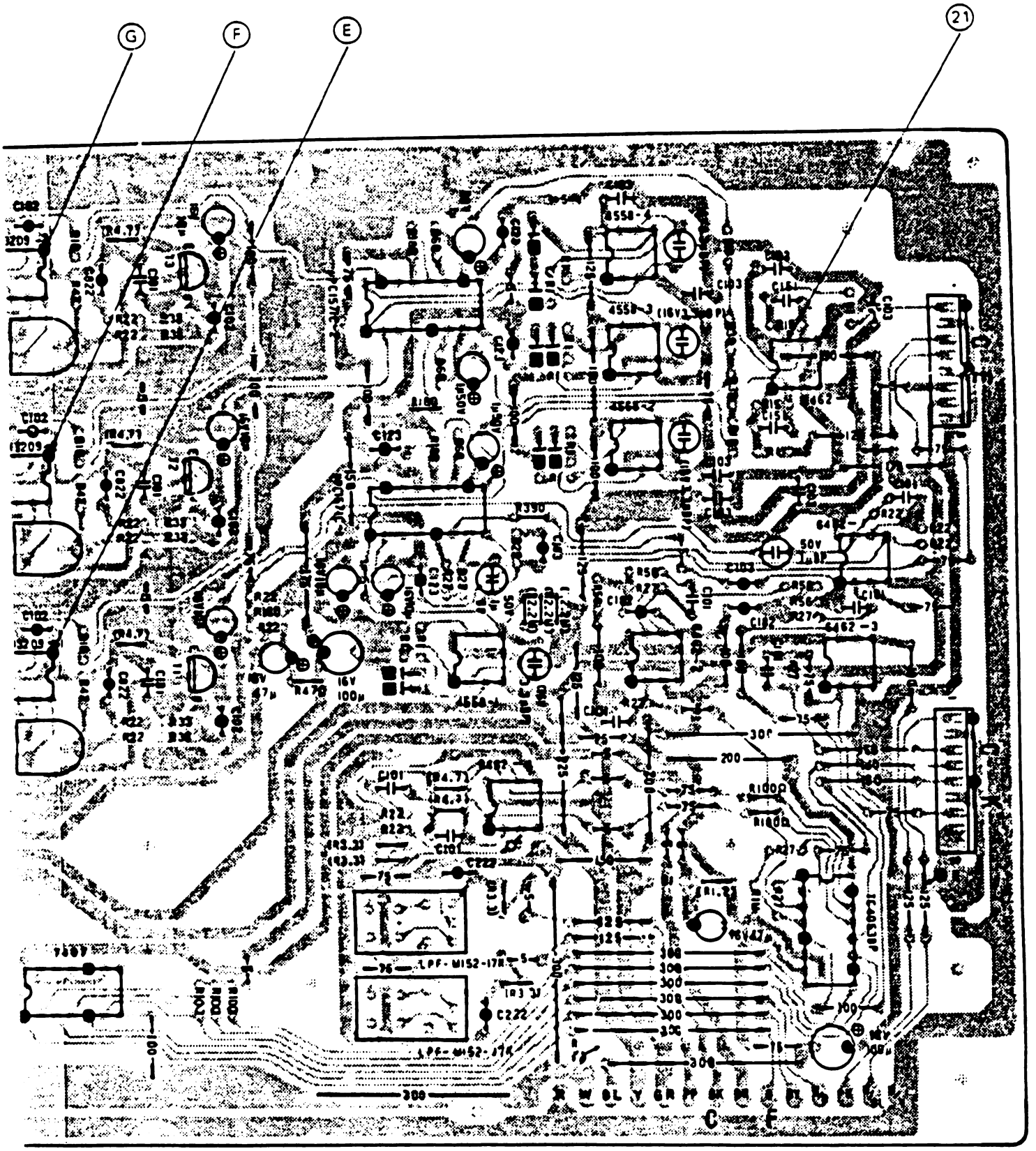



17
3
4
5


B
1
M5154-MAIM B
M5154-MAIM A

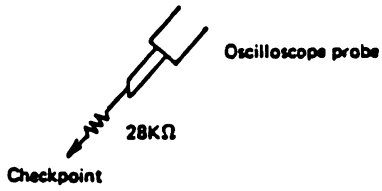

18
19
M5154-MA2M ©
NO.

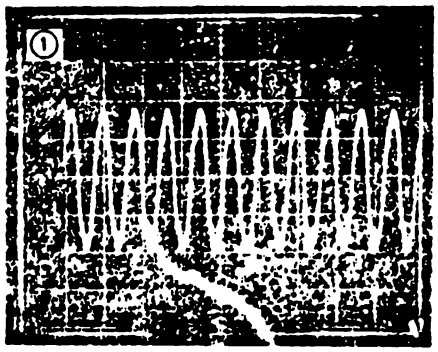
3-2. PCB M5154-MA2M



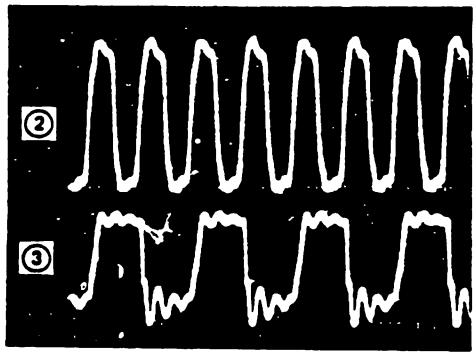
4. MAJOR WAVEFORMS

Notes: Photographs marked Ⓜ show stored waveforms in a memory scope.
The analog waveforms were observed via a 28 Kohm resistor.
Probe reduction; 10:1



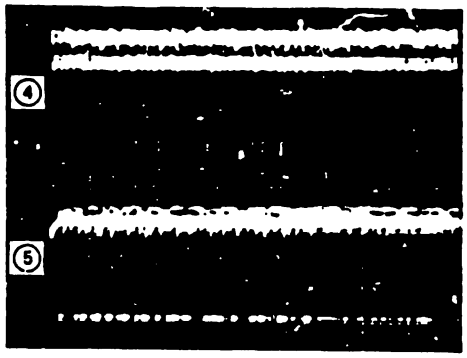


① μPD7810H clock pulse
PCB M5154-MA1M
TC74HC04P-2 pin 2
0.1μS/div, 0.2V/div



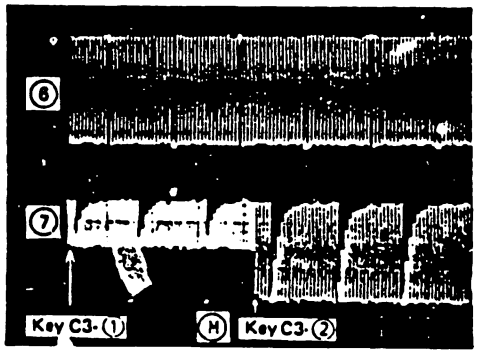
② μPD8049HC clock pulse
PCB M5154-MA1M
TC74HC04P-1 pin 11
0.1μS/div, 0.2V/div

③ μPD933AC clock pulse
PCB M5154-MA1M
μPD933AC pin 8
0.1μS/div, 0.2V/div



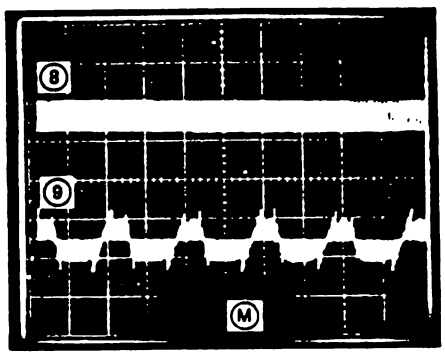
④ μPD7810H $\overline{WR}$ signal
PCB M5154-MA1M
μPD7810H (SUB) pin 45
5μS/div, 0.2V/div

⑤ μPD4464C $\overline{CE}$ signal
PCB M5154-MA1M
μPD4464C-15L-1 pin 20
5μS/div, 0.2V/div



⑥ Key common signal
PCB M5177-KY2M
Refer to page 9
0.2mS/div, 0.2V/div

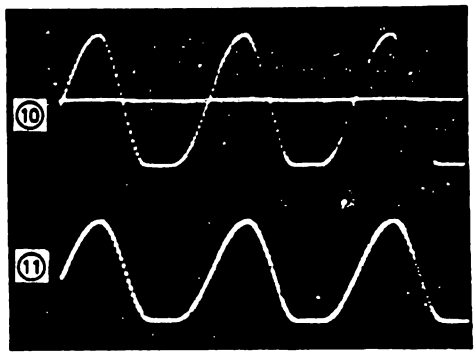
⑦ Key input signal
PCB M5177-KY2M
Refer to page 9
0.2mS/div, 0.2V/div



⑧ μPD933AC DOE signal
PCB M5154-MA1M
μPD933AC pin 12
2mS/div, 0.5V/div

⑨ DAC output
PCB M5154-MA1M
TL082-1 pin 1
10μS/div, 0.5V/div

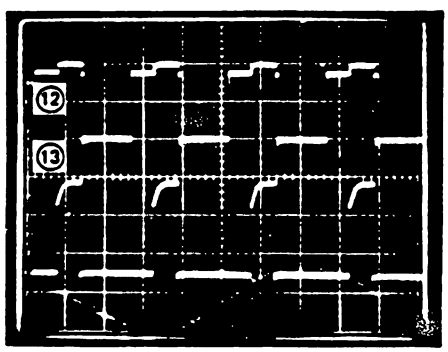
Tone: Flute, Key: C4



⑩ DAC output
PCB M5154-MA1M
TL082-1 pin 1
5mS/div, 0.2V/div

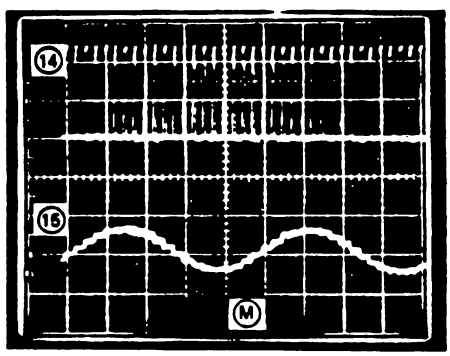
⑪ Expander circuit output
PCB M5154-MA1M
TL082-1 pin 7
5mS/div, 50mV/div

Tone: Flute, Key: C4



⑫ μPD933AC(M) DOE signal
PCB M5154-MA1M
μPD933AC(M) pin 12
10μS/div, 0.2V/div

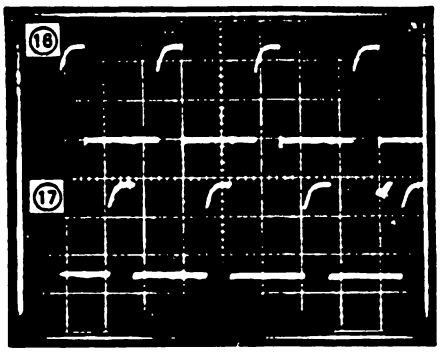
⑬ μPD933AC(M) SH signal
PCB M5154-MA1M
μPD933AC(M) pin 13
10μS/div, 0.2V/div



⑭ μPD933AC(M) SH signal
PCB M5154-MA1M
μPD933AC(M) pin 13
0.1μS/div, 0.2V/div

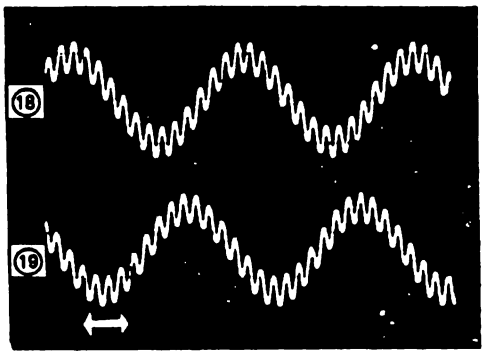
⑮ Sample/Hold circuit output
PCB M5154-MA1M
TL082-2 pin 7
0.1μS/div, 2V/div

Tone: Flute, Key: C7



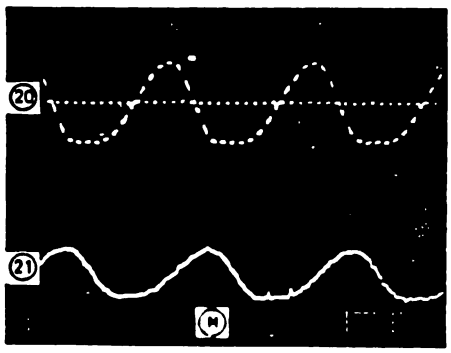
⑯ μPD933AC (M) SH signal
PCB M5154-MA1M
μPD933AC (M) pin 13
10μS/div, 0.2V/div

⑰ μPD933AC (S) SH signal
PCB M5154-MA1M
μPD933AC (S) pin 13
10μS/div, 0.2V/div



⑱ LFO1 output
PCB M5154-MA2M
Refer to page 12
0.5S/div, 0.1V/div

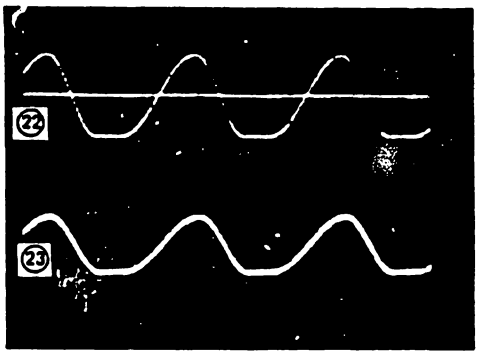
⑲ LFO2 output
PCB M5154-MA2M
Refer to page 12
0.5S/div, 0.1V/div



⑳ DAC output
PCB M5154-MA1M
TL082-1 pin 1
0.5mS/div, 0.2V/div

㉑ Stereo chorus output
PCB M5154-MA2M
LA6462D-5 pin 7
0.5mS/div, 5mV/div

Tone: Flute, Key: A3

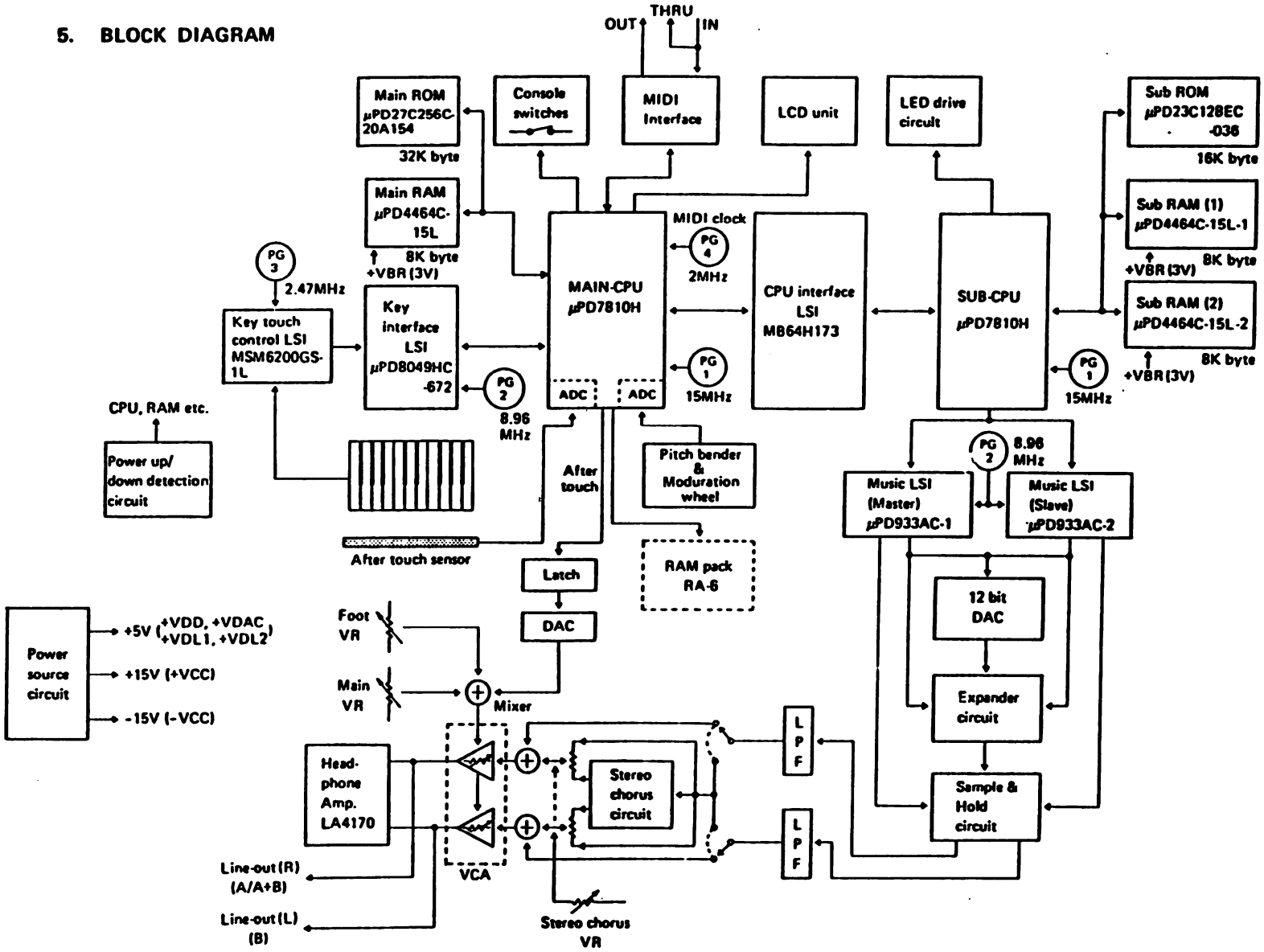


㉒ DAC output
PCB M5154-MA1M
TL082-1 pin 1
0.5mS/div, 0.2V/div

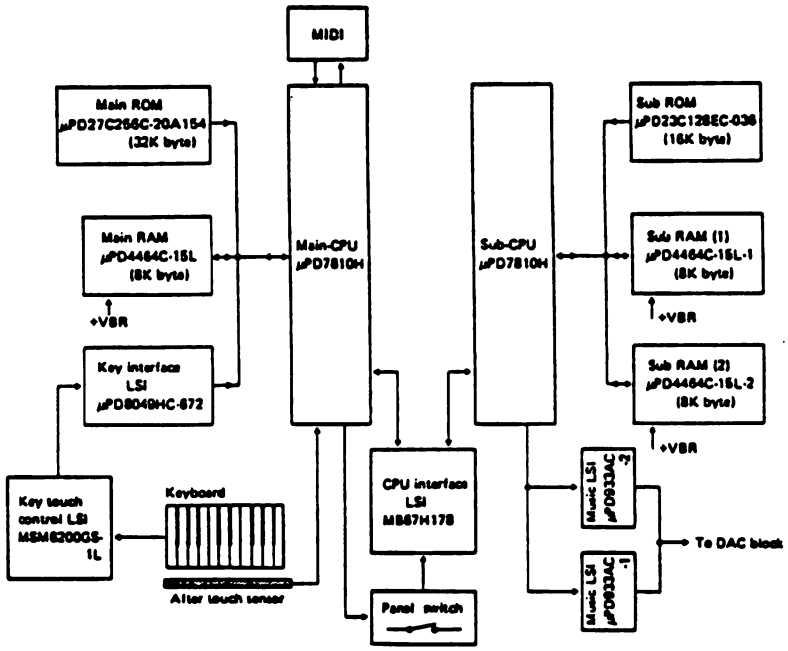
㉓ LINE-OUT putput
A/A+B LINE-OUT terminal
0.5mS/div 10mV/div

Tone: Flute, Key: A3, Volume: Max., Stereo chorus: OFF

5. BLOCK DIAGRAM



6. DIGITAL CIRCUIT BLOCK DIAGRAM



CZ-1 employs five control LSIs for quick processing.

(1) Main CPU Block

The block mainly controls operation of the digital circuits.

Main CPU ..... Controls keys, switch scanning, memory devices and MIDI.

Main ROM ..... Contains program for system execution.

Main RAM ..... Has work area for system execution and stores operation memories and tone name data.

Key interface LSI .... A buffer for data communication between CPU and Key touch control LSI.

Key touch control LSI ... Detects key entry and initial key touch speed.

(2) Sub CPU Block

The block mainly controls music LSIs.

Sub CPU ..... Controls music LSIs and memory devices.

Sub ROM ..... Contains program for system execution and data for preset tones.

Sub RAM (1) ... Stores data area for created sound.

Sub RAM (2) ... Work area for system execution.

Music LSIs ..... Refer to page 42.

(3) CPU Interface LSI ... Interfaces between Main CPU and Sub CPU.

7. CPU (μPD7810H)

As CPU (μPD7810H) does not have a internal ROM, it accesses control data for system execusion from a external ROM directly.
Main CPU and Sub CPU have different functions.

7-1. Pin Functions of Main CPU

Pin No.	Terminal Name	In/Out	Function
1 ~ 8	PA0(S0) ~ PA7 (S7)	In/Out	Data bus for LCD and RAM pack. Signal PA0~PA3 also generate key common signal.
9	PB0 (SYC)	In	Synchronous signal from CPU interface LSI (MB64H173).
11	PB2 (INT)	Out	Sub CPU interrupt signal.
12	PB3 (CONT)	In/Out	Control signal between Main and Sub CPUs.
13	PB4 (RCE)	Out	Chip enable signal for RAM pack.
14	PB5 (RS)	Out	Control signal for LCD unit.
15	PB6 (R/W)	Out	Read/Write signal for RAM pack and LCD unit.
16	PB7 (LE)	Out	Enable signal for LCD unit.
17	PC0 (TXD)	Out	MIDI (Musical Instrument Digital Interface) data output.
18	PC1 (RXD)	In	MIDI data input.
19	PC2 ($\overline{SCK}$)	In	MIDI clock pulse input.
20	PC3 (INT49)	In	Interrupt signal from Key interface LSI (μPD8049HC).
21	PC4 (CNT49)	Out	Control signal of Key interface LSI (μPD8049HC).
22	PC5 (CI)	In	Timing signal of data transmission between Main CPU and Key touch control LSI (MSM6200).
24	PC7 (TST)	Out	Check signal for internal ROM/RAM of Key interface LSI (μPD8049HC) at power ON.
26	INT1 (X896)	In	Interrupt signal from Sub CPU.
28	$\overline{RESET}$	In	Reset signal input. CPU internal circuits are initialized when the terminal receives a LOW level pulse at power ON.
31	X1	In	15MHz clock pulse input.
32	Vss		Ground (0V) source.
33	AVss		Ground (0V) source for internal ADC (Analog to Digital Converter)
34	AN0	In	Modulation wheel input. Voltage level from modulation wheel is converted into digital data by built-in ADC.
35	AN1	In	Pitch bender wheel input. Voltage level from pitch bender wheel is converted into digital data by built-in ADC.
36	AN2	In	After touch sensor input. Voltage level from after touch sensor is converted into digital data by built-in ADC.
42	VAREF		Reference voltage (+5V) for built-in ADCs.
43	AVcc		+5V power source for built-in ADCs.
44	$\overline{RD}$	Out	Read signal output. Drops to LOW when Main CPU reads data from peripheral devices.

Pin No.	Terminal Name	In/Out	Function
45	$\overline{WR}$	Out	Write signal output. Drops to LOW when Main CPU writes data into peripheral devices.
46	ALE	Out	Address latch enable signal output. Data signals D0~D7 become address signals A0~A7 when the terminal rises to HIGH.
47~54	PF0 (A8) ~ PF7 (A15)	Out	Upper address signals (A8 ~ A15).
55~62	PD0 (D0) ~ PD7 (D7)	In/Out	Data signals (D0 ~ D7).
63, 64	VDD, Vcc		+5V power source.

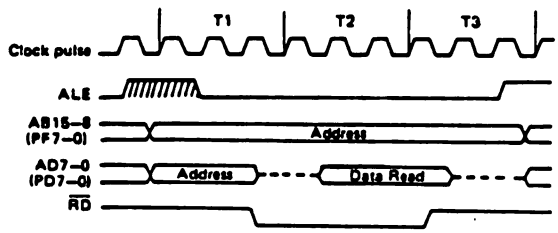
7-2. Pin Functions of Sub CPU

Pin No.	Terminal Name	In/Out	Function
1 ~ 8	PA0 (L0) ~ PA7 (L7)	Out	LED drive signals output.
9	PB0	In	Interrupt request signal input from Master Music LSI.
10	PB1	In	Interrupt request signal input from Slave Music LSI.
11	PB2	Out	Master Music LSI chip select signal output.
12	PB3	Out	Slave Music LSI chip select signal output.
13	PB4	Out	Write enable signal for Music LSIs.
14	PB5	Out	ID (Interrupt Disable) signal output. When Sub CPU is busy, it sends ID signal to Music LSIs so as not to be interrupted.
15	PB6 (LDC)	Out	Stays HIGH level for approximately 830 milliseconds after power switch is turned on in order to avoid mis-lighting of LEDs and shock noise on power UP.
17	PC0 (L11)	Out	LED drive signal output.
18	PC1 (SYC)	In	Synchronous signal from Main CPU.
19	PC2 (CONT)	In/Out	Control signal between Main and Sub CPUs.
20	PC3 ($\overline{INT2}$)	In	Interrupt signal from Music LSIs.
22~24	PC5 (L8) ~ PC7 (L10)	Out	LED drive signals output.
26	INT1	In	Interrupt signal from Main CPU.
28	$\overline{RESET}$	In	Reset signal input. The terminal receives a LOW level pulse at power ON. CPU internal circuits are initialized then.
31	X1	In	15MHz clock pulse input.
32	Vss		Ground (0V) source.
44	$\overline{RD}$	Out	Read signal output. Drops to LOW when Sub CPU reads data from peripheral devices.
45	$\overline{WR}$	Out	Write signal output. Drops to LOW when Sub CPU writes data into peripheral devices.
46	ALE	Out	Address latch enable signal output. Data signals D0~D7 become address signals AS0~AS7 when the terminal rises to HIGH.

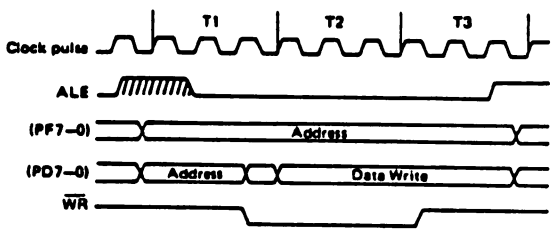
Pin No.	Terminal Name	In/Out	Function
47~54	PF0 (AS8) ~ PF7 (AS15)	Out	Upper address signals (AS8 ~ AS15).
55~62	PD0 (DS0) ~ PD7 (DS7)	In/Out	Data signals (DS0 ~ DS7).
63, 64	VDD, Vcc		+5V power source.

Data Read and Write Timing Chart

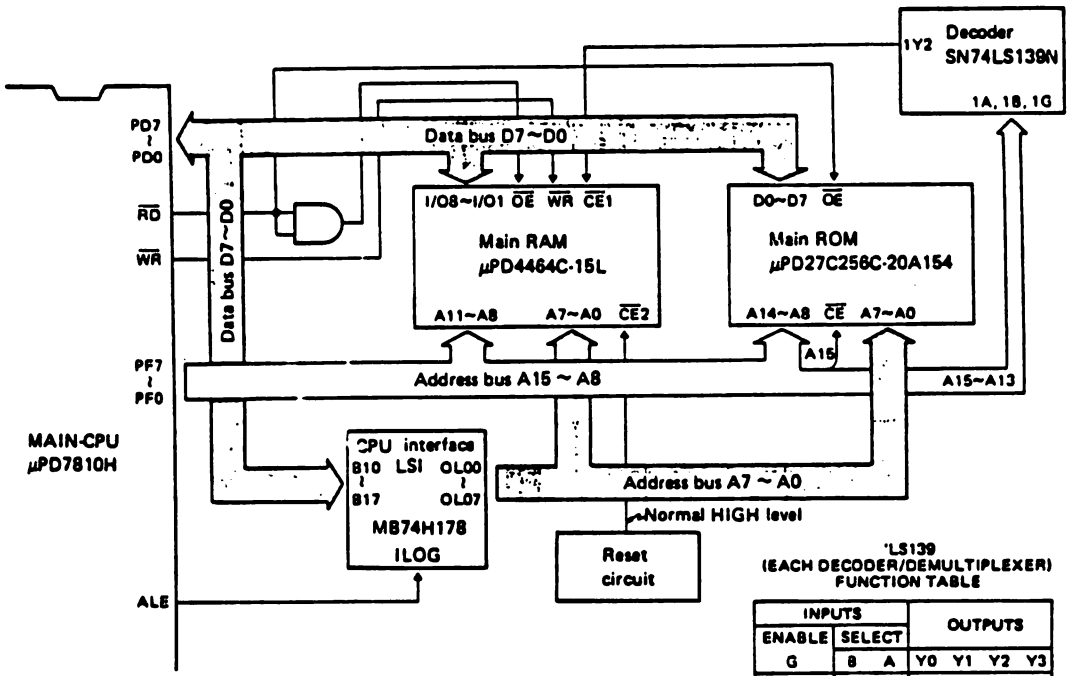
Data Read



Data Write



8. MAIN RAM & ROM ACCESSES



'LS139
(EACH DECODER/DEMULTIPLEXER)
FUNCTION TABLE

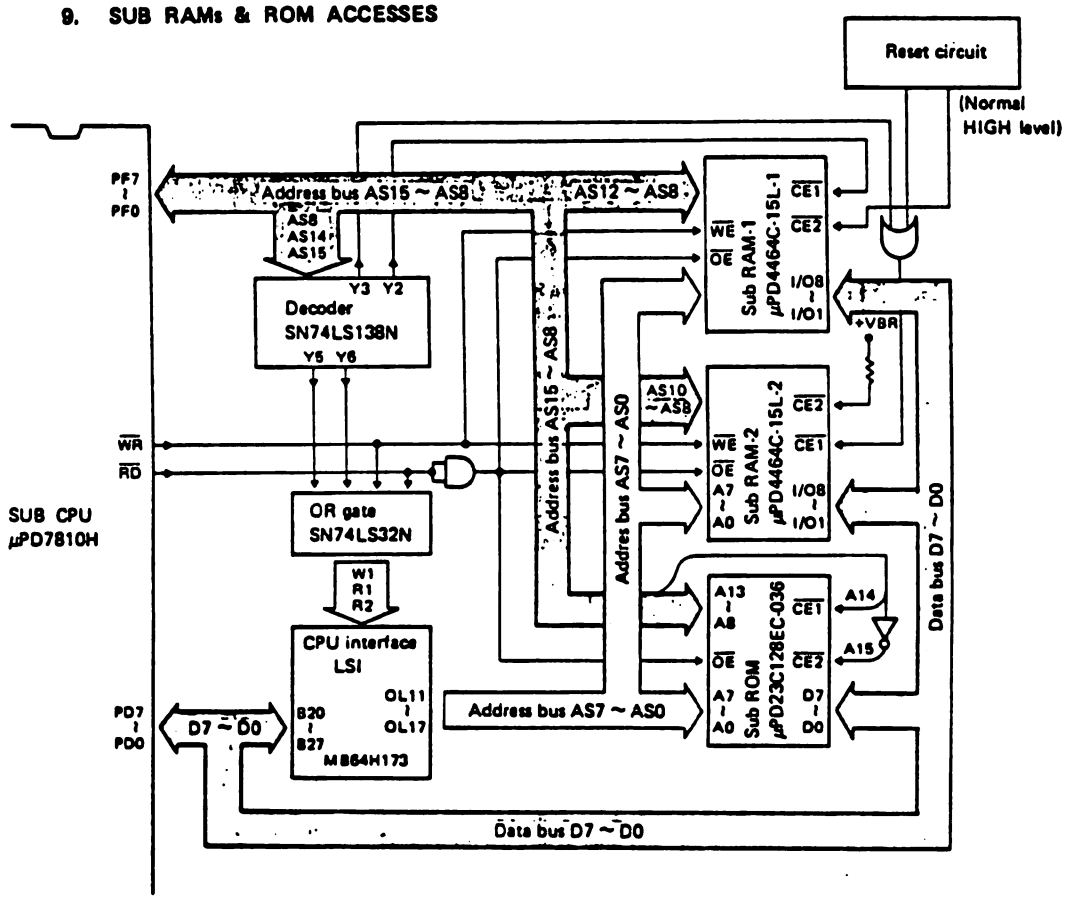
INPUTS			OUTPUTS			
ENABLE	SELECT					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = irrelevant

8K byte of Main RAM is the data area as written on page 17.
The RAM is backed up by +VBR (3V) of lithium battery.
The capacity of Main ROM is 32K byte and containts program for the system execution.
Lower address bus (A0 ~ A7) is provided from CPU interface LSI (MB74H178).
When signal ALE from Main CPU rises to HIGH, data bus (D0 ~ D7) becomes address bus (A0 ~ A7) in CPU interface LSI (MB74H178). Upper address bus A8 ~ A15 is directly supplied from Main CPU.
Chip select signals are from signals A13 ~ A15.

Chip selection	A13	A14	A15	$\overline{WR}$	$\overline{RD}$
Main RAM	LOW	LOW	HIGH	H or L	HIGH
Main ROM	–	–	LOW	–	LOW

9. SUB RAMs & ROM ACCESSES



μPD4464C-15L is an 8K byte RAM while μPD23C128EC is a 16K byte ROM.

Refer to page 17 for the functions of each device.

In the same procedures as for Main CPU, lower address bus (AS0 ~ AS7) is generated from data bus (DS0 ~ DS7) in CPU interface LSI (MB64H173) when signal ALE is HIGH. Upper address bus (AS8 ~ AS15) are provided from Sub CPU directly.

Chip select signals are generated from signals AS8, AS14 and AS15.

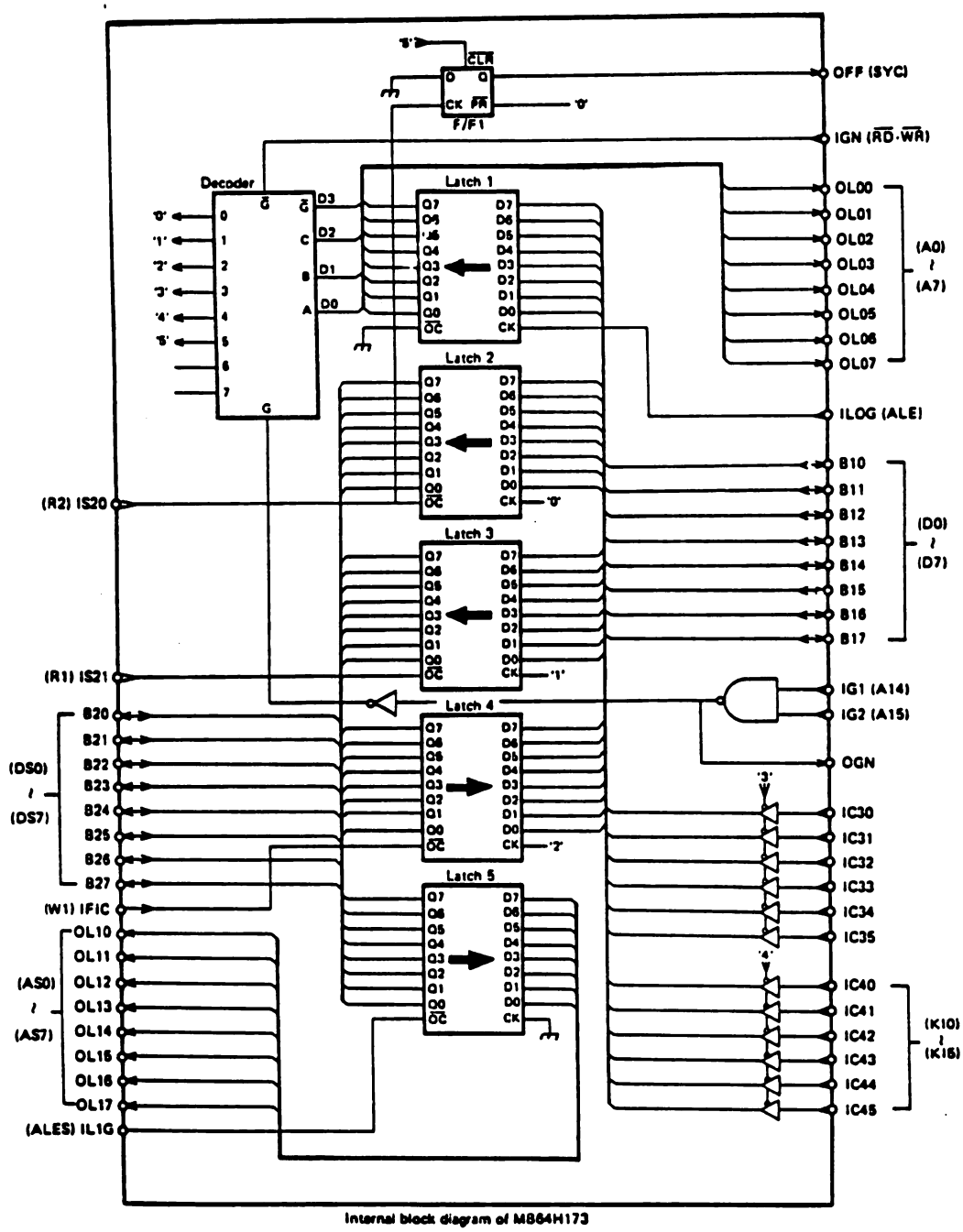
Chip selection	AS8	AS14	AS15	$\overline{WR}$	$\overline{RD}$
RAM-1	LOW	HIGH	LOW	L or H	HIGH
RAM-2	HIGH	HIGH	LOW	L or H	HIGH
ROM	–	LOW	HIGH	–	LOW

'LS138
FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B
H = high level, L = low level, X = irrelevant

10. CPU INTERFACE LSI (MB64H173)



Internal block diagram of MB64H173

10-1. Function of Each Block

F/F 1 – Set by the clock pulse '0' and signal R2 from SUB CPU, and generates signal SYC which synchronizes MAIN and SUB CPUs.

FUNCTION TABLE

INPUT				OUTPUT	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

Decoder 1 – Generates clock pulses for the latches from signals A0 ~ A3, A14, A15, $\overline{P.D}$ and $\overline{WR}$.

FUNCTION TABLE

ENABLE INPUT		SELECT INPUT			OUTPUT							
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*$\overline{G2} = \overline{G2A} + \overline{G2B}$

Latch 1 – Converts MAIN CPU's data bus (D0 ~ D7) into address bus A0 ~ A7, and generates clock pulses '0' ~ '5'.

Latch 2 – For data transfer from MAIN CPU to SUB CPU.

Latch 3 – Transfers data from pitch bender and modulator wheel to SUB CPU.

Latch 4 – For data transfer from SUB CPU to MAIN CPU.

Latch 5 – Converts SUB CPU's data bus (DS0 ~ DS7) into address bus AS0 ~ AS7.

FUNCTION TABLE (EACH LATCH)

INPUT			OUTPUT
$\overline{OC}$	ENABLE C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

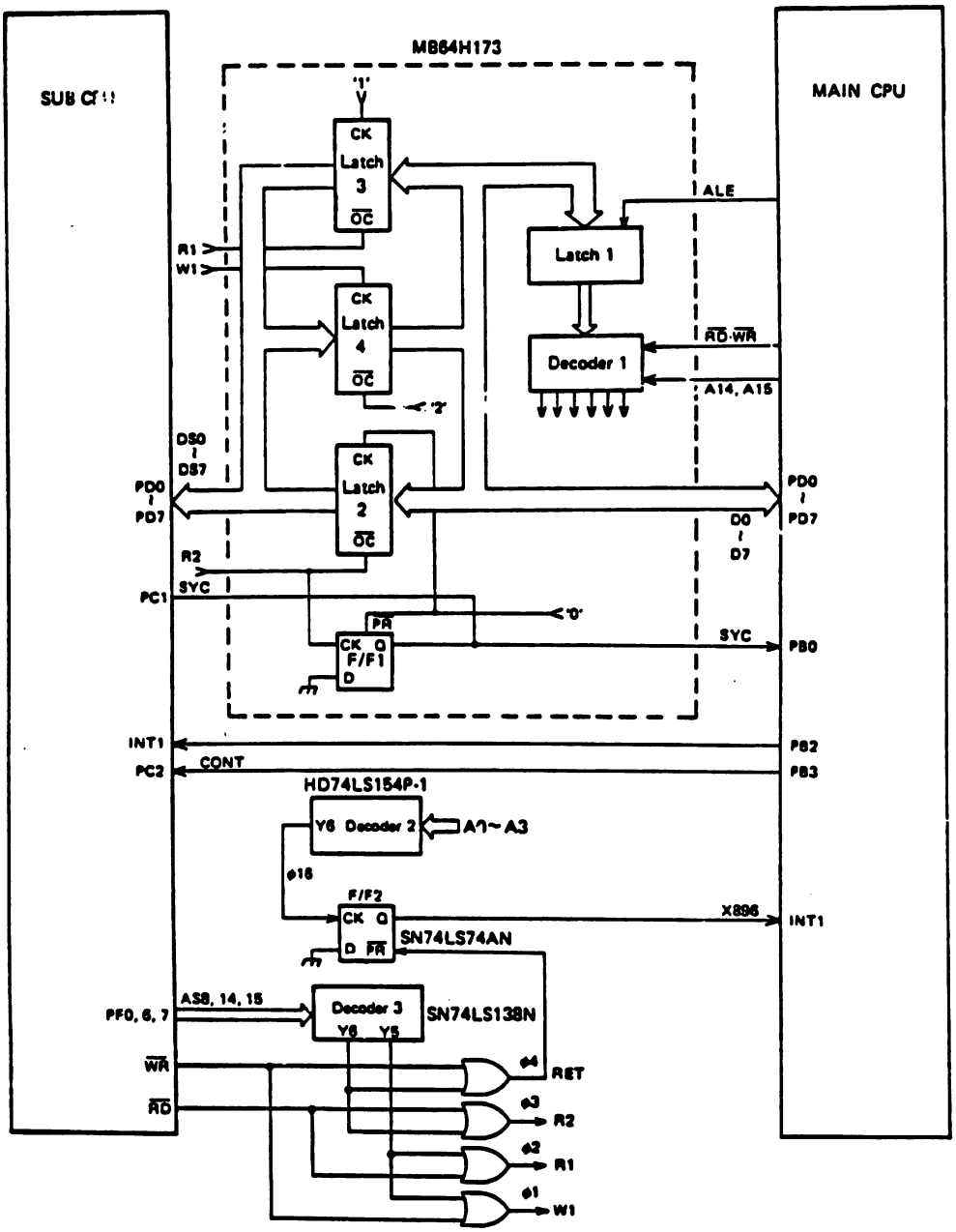
Latch 1 and 5

FUNCTION TABLE (EACH FLIP-FLOP)

INPUT			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

Latch 2 ~ 4

10-2. Data Transfer Procedures



(1) Pitch Bender & Modulator ⇨ SUB CPU.

① Voltage level from the pitch bender or the modulator is converted into digital data in the CPU's built-in ADC (Analog to Digital Converter) and output from data bus (D0 ~ D7).

② The data is entered into CPU Interface LSI.

③ Sending signal R1, SUB CPU sets Latch 3 and reads data periodically.

(2) MAIN CPU ⇨ SUB CPU.

① Via Latch 1 and Decoder 1, MAIN CPU drops clock pulse '0' to LOW level.
By clock pulse '0', F/F 1 is preset to rise signal SYC.

② MAIN CPU puts data on data bus D0 ~ D7, and at the same time, clock pulse '0' rises to HIGH level.
At the rising edge of clock pulse '0', data from MAIN CPU is set in Latch 2.

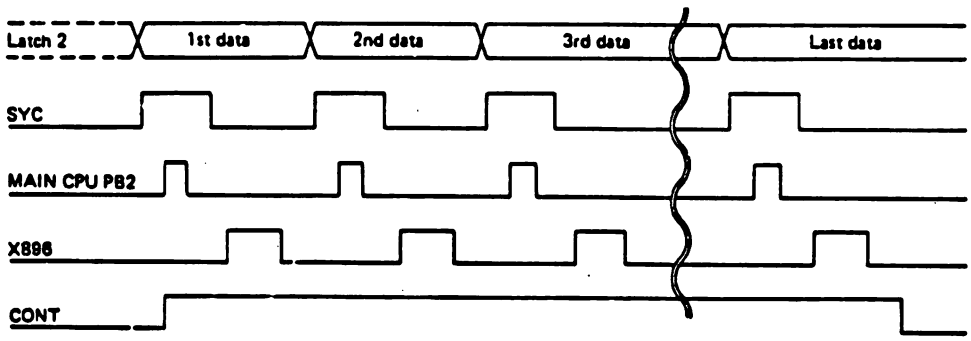
③ MAIN CPU interrupts SUB CPU from terminal PB2, and simultaneously generates signal CONT from terminal PB3.

④ Generating signal R2 from Decoder 3, SUB CPU reads the data from Latch 2 via data bus DS0 ~ DS7.

⑤ SUB CPU sends signal ACK to MAIN CPU via Decoder 3 and F/F 2.
Upon receipt of signal ACK, MAIN CPU confirms that SUB CPU has received the data and generates signal ϕ16 in Decoder 2.

⑥ When all the data have sent to SUB CPU by repeating the above procedures ①~⑤, MAIN CPU drops signal CONT to LOW.

⑦ Confirming that both CONT and SYC are LOW, SUB CPU determines that all the data have been received.



(3) SUB CPU ⇨ MAIN CPU.

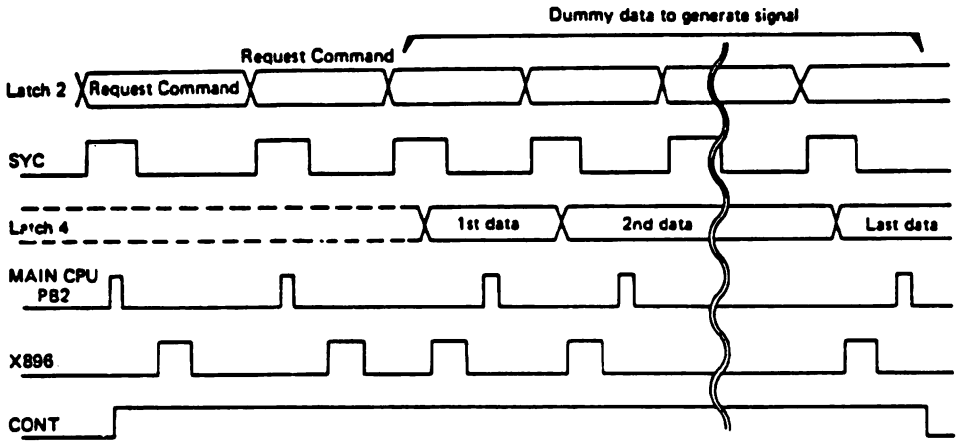
① In the same procedures as stated in the item (2), MAIN CPU sends "Request Command" that inquires SUB CPU to transmit data.

② SUB CPU puts data on data bus DS0 ~ DS7 and sets the data in Latch 4 by signal W1. SUB CPU then presets F/F 2 by pulse ϕ4, causing signal X896 to be entered in MAIN CPU.

③ Acknowledging that data is set in Latch 4 by signal X896, MAIN CPU generates clock pulse '2', causing data from SUB CPU to be put on MAIN CPU data bus D0 ~ D7.

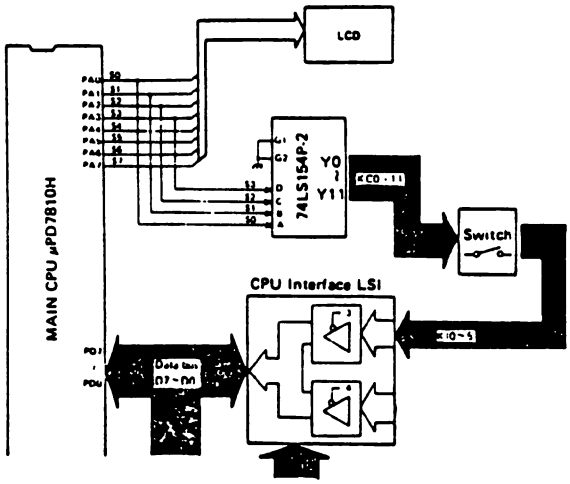
④ After receiving data, MAIN CPU sends SUB CPU an interrupt signal from terminal PB2, and by interrupt signal, SUB CPU confirms that the data is received by MAIN CPU.

⑤ Repeating the above procedures ②~④, SUB CPU sends the next data to MAIN CPU.



(4) Key and switch scanning

Receiving a key common signal from data bus, MAIN CPU discriminates a key or a switch input.



(1) From signals PA0 ~ PA3 of MAIN CPU, 4-line to 16-line decoder 74LS154P-2 generates key common signals KC0 ~ KC11.

(2) When a switch is put, one of the input signals KI0 ~ KI5 (for switches) is entered in CPU Interface LSI MB64H173.

(3) MAIN CPU generates the clock pulse '4' (for switches), causing the tristate buffers to be opened.

(4) The input pulse is entered into data bus.

(5) Discriminating the contents of the data bus, MAIN CPU determines which switch is pushed.

INPUT						OUTPUT													
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

74LS154P Function Table

10-3. Switch Matrix

	KI 5	KI 4	KI 3	KI 2	KI 1	KI 0
KC 0	MIDI	SOLO	OPERATION MEMORY	KEY SPLIT	TONE MIX	NORMAL
KC 1	CARTRIDGE	EXCHANGE	MASTER TUNE	KEY TRANSPOSE	GLIDE ON/OFF	PORTAMENTO ON/OFF
KC 2	BANK F	BANK E	BANK D	BANK C	BANK B	BANK A
KC 3	BANK H	BANK G	MEMORY 8	MEMORY 7	MEMORY 6	MEMORY 5
KC 4	MEMORY 4	MEMORY 3	MEMORY 2	MEMORY 1	YES →	NO ←
KC 5	VALUE ▲ LOAD	VALUE ▼ SAVE	ENV. POINT END	ENV. POINT SUSTAIN	PAGE UP	PAGE DOWN
KC 6	CARTRIDGE SAVE/LOAD	NAME	PORTAMENTO	GLIDE	BEND RANGE	WHEEL/ AFTER TOUCH
KC 7	NOISE	RING	LINE SELECT	VIBRATO	OCTAVE	INITIALIZE
KC 8	DCA 1 ENV	DCA 1 KEY FOLLOW	DCW 1 ENV	DCW 1 KEY FOLLOW	DCO 1 ENV	DCO 1 WAVE FORM
KC 9	DCA 2 ENV	DCA 2 KEY FOLLOW	DCW 2 ENV	DCW 2 KEY FOLLOW	DCO 1 ENV	DCO 1 WAVE FORM
KC10	DETUNE	PARAMETER COPY	DCA 2 LEVEL	DCA 1 LEVEL	DCA 2 VELOCITY	DCA 1 VELOCITY
KC11	SUSTAIN PEDAL	PROTECT ON/OFF	MODULATION ON/OFF	WRITE	COMPARE/ RECALL	MIDI ON/OFF
KC12						PACK DETECTION

11. KEYBOARD

CZ-1 varies the sound volume in accordance with the key touch speed and depression strength.

11-1. Key Touch Speed Detection

Each key has two key contact switches S1 and S2.

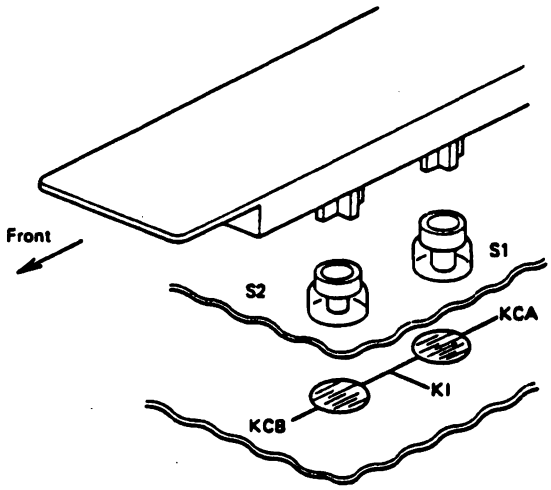


Fig. 11-1

When a key is hit, S1 turns on first, then S2.

The interval time between turning on of S1 and S2 varies according to the touch speed of the key.

LSI MSM 6200 detects the time interval and determines the key touch speed.

Some RC (resistor and capacitor) integrating circuits are connected to the MSM6200 and when switch S1 turns on, the RC circuit starts to discharge. The discharging stops when S2 turns on.

The MSM 6200 also contains an ADC (Analog to Digital Converter) and changes the voltage Vc of the RC circuits into a 5-bit digital signal which is sent to the CPU as key entry and hitting speed data.

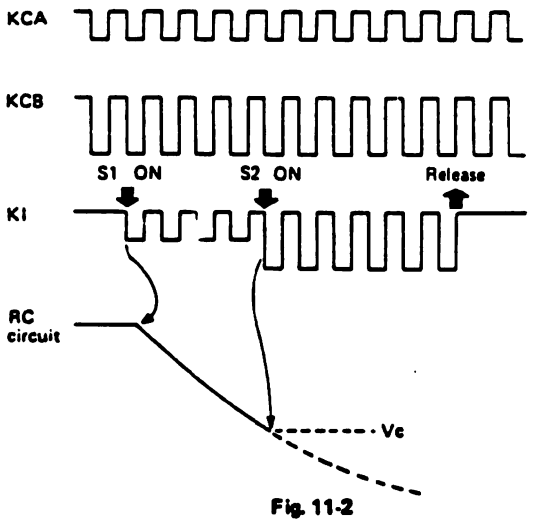
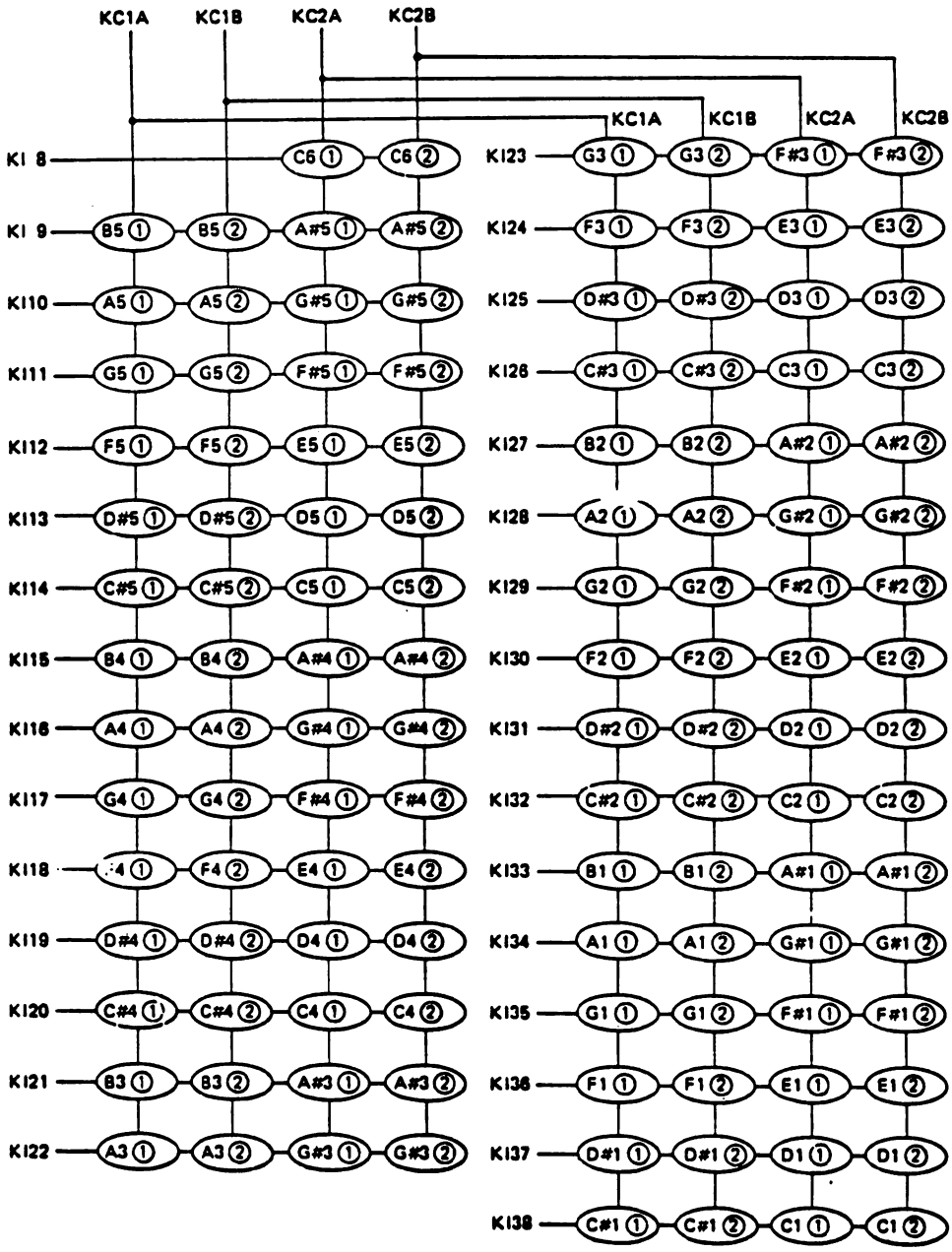


Fig. 11-2

11-2. Key Matrix



11-3. Pin Functions of Key Touch Control LSI (MSM6200)

Pin No.	Terminal Name	In/Out	Function
1 ~ 8	IR8 ~ IC8	In/Out	External RC discharging circuit inputs and outputs.
10	REF		Reference voltage (+5V).
11	AG		Analog ground.
20	O1	Out	Interrupt request signal output. When LOW, MSM6200 interrupts the CPU.
25~28 29~32	O2 ~ O5 IO1 ~ IO4	Out In/Out	Upper 4-bit data bus. Lower 4-bit data bus. $\underline{O2}$ O3 O4 O5 IO1 IO2 IO3 $\underline{IO4}$ MSB LSB
34	I 2	In	ALE (Address Latch Enable) signal input. When HGIH, address in MSM6200 is assigned.
35	I 3	In	$\overline{WR}$ signal input. When LOW, data or address can be written in MSM6200.
36	I 4	In	$\overline{RD}$ signal input. When LOW, CPU reads data from MSM6200.
37	I 5	In	$\overline{CS}$ (chip select) signal input. When LOW, communications between the CPU and MSM6200 is possible.
39	I 10	In	Reset signal input. LOW: Active. At power on, receives a reset signal to initialize MSM6200's internal circuits.
40	VDD		+5 volt source.
43	PGI	In	Clock pulse (2.47 MHz) input.
45	VSS2		Ground (0 volt) source.
46	VSS1		+2.25 volt source.
47~60	KC2B~KC1A	Out	Key common signal outputs.
58~68	K8 ~ K38	In	Key input terminals.
91~100	IR1 ~ IC5	In/Out	External CR circuits inputs and outputs.

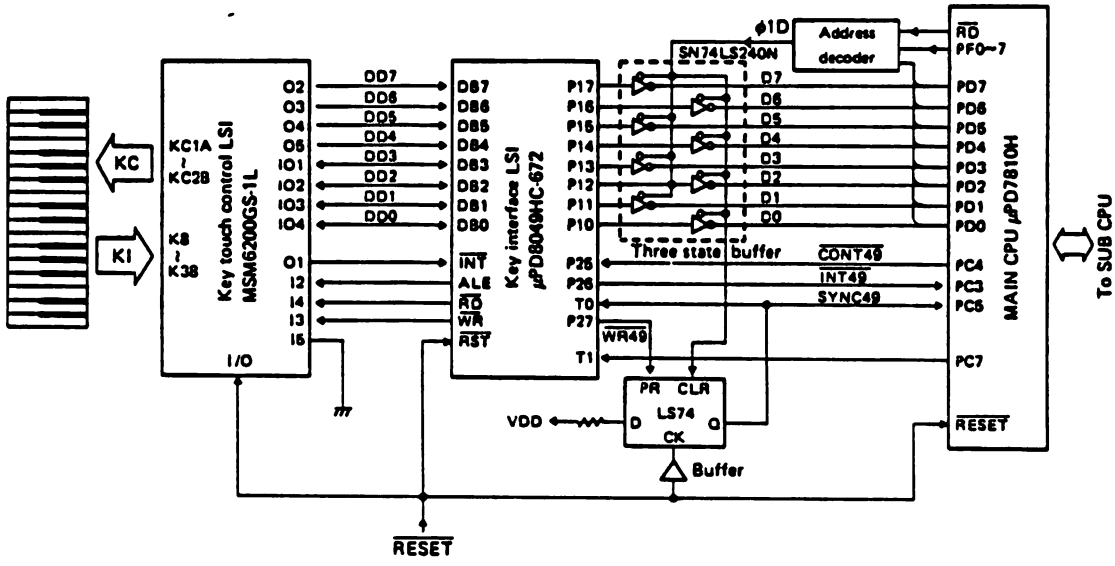
11-4. Pin Functions of Key Interface LSI (μPD8049HC)

Pin No.	Terminal Name	In/Out	Function
1	T0	In	Clock pulse input for data read/write.
2	XTAL1	In	8.96 MH clock pulse input.
4	$\overline{RESET}$	In	At power ON, the terminal stays LOW level for a while in order to initialize internal circuits.
6	$\overline{INT}$	In	Interrupt signal input from MSM6200.
8	$\overline{RD}$	Out	Read signal output. Key interface LSI reads data from MSM6200 when terminal is LOW.
10	$\overline{WR}$	Out	Write signal output. Key interface LSI writes data or address in MSM6200 when terminal is LOW.
11	ALE	Out	ALE (Address Latch Enable) signal output. Address in MSM6200 is assigned when HIGH level.

Pin No.	Terminal Name	In/Out	Function
12~19	DB0 ~ DB7	In/Out	Data bus (D0 ~ D7) between MSM6200.
20	Vss		Ground (0V) source.
26	VDD		+5V source.
27~34	P10 ~ P17	Out	Data bus (D0 ~ D7) between Main CPU.
36	P25 (CNT49)	In	Control signal input from CPU.
37	P26 (INT49)	Out	Interrupt signal output to CPU.
38	P27 (WR49)	Out	Timing pulse output for data read/write.
39	T1 ($\overline{TST}$)	In	Test signal input. Key interface LSI does selfcheck of internal RAM/ROM at LOW.
40	VCC		+5V source.

11-5. Key Touch Data Communication

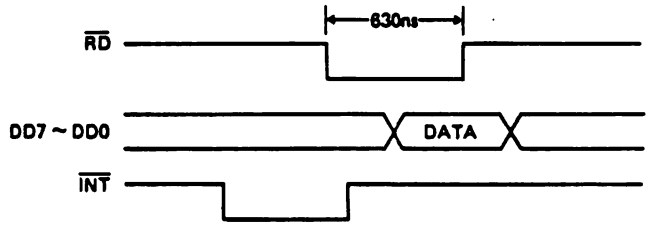
(1) Block Diagram



Key touch control LSI fetches the data of key entry and key touch speed from keyboard, then the data are transmitted to Main CPU via Key interface LSI which is a buffer.
The Key interface LSI quicken the data communication between the Key touch control LSI and the CPU.

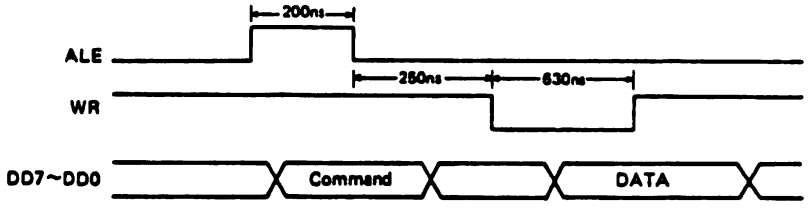
(2) Timing chart from MSM6200 to μPD8049HC

For sending mainly key entry and initial touch data.



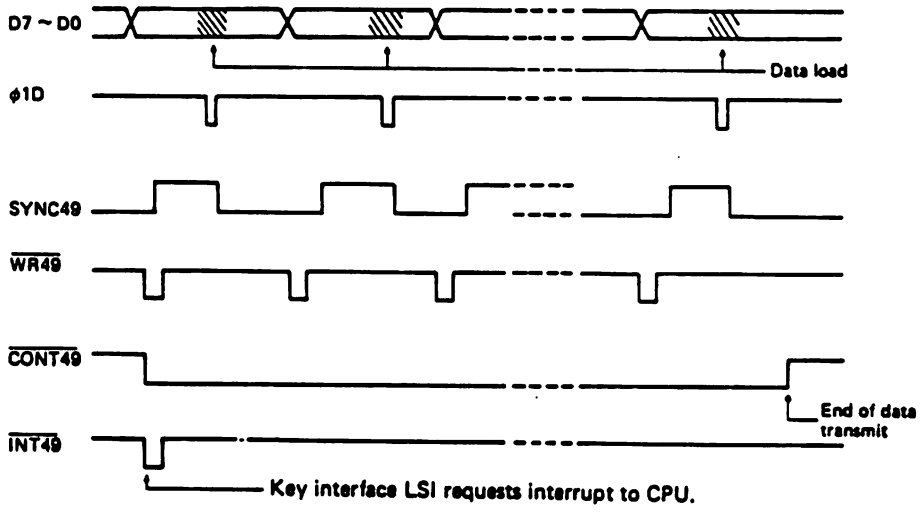
(3) Timing chart from μPD8049HC to MSM6200

For sending mainly request command of key entry and key touch speed data.

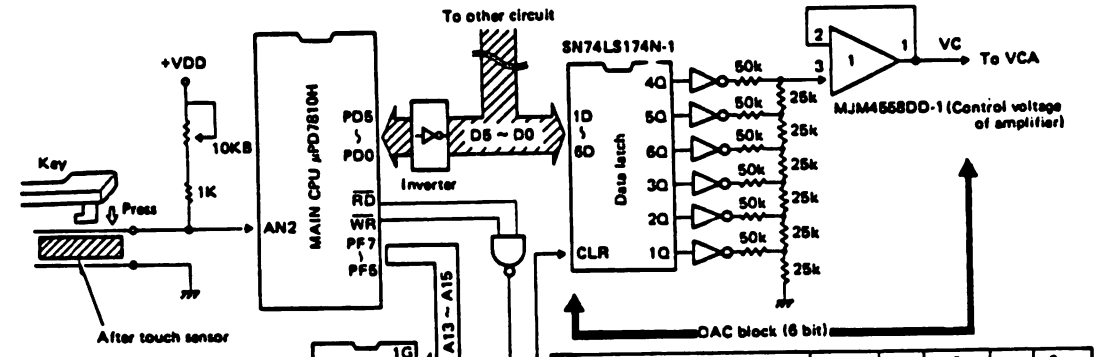


(4) Timing chart from μPD8049HC to MSM6200

For transmitting mainly key entry and key touch speed data in this process.



11-6. After Touch Control Circuit



AFTER TOUCH PARAMETER		15	~	8	~	0
VC output	No pressure	+3.8V	~	+2.0V	~	GND
	Pressure Max.	GND	~	GND	~	GND

'LS139
(EACH DECODER/DEMULTIPLEXER)
FUNCTION TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = irrelevant

LS174
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
† = '176, 'LS175, and 'S175 only

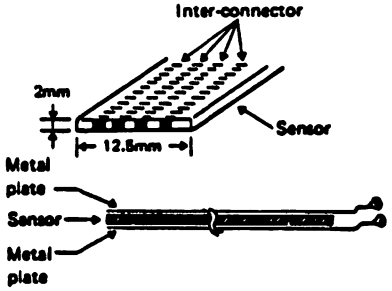
(1) When the after touch sensor is pressed harder, its resistance becomes lower dropping the voltage level of terminal AN2.

(2) Main CPU convertes analog signal into digital data in the internal ADC (Analog to Digital Converter), then output the data to DAC (Digital to Analog Converter) block.

(3) These data are converted to analog signal by DAC block.

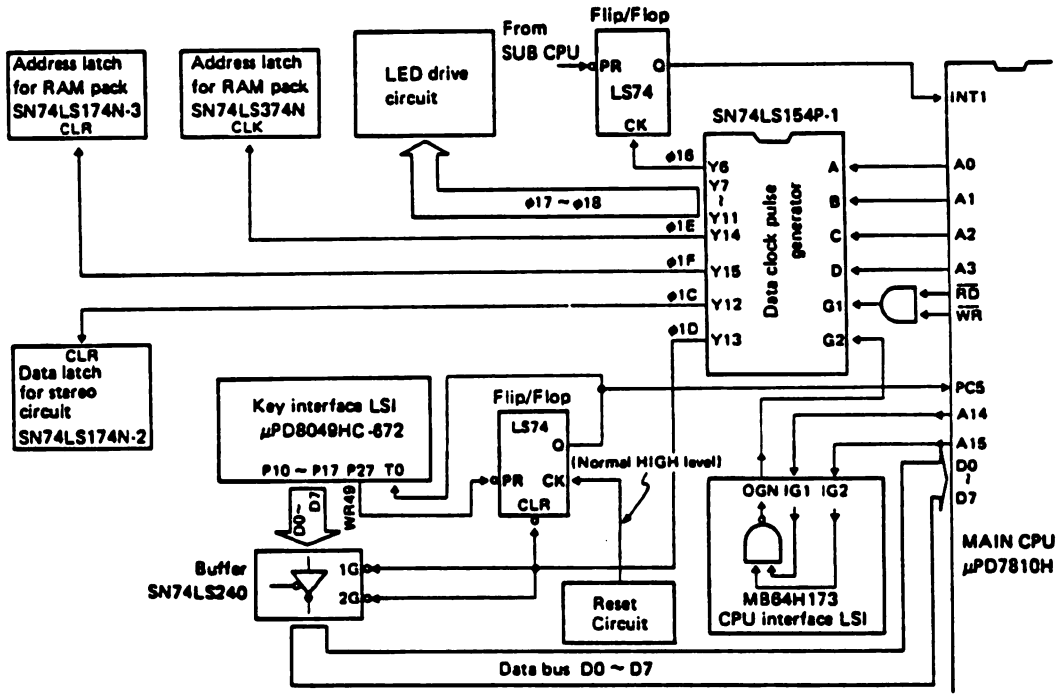
(4) The output voltage VC is input to VCA (M5241L) on PCB AS1M, to vary the amplitude of the VCA.

Note: Construction of after touch sensor.



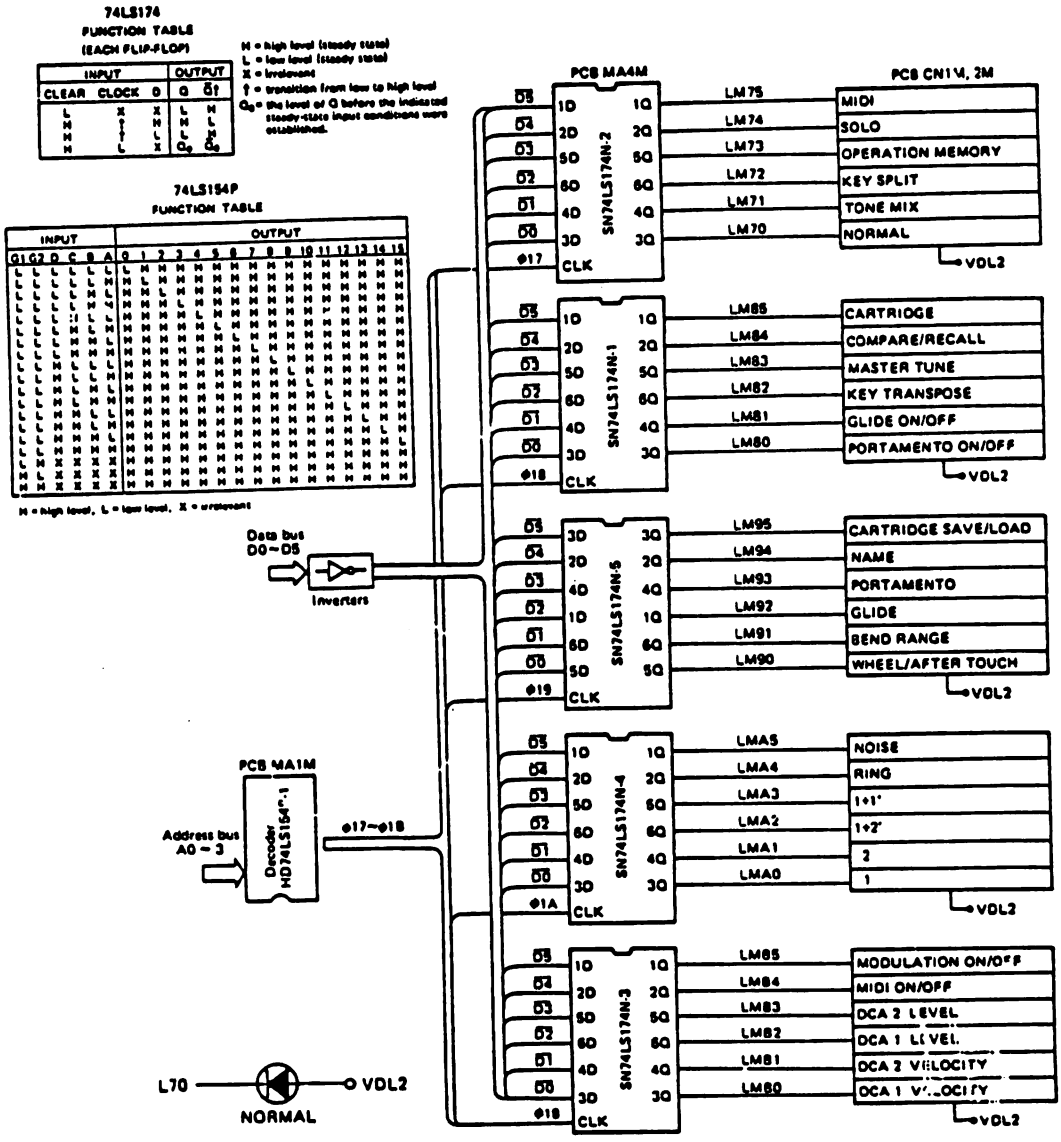
After touch sensor is a sheet of silicon rubber in which carbon particles are inlaid.
While no force is applied, the resistance between the both sides is infinity. However, when it is pressed hard, the density of the carbon becomes high causing its resistance to be as small as 10 ~ 30 ohms.
The silicon rubber is put between two thin metal plates.

12. DATA CLOCK PULSE GENERATOR



Terminal	Clock	Function
Y6	φ16	Clock pulse for interrupt from Sub CPU to Main CPU.
Y7~Y11	φ17~φ18	Clock pulse for LED drive circuit.
Y12	φ1C	Clock pulse of control signal for stereo circuit.
Y13	φ1D	Enable signal of buffer (SN74LS240N) and reset pulse of Flip/Flop (SN74LS74) for key data transmission.
Y14, Y15	φ1E, φ1F	ALE (Address Latch Enable) signal for RAM pack.

13. LED DRIVING CIRCUITS



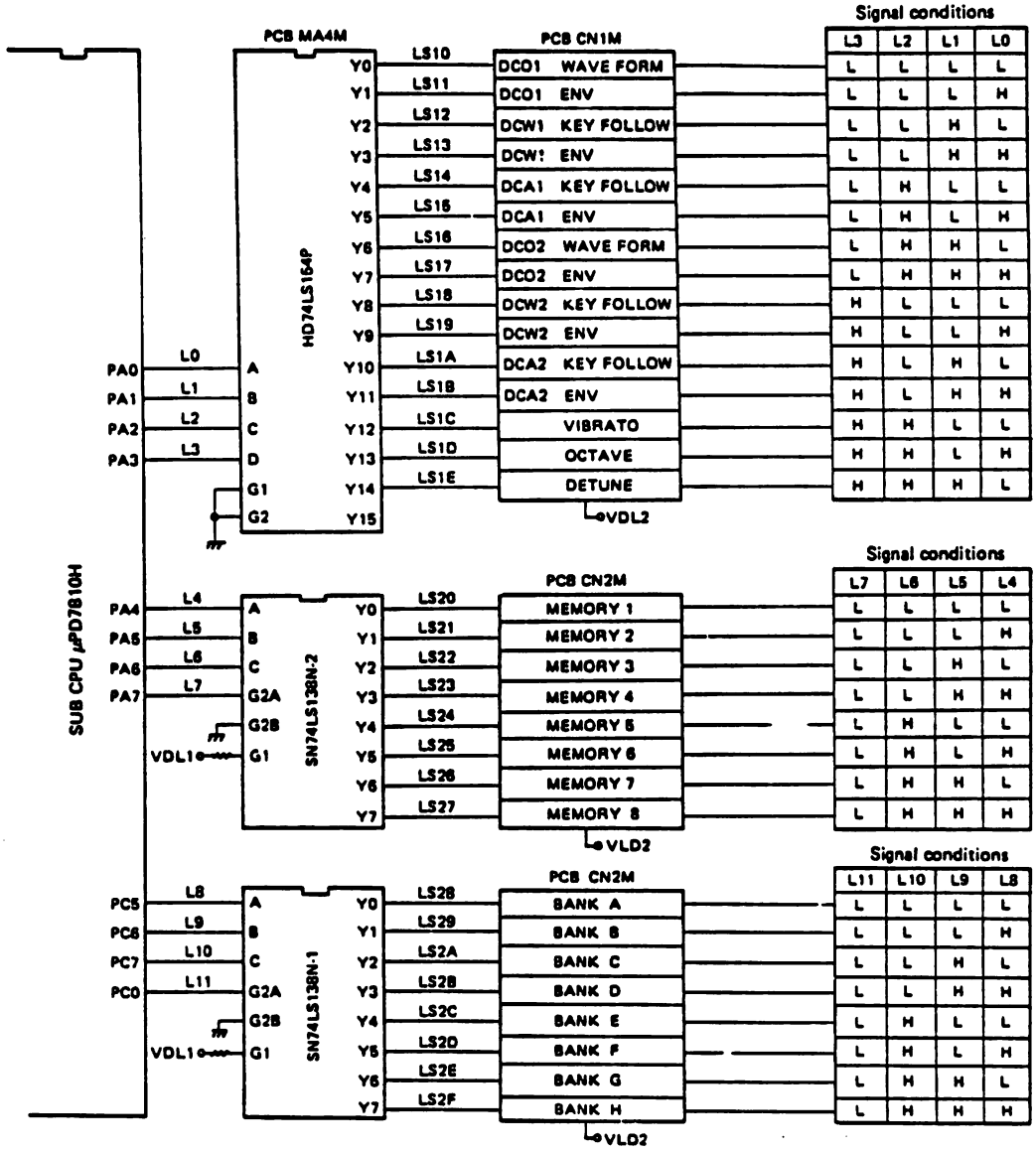
Combining the signals A0 ~ A3, decoder 74LS154P-1 generates signals ϕ17 ~ ϕ1A which are latches 74LS174N-1 ~ 5.

For lighting the LED "NORMAL", MAIN CPU raises signal D0 which is inverted to LOW level.

Then, Main CPU generates clock signal ϕ17 from signals A0 ~ A3.

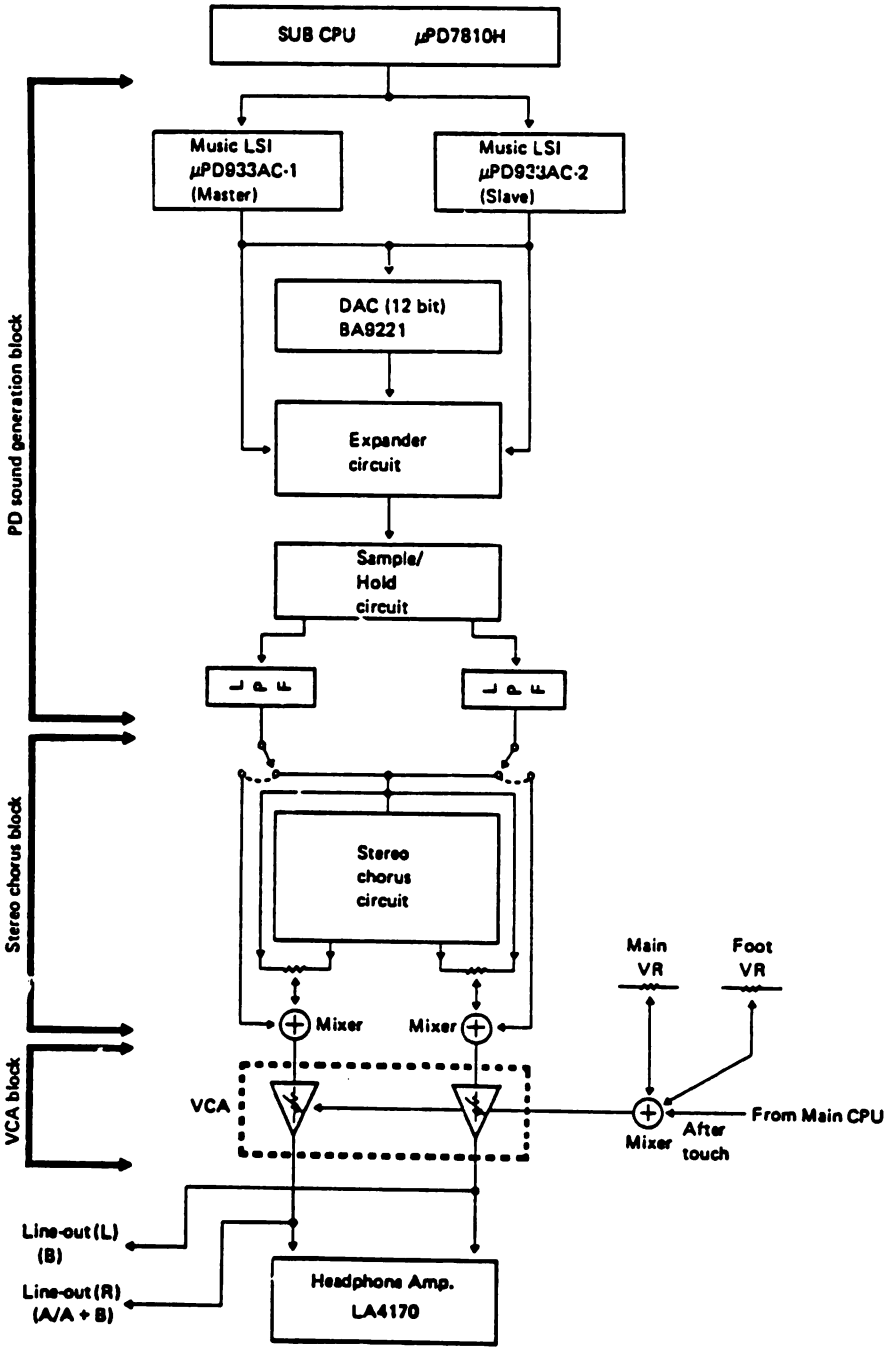
$\overline{D0}$ (= LOW) is set in latch SN74LS174N-1 dropping signal LM70 LOW.

The LED "NORMAL" is lit since its anode is connected to VDL2 (+5V).



These LEDs are controlled by Sub CPU.
For example, when Sub CPU wishes to light the "BANK-A" LED, it drops all the signals L8 ~ L11. Y0 output of Decoder 5 drops to LOW, causing the LED to be lit.

14. ANALOG CIRCUIT BLOCK DIAGRAM



(1) PD (Phase Distortion) Sound Block

Music LSI ..... Two LSIs generate digital PD sound signals as show below.

Mode	NORMAL	TONE MIX	KEY SPLIT
μPD933AC-1 (Master)	Mix	TONE 1	LOW
μPD933AC-2 (Slave)		TONE 2	UPPER

DAC (Digital to Analog Converter) .... Mixes the two different digital signals and converts into an analog signal.

Expander Circuit ..... Music LSIs' outputs are contracted to obtain a wide dynamic range of amplitude. Expander circuit reforms it into a proper waveform.

Sample/Hold Circuit ... Removes a high frequency noise called as glitch contained in the DAC output. Also separates the master and slave waveforms.

(2) After Touch Block

After touch effect gives variation of amplitude and modulation to the output sound.
After touch sensor under the keyboard varies its resistance from infinity to approximately 10ohm by means of pressure strength. The change of the resistance is input to Music LSIs or VAC circuit via main CPU.
The CZ-1 is able to set the depth of the effects by parameter (0 ~ 15).

After touch effect	Flow of after touch signal
Modulation	Sensor ➡ Main CPU ➡ Music LSIs
Amplitude	Sensor ➡ Main CPU ➡ After touch control circuit ➡ VCA circuit

(3) Stereo Chorus Block

Gives stereo effect to the output sound. ON/OFF of stereo effect is input by panel switch.
The stereo chorus effect can be set individually even in Tone Mix or Key Split mode.

Ex.

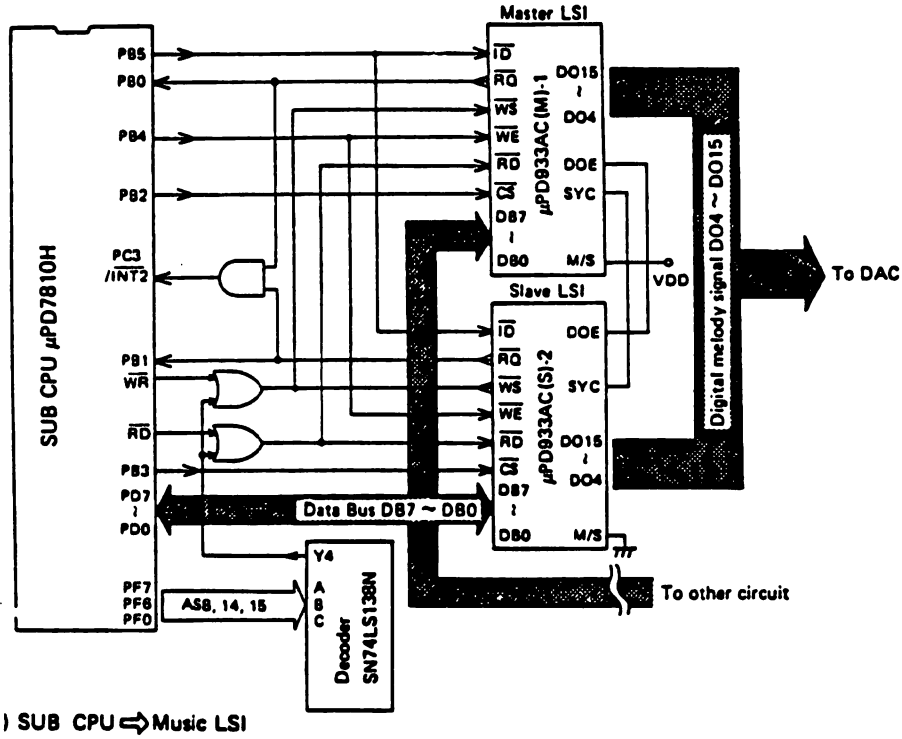
Mode	Stereo effect ON/OFF
Tone mix	Tone 1: ON, Tone 2: OFF
Key split	LOW: OFF, UPPER: ON

(4) VCA (Voltage Controlled Amplifier)

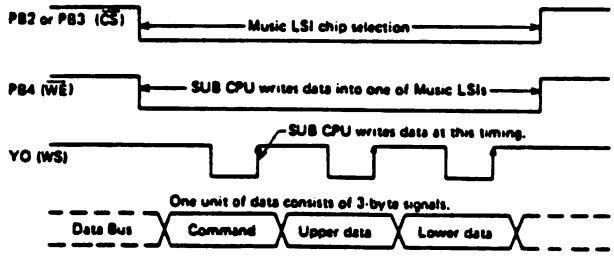
Receives voltage which are converted from the resistance value of Main VR, Foot VR, or after touch sensor.
In accordance with the voltage level, this block vary the amplitude of the sound.

15. MUSIC LSIs ACCESSES

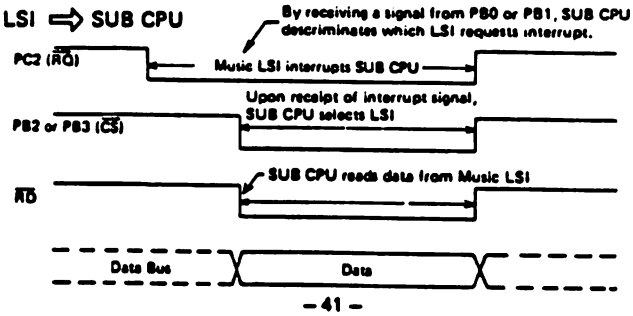
CZ-1 employs two Music LSIs, Master LSI and Slave LSI, which are controlled by SUB CPU.



(1) SUB CPU ⇨ Music LSI



(2) Music LSI ⇨ SUB CPU

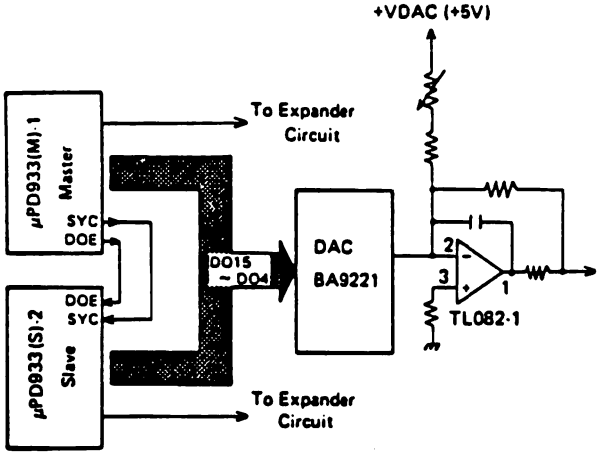


16. PIN FUNCTION OF MUSIC LSI (μPD933AC)

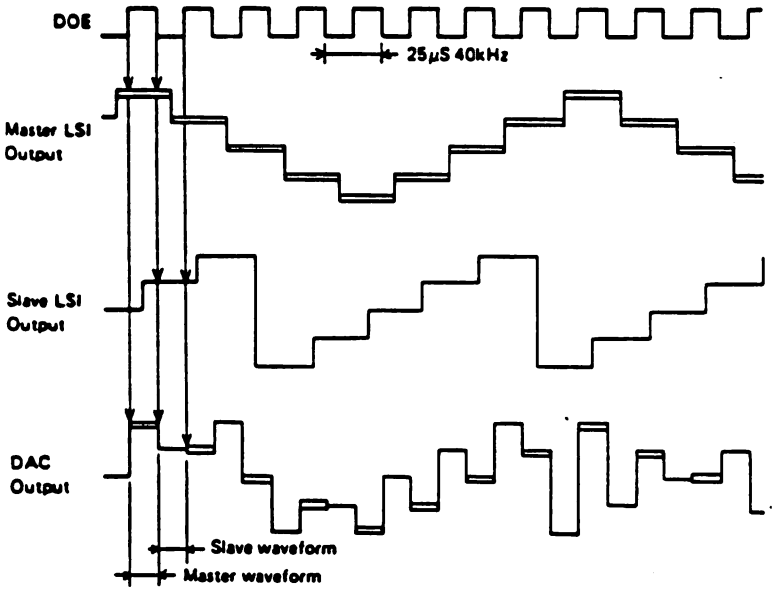
Pin No.	Terminal Name	In/Out	Function
1	$\overline{WE}$	In	Write enable terminal. At LOW, the LSI receives data from SUB CPU.
2	$\overline{WS}$	In	Write strobe terminal. SUB CPU writes data into Music LSI at the rising edge of the signal.
3	$\overline{RQ}$	Out	Request signal terminal. At LOW.
4	$\overline{ID}$	In	Interrupt disenable terminal. At LOW, the LSI receives interrupt mask signal.
6	M/$\overline{S}$	In	Master or Slave determination terminal. When LOW, the LSI becomes Slave LSI while it becomes Master LSI when the terminal is HIGH.
7	SYC	In/Out	Synchronous signal input/output terminal. The synchronous signal is sent from Master LSI to Slave LSI.
8	CLK	In	4.48 MHz clock pulse input.
10	GND		Ground (0V) source.
11	RST	In	Reset signal input. Normally the terminal stays LOW. At power ON, the terminal rises to HIGH level for a while and the internal circuits of the LSI are initialized.
12	DOE	In/Out	Data output enable terminal. At HIGH, digital sound signals are output from Master LSI while Slave LSI outputs sound signal at LOW level.
13	SH	Out	40 KHz sampling signal for Sample & Hold circuit.
15~17	DO1 ~ DO3	Out	Control signals for Expander circuit.
18~29	DO4 ~ DO15	Out	12-bit digital sound signals.
30	VDD		+5V power source.
31~38	DB7 ~ DB0	In/Out	8-bit data bus between Music LSIs and SUB CPU.
39	$\overline{CS}$	In	Chip select terminal. At LOW, the LSI is designated by SUB CPU.
40	$\overline{RD}$	In	Read data terminal. At LOW, the LSI sends data to SUB CPU.

17. DAC (Digital to Analog Converter) CIRCUIT

The two Music LSIs output different waveforms. When signal DOE is HIGH, Master LSI outputs a waveform while Slave LSI outputs a waveform at LOW level of DOE.

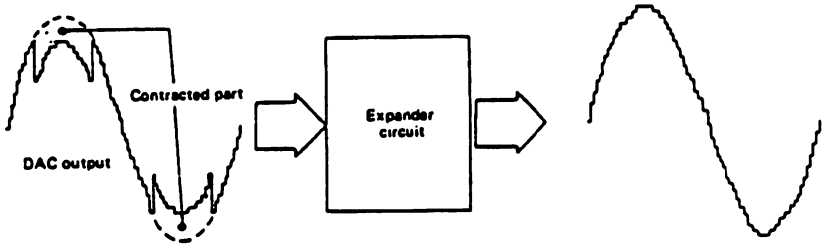


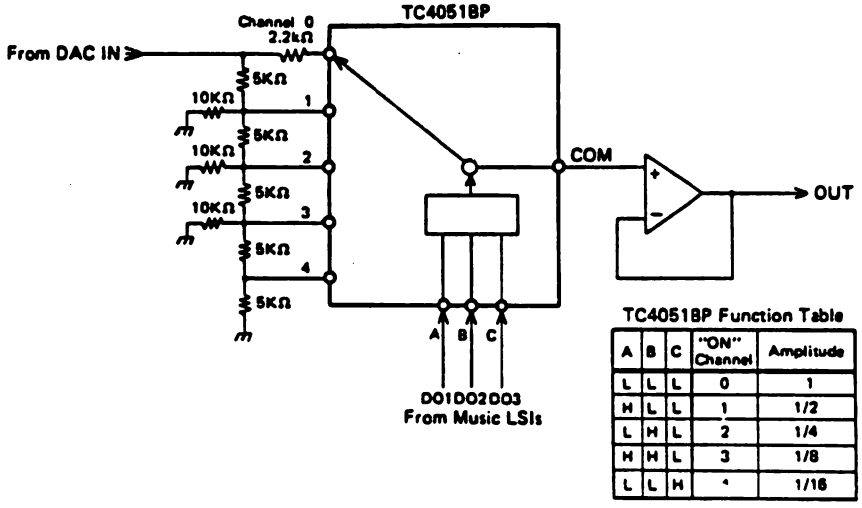
Note: **As the following figure is an illustration for a principle of the time sharing, the actual waveforms differ.**
Master/Slave LSI are digital signals, not analog ones.



18. EXPANDER CIRCUIT

In order to extend the dynamic range of the melody signal, a part of DAC output waveform is contracted and expanded by Expander Circuit.



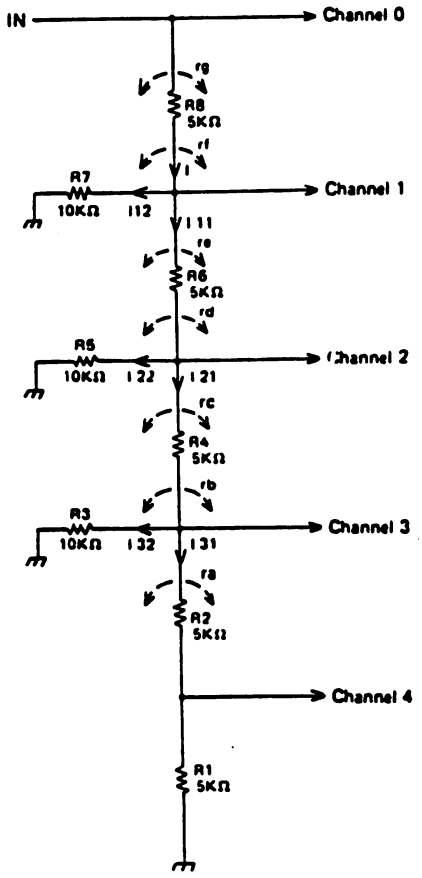


TC40518P Function Table

A	B	C	"ON" Channel	Amplitude
L	L	L	0	1
H	L	L	1	1/2
L	H	L	2	1/4
H	H	L	3	1/8
L	L	H	*	1/16

In accordance with the voltage levels of the signals DO1, DO2 and DO3, one of the input channels is turned on.

By the resistors connected to each channel, the amplitude of DAC output varies from 1 to 1/16.



Combined resistances at each point are:

ra = R1 (5KΩ) + R2 (5KΩ) = 10KΩ
rb = Parallel connected ra (10KΩ) and R3 (10KΩ) = 5KΩ
rc = rb (5KΩ) + R4 (5KΩ) = 10KΩ
rd = Parallel connected rc (10KΩ) and R5 (10KΩ) = 5KΩ
re = rd (5KΩ) + R6 (5KΩ) = 10KΩ
rf = Parallel connected re (10KΩ) and R7 (10KΩ) = 5KΩ
rg = rf (5KΩ) + R8 (5KΩ) = 10KΩ

Each current value is:

I = I11 + I12
I11 = I21 + I22
I21 = I31 + I32

Namely, I11 = I/2
I21 = I11/2 = I/4
I31 = I21/2 = I/8

Voltage level at each channel is:

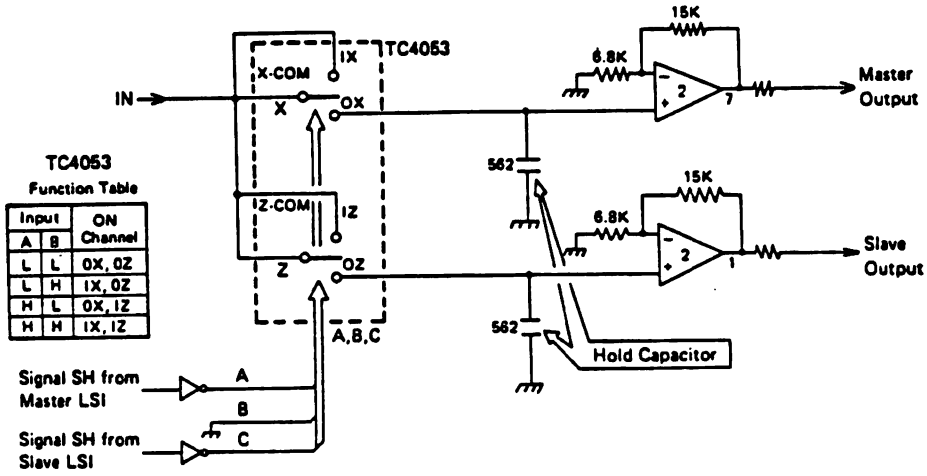
Channel 0: rg x I = 10KΩ x I
Channel 1: re x I11 = 10KΩ x I/2
Channel 2: rc x I21 = 10KΩ x I/4
Channel 3: ra x I31 = 10KΩ x I/8
Channel 4: R1 x I31 = 5KΩ x I/8 = 10K x I/16

If input voltage is E:

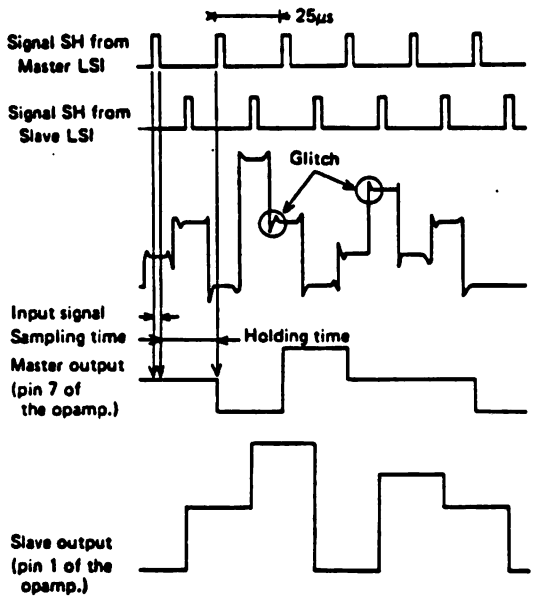
Channel 0 input voltage is E.
Channel 1 input voltage is E/2.
Channel 2 input voltage is E/4.
Channel 3 input voltage is E/8.
Channel 4 input voltage is E/16.

Thus, output of DAC is expanded in accordance with the voltage levels of signals DO1, DO2 and DO3.

19. SAMPLE & HOLD CIRCUIT



The block eliminates a high frequency noise called as "Glitch" which appears at the end of the stepped waveform.



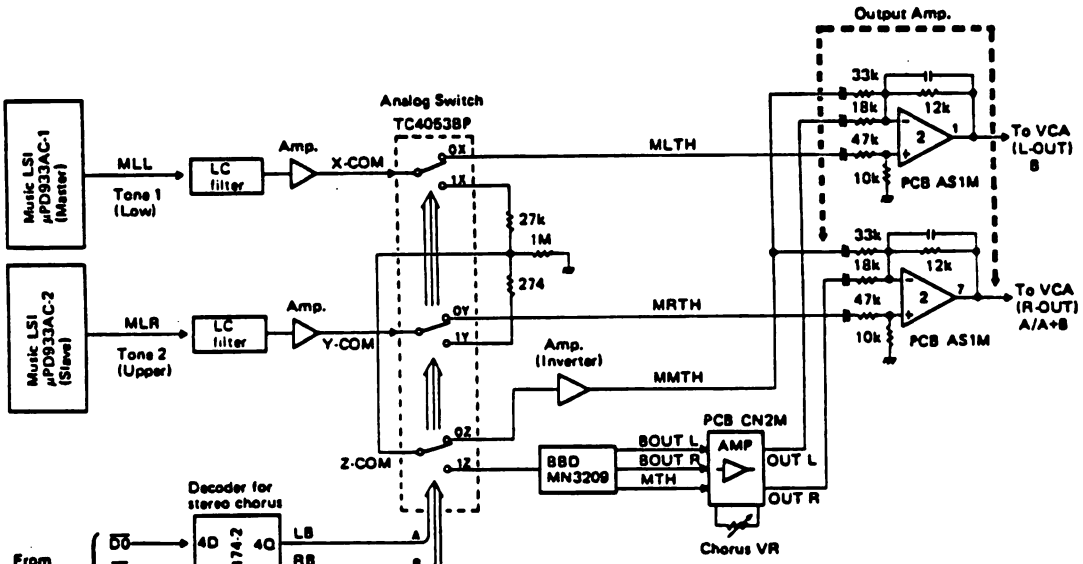
When signal SH from Master LSI is HIGH, the switch X in TC4053 is contacted with the terminal OX. This causes the input signal to pass through. At this time, the voltage level of the waveform is charged in the Hold Capacitor.

On the other hand, while a glitch appears on the waveform, the switch X is contacted with the terminal IX. This results in cutting off the glitch. Although no signal comes out of TC4053, the input of the opamp keeps the same voltage level by discharging of the Hold Capacitor.

Sampling or holding the slave waveform is performed by the same procedures using signal SH from Slave LSI and switch Z.

20. STEREO CHORUS CONTROL CIRCUIT

20-1. Block Diagram



Whether or not passing the tone through the Stereo Chorus circuits are determined panel switch.
The Main CPU controls analog switch TC4053BP to pass only selected tone through Stereo Chorus circuits.

20-2. Signal Function

① MLL, MLR ..... Left (Right) analog melody signal of DAC output.

② MLTH, MRTH ..... Left (Right) analog melody signal of original sound. (Not through Stereo Chorus circuit)

③ MMTH ..... Mixed (L+R) analog melody signal of original sound. (Not through Stereo Chorus circuit)

④ BOUT L, BOUT R ... Left (Right) analog melody signal of Stereo Chorus sound. (Through Stereo Chorus circuit)

⑤ MTH ..... Mixed (L+R) analog melody signal of original sound for Stereo Chorus sound.

⑥ OUT L, OUT R ..... Stereo Chorus sound. (BOUT L (R) + MTH)

20-3. Circuit Function

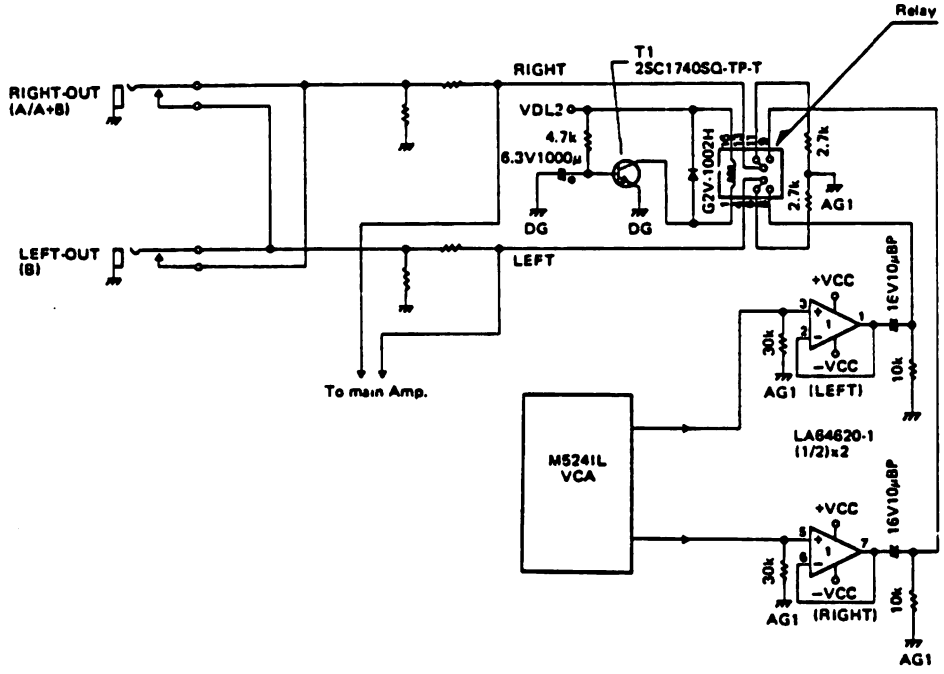
① Decoder for Stereo Chorus .... Generates control signals for the analog switch.
(SN74LS174N-2)

② Analog switch ..... Selects whether or not passing the melody signal through
(TC4053BP) Stereo Chorus circuits.

③ BBD (MN3209) ..... Bucket Brigade Device for Stereo Chorus effect.

④ Output Amp. ..... Mixes the stereo or monaural signals.

20-4. Line-out Circuit



① Stereo sounds are output only when output plugs are connected to both A/A+B and B terminals, while mixed sound is heard when output plug is connected only one terminal.

Note: When output plug is connected at B terminal, mixed sound B/A+B is also output.

② The relay eliminates a shock noise at power ON/OFF. Voltage level VDL2 is controlled by signal LDC from terminal PB6 of Sub CPU. (Refer to page 19)

The following table shows combinations of the analog switch and the LINE-OUT terminal output in each mode.

MODE	Stereo Chorus ON/OFF	LINE-OUT terminal output		Stereo Chorus VR O: Effective X: No effective	Analog switch TC4053						Melody signal output			O: Output X: No output
		A/A+B (OUT-R)	B (OUT-L)		Input			Output			MRTH	MLTH	MMTH	MTH, B OUT {L R}
					C	B	A	X	Y	Z				
NORMAL	ON	OUT L + OUT R	OUT L + OUT R	O	H	H	H	1	1	1	X	X	X	O
	OFF	MMTH	MMTH	X	L	H	H	1	1	0	X	X	O	X
TONE MIX	TONE 1: ON TONE 2: ON	OUT L + OUT R	OUT L + OUT R	TONE 1: O TONE 2: O	H	H	H	1	1	1	X	X	X	O
	TONE 1: ON TONE 2: OFF	OUT R + MRTH	OUT L	TONE 1: O TONE 2: X	H	L	H	1	0	1	O	X	X	O
	TONE 1: OFF TONE 2: ON	OUT R	OUT L + MLTH	TONE 1: X TONE 2: O	H	H	L	0	1	1	X	O	X	O
	TONE 1: OFF TONE 2: OFF	MRTH	MLTH	TONE 1: X TONE 2: X	L	L	L	0	0	0	O	O	X	X
KEY SPRIT	UPPER : ON LOWER: ON	OUT L + OUT R	OUT L + OUT R	UPPER : O LOWER O	H	H	H	1	1	1	X	X	X	O
	UPPER: ON LOWER: OFF	OUT R	OUT L + MLTH	UPPER : O LOWER: X	H	H	L	0	1	1	X	O	X	O
	UPPER : OFF LOWER: ON	OUT R + MLTH	OUT L	UPPER : X LOWER: O	H	L	H	1	0	1	O	X	X	O
	UPPER : OFF LOWER: OFF	MLTH	MRTH	UPPER : X LOWER: X	L	L	L	0	0	0	O	O	X	X

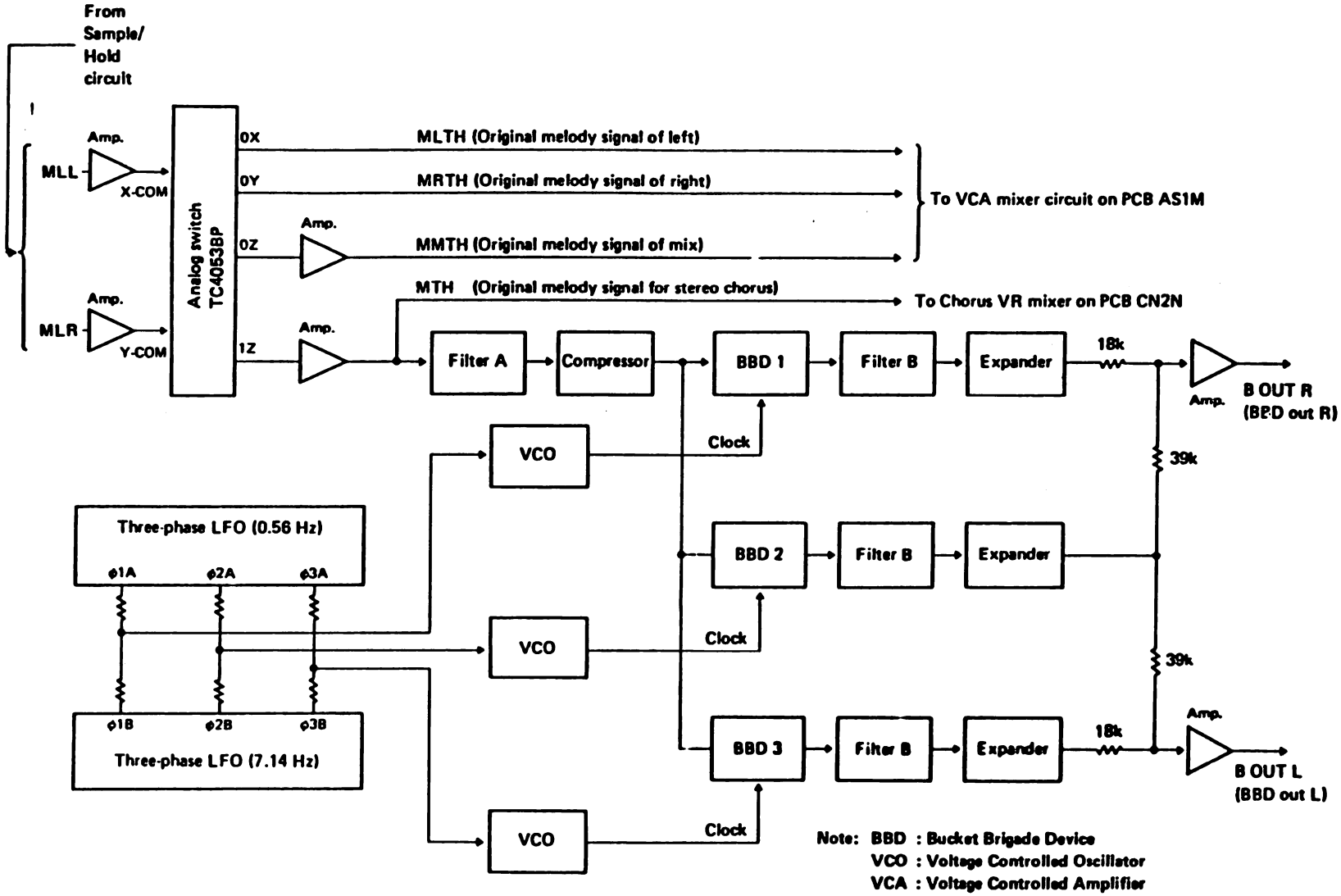
Note: ① When connecting both A/A+B and B output of LINE-OUT terminal.

②

Line-out \ Mode	Normal	Tone mix	Key sprit
A/A+B	R-OUT (Output of Music LSI (Master))	Tone 2	Upper
B	L-OUT (Output of Music LSI (Slave))	Tone 1	Lower

21. Stereo Chorus Circuit

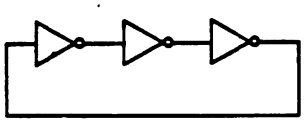
21.1. BLOCK DIAGRAM



21-2. Function of Each Block

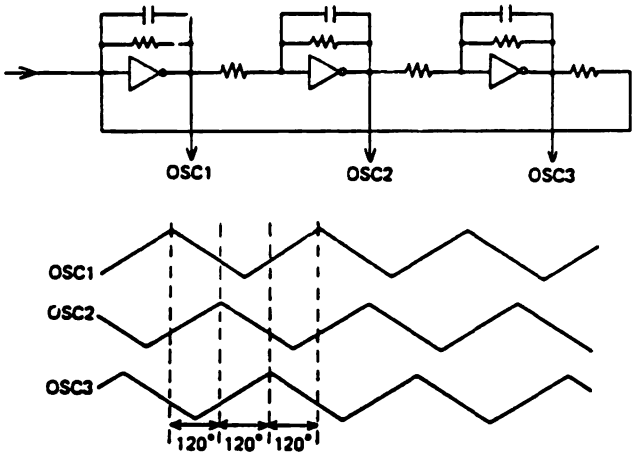
Analog switch (TC4053BP)	–	Determines whether or not passing melody signal through Stereo Chorus circuits. (Controlled by CPU)
Filter A	–	As the BBD does not pass signals which exceed 20KHz, this block is a low-pass filter whose cutoff frequency is 20KHz.
Compressor	–	In accordance with input signal level, this block controls the amplitude. When the input signal is small, the circuit amplifies the signal whereas the amplitude becomes smaller when the input is a large-level waveform. The block is used for reducing the noise.
Three-Phase LFOs	–	Generates low-frequency triangle signals of 0.56Hz and 7.14Hz. The three outputs differ 120 degrees in phase.
VCOs	–	Voltage Controlled Oscillator which generates the clock pulses for the BBDs. Their oscillation frequencies vary in accordance with the input voltage level.
BBDs	–	Bucket Brigade Device. Stereo chorus effect is given by delaying the right or the left sound.
Filter B	–	Since the output signal of the BBD carries a noise caused by clock pulses, the filter removes the noise.
Expander	–	Functions contrary to the Compressor. This circuit is also used for reducing the noise.

21-3. Three-Phase LFO (Low Frequency Oscillator)

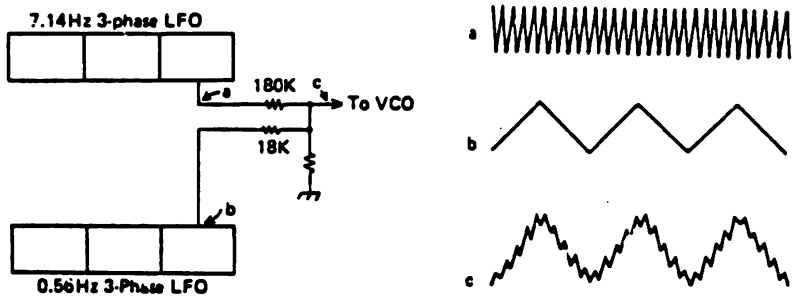


The left figure shows three inverters serially connected.
If LOW level input enters the circuit, the output becomes HIGH level. Because of the transfer characteristic of the inverter, the inverted input voltage appears on the output with a time lag.
Hence, the circuit oscilates and the oscillation frequency is determined by the time lag.

The following shows the actual circuit of the Three-Phase LFO. The time lag is controlled by the parallel connected capacitor and the resistors.
Model CZ-1 employs two LFOs whose oscillation frequencies are 0.56 Hz and 7.14 Hz.
The output differs 120 degrees in phase.

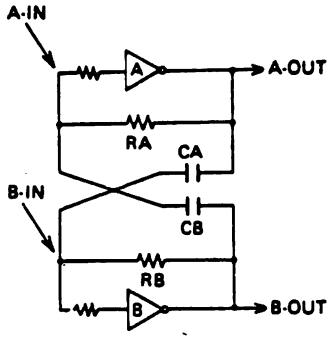


Both 0.56 Hz and 7.14 Hz triangle waveforms are mixed to give variational delays of the sound in the BBD.



The 0.56 Hz and 7.14 Hz waveforms are mixed in the ratio of 10:1 as they pass through 18Kohm and 180Kohm resistors, respectively.

21-4. VCO (Voltage Controlled Oscillator)

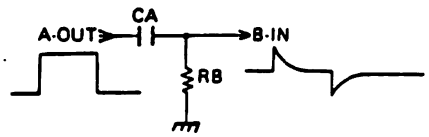


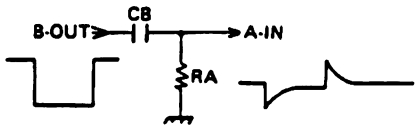
The VCO is an oscillator whose oscillation frequency varies in accordance with the input voltage level.

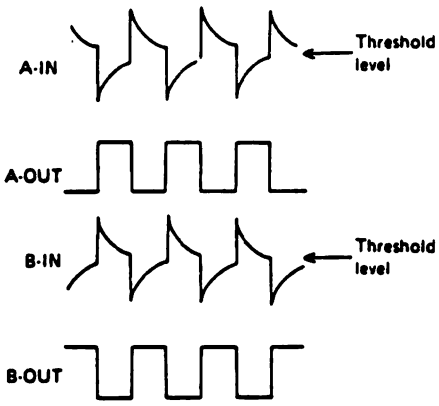
In the left figure, the voltage levels of the A-OUT and the B-OUT are opposite.

(1) When A-OUT is HIGH, B-OUT drops to LOW.

(2) From A-OUT, electric current flows into B-IN via a differentiation circuit.
As a result, the voltage of B-IN drops gradually while the A-IN voltage gradually rises.



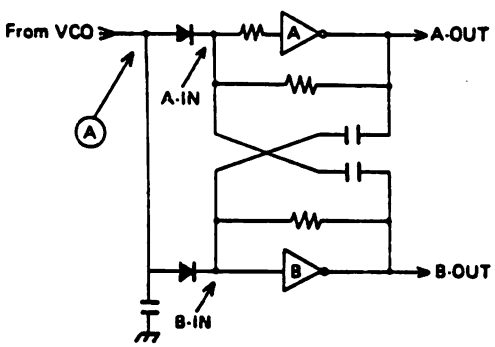


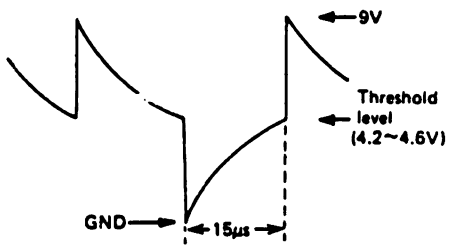


(3) When B-IN becomes lower than the threshold level, B-OUT rises to HIGH.
When A-IN becomes higher than the threshold level, A-OUT drops to LOW.

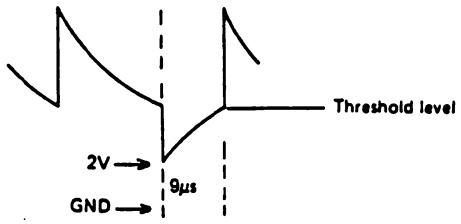
(4) The circuit oscillates repeating the above operations.

The following shows the actual circuit of VCO. When control terminal (A) is GND (zero volt), it takes approximately 15 microseconds for the differentiation circuit to reach the threshold voltage.



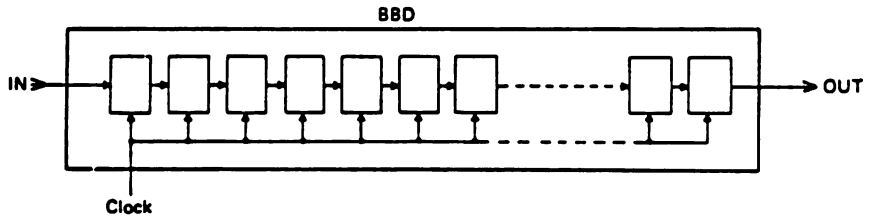


When the voltage of Ⓐ is 2 volts, it takes only 9 microseconds to reach the threshold level.

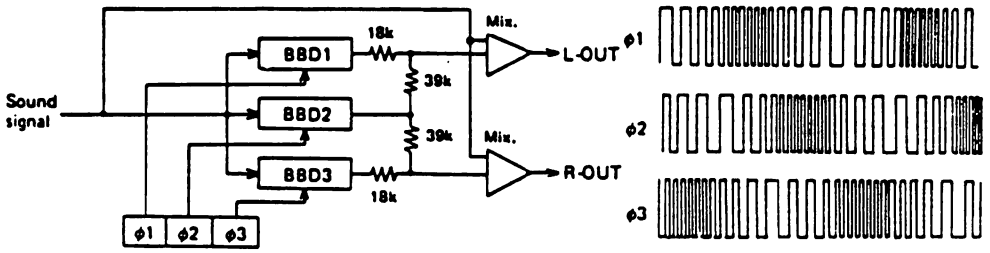


As VCO receives a triangle waveform from the Three-Phase LFO, it oscillates from 55.6 KHz to 33.3 KHz in accordance with the voltage level of LFO output.

21-5. BBD (Bucket Brigade Device)



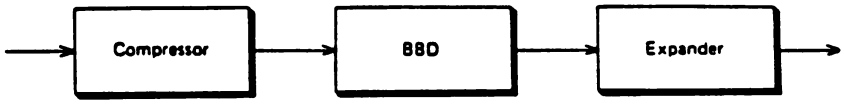
The BBD contains serial-connected delay elements. The input signal is shifted one step per one clock pulse.
The clock pulse is generated in the VCO, and as it varies from 33.3 KHz to 55.6 KHz, the delay time varies.



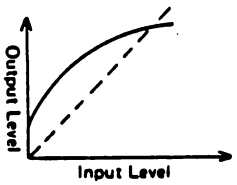
Model CZ-1 employs three BBDs in order to give better stereo effect.

21-6. Compressor and Expander Circuits

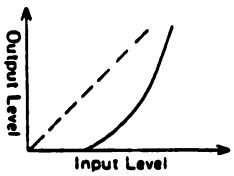
If a sound signal passes through the BBD, a noise is carried on the signal especially when the input level of the signal is low.



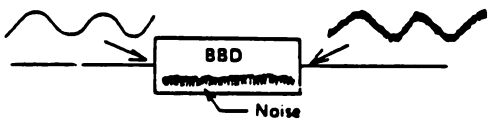
Compressor ..... When the level of input signal is low, the amplitude is large. If the input level is high, the amplitude decreases.



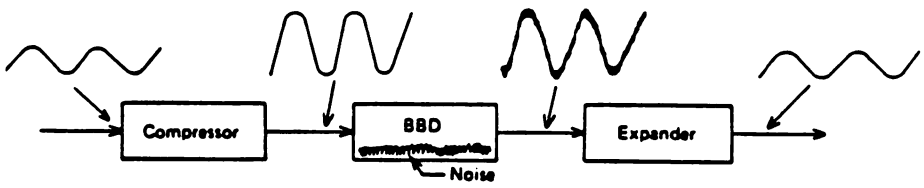
Expander ..... When the level of input signla is low, the amplitude is small. The amplitude increases when the input level is high.



When a low signal does not pass through the Compressor and the Expander;

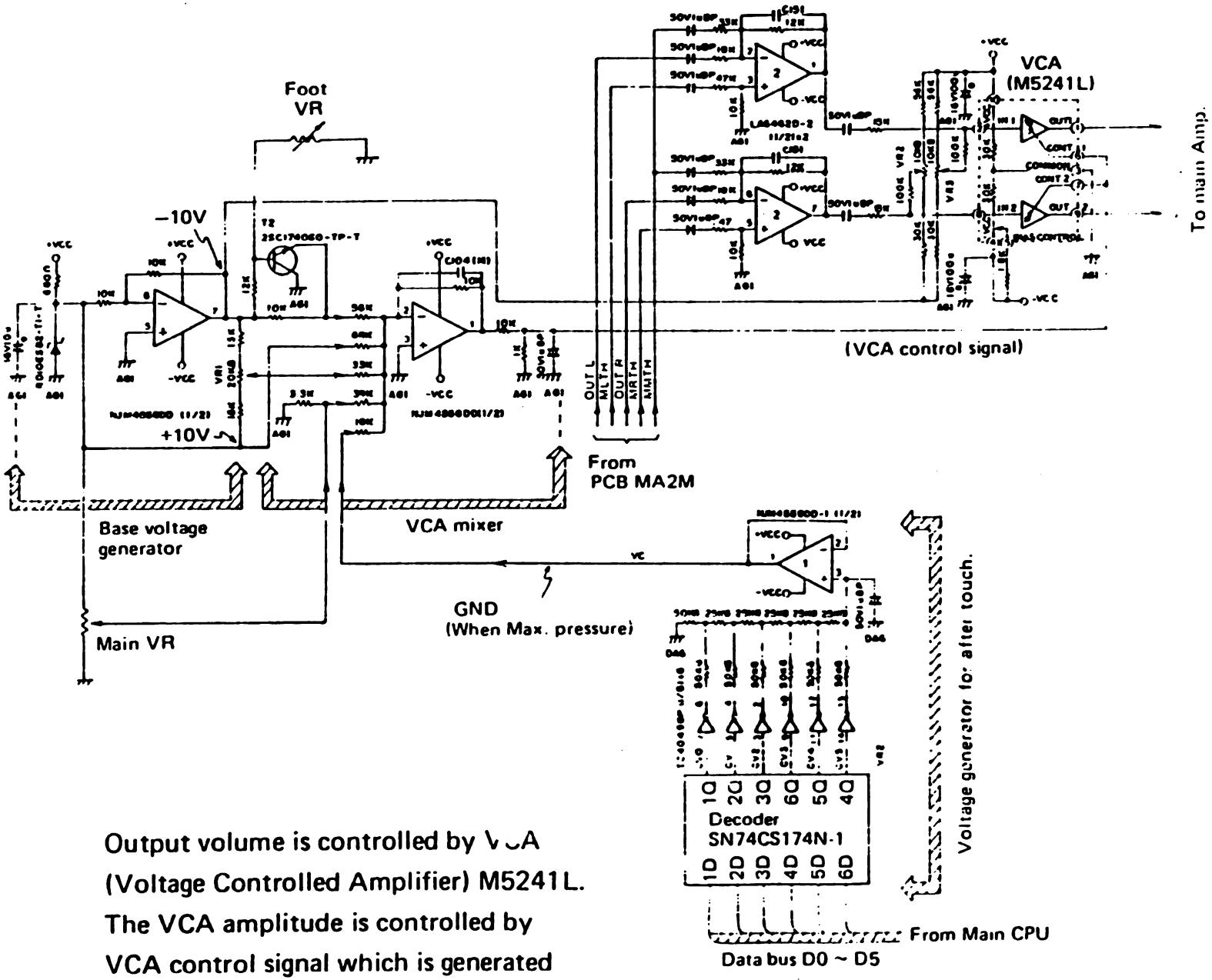


When a low signal passes through the Compressor and the Expander;

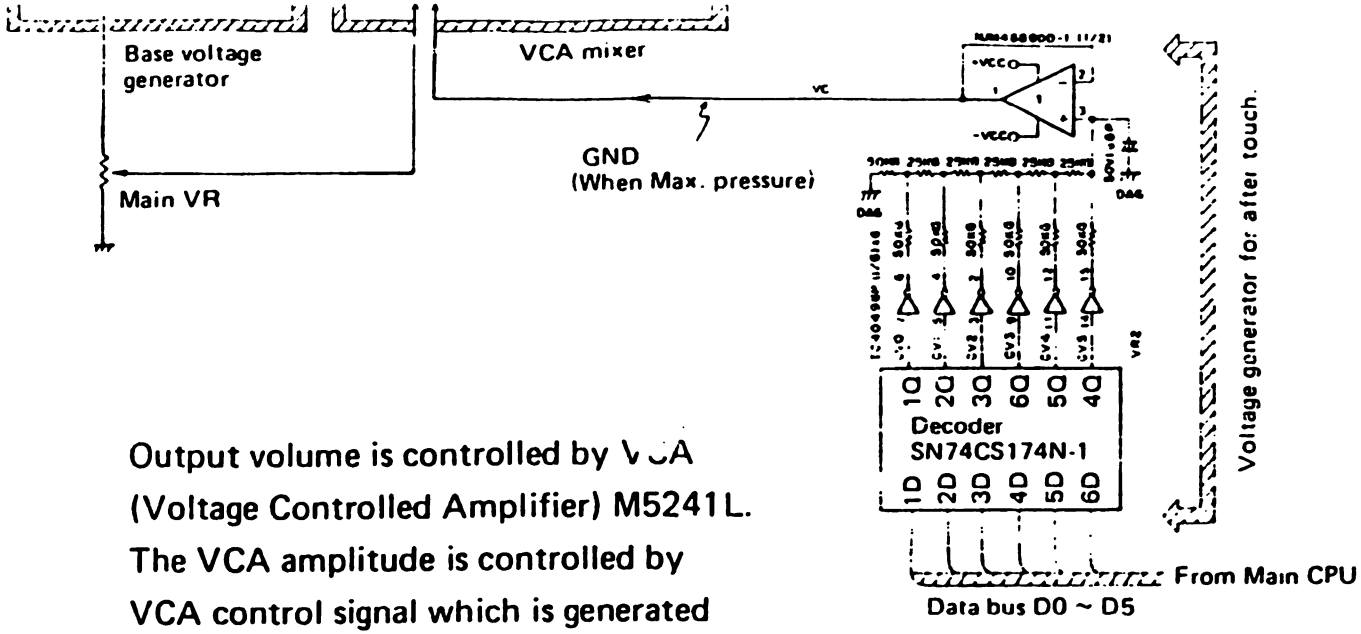


Thus, the S/N ratio of the circuit is heightened.

22. OUTPUT VOLUME CONTROL CIRCUIT



Output volume is controlled by VCA (Voltage Controlled Amplifier) M5241L. The VCA amplitude is controlled by VCA control signal which is generated by VCA mixer.

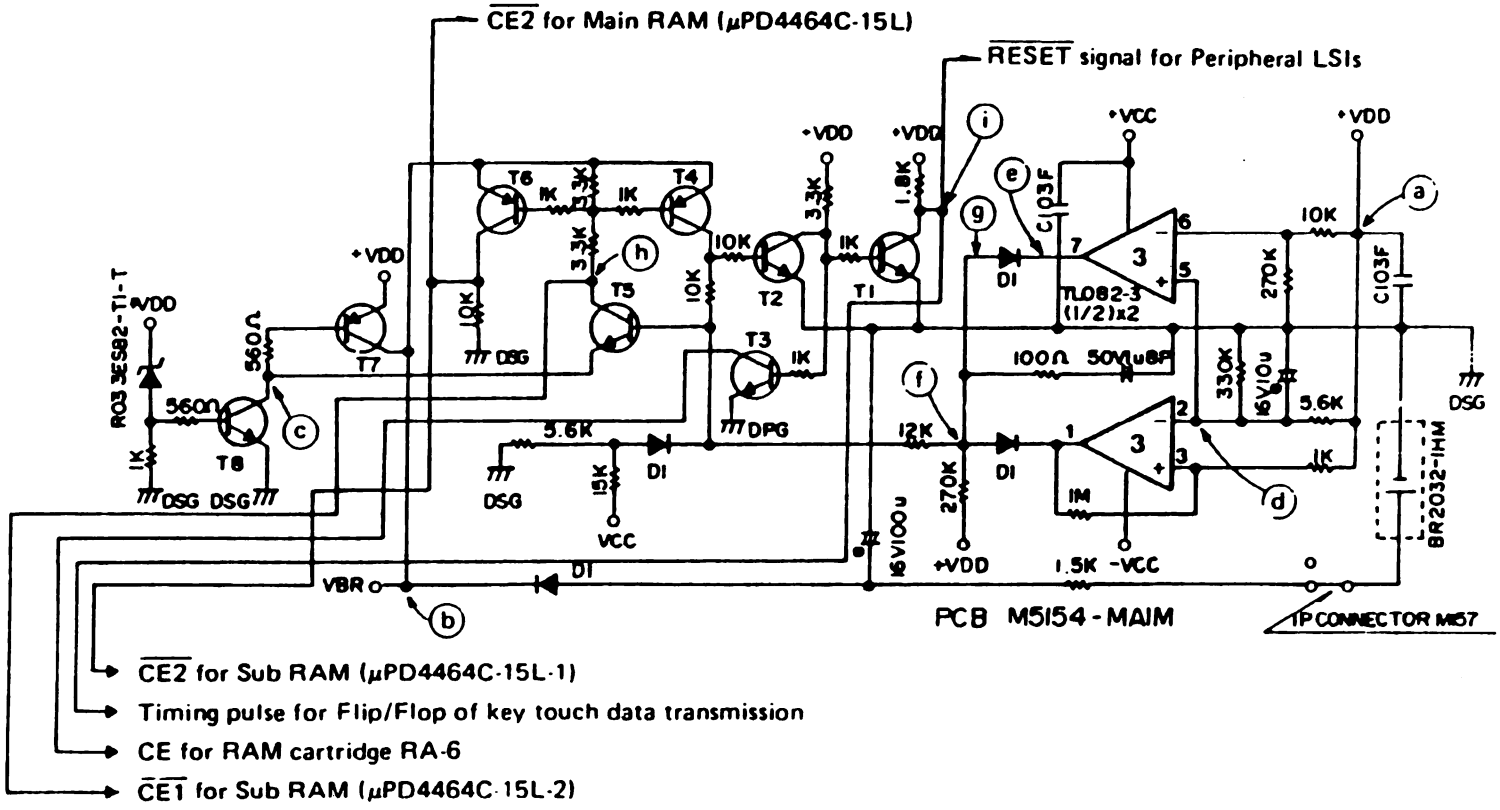


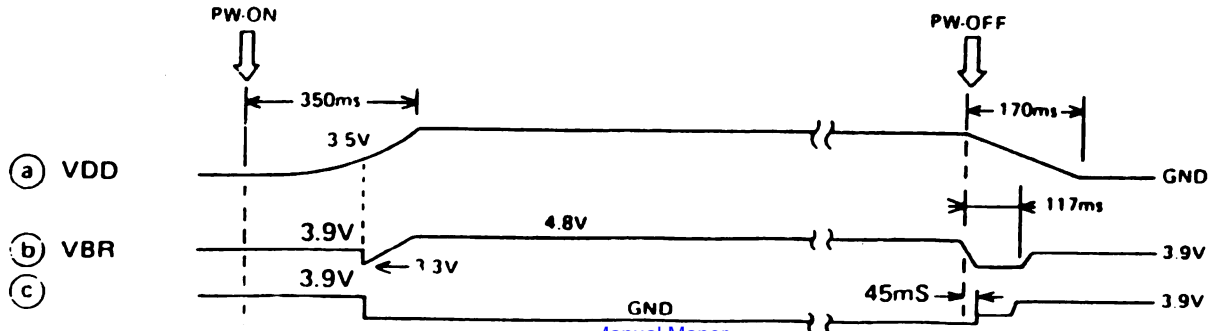
Output volume is controlled by VCA (Voltage Controlled Amplifier) M5241L.
The VCA amplitude is controlled by VCA control signal which is generated by VCA mixer.
The VCA mixer output is controlled by foot VR, main VR, and after touch sensor, and varies its output voltage in negative logic.
Besides, VCA control signal is also varied by Amp. or after touch parameter.

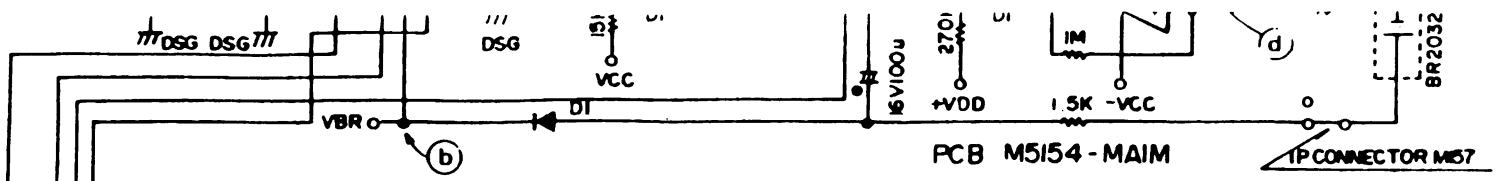
	Main VR	Pressure of after touch sensor	Amp./After touch parameter				
			15	~	8	~	0
VCA control signal	Min.	No pressure	–4.6V	~	–3.6V	~	–2.5V
	Max.	No pressure	–2.0V	~	–1.0V	~	+0.2V
	Max.	Max. pressure	+0.2V	~	+0.2V	~	+0.2V

23. RESET CIRCUIT

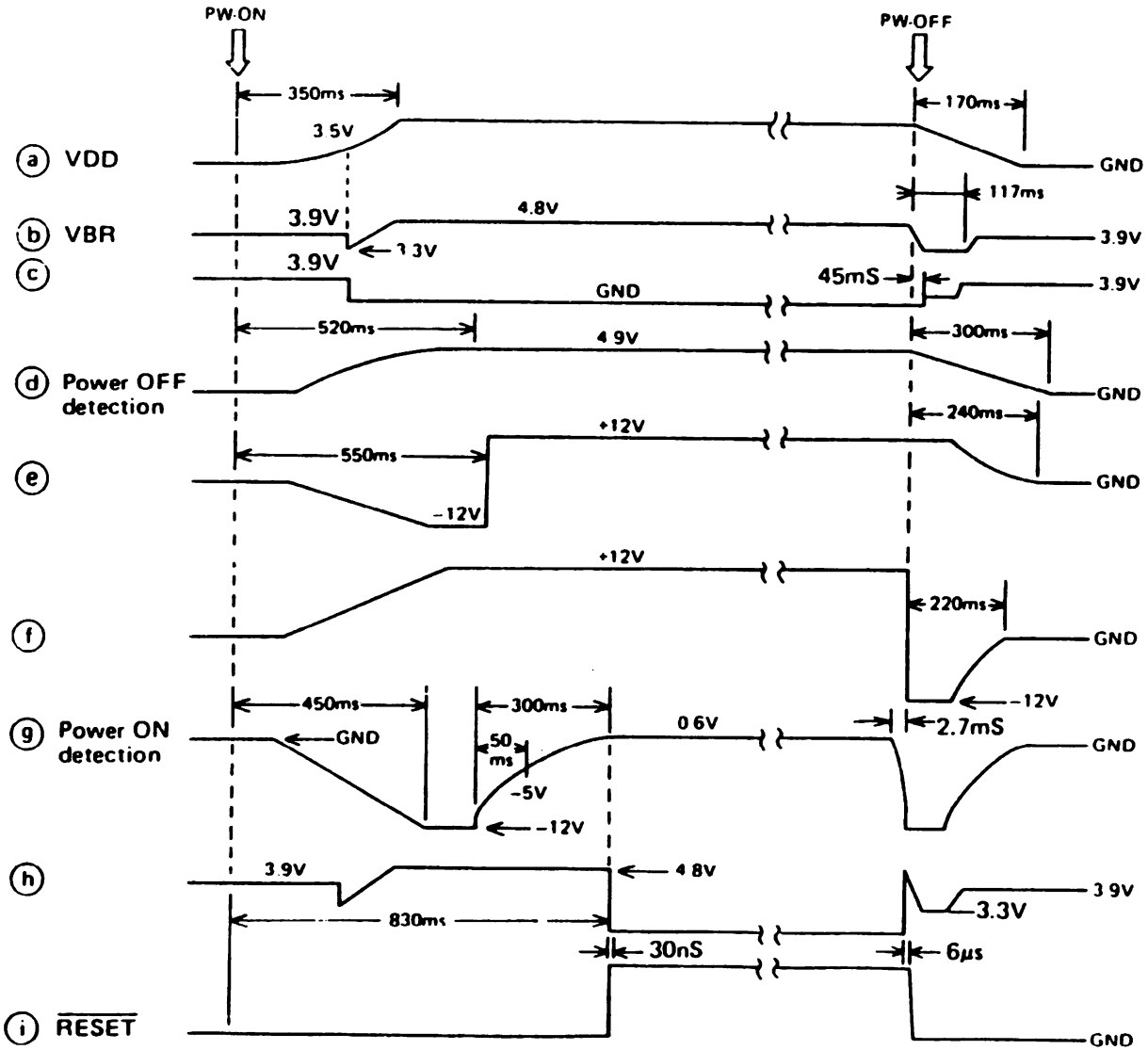
The following circuit is Reset (power fail detection) circuit which generates power ON/OFF reset pulse for peripheral LSIs (CPUs, Music LSIs, Key interface LSI, and Key touch control LSI), to protect recorded data in the RAM's.





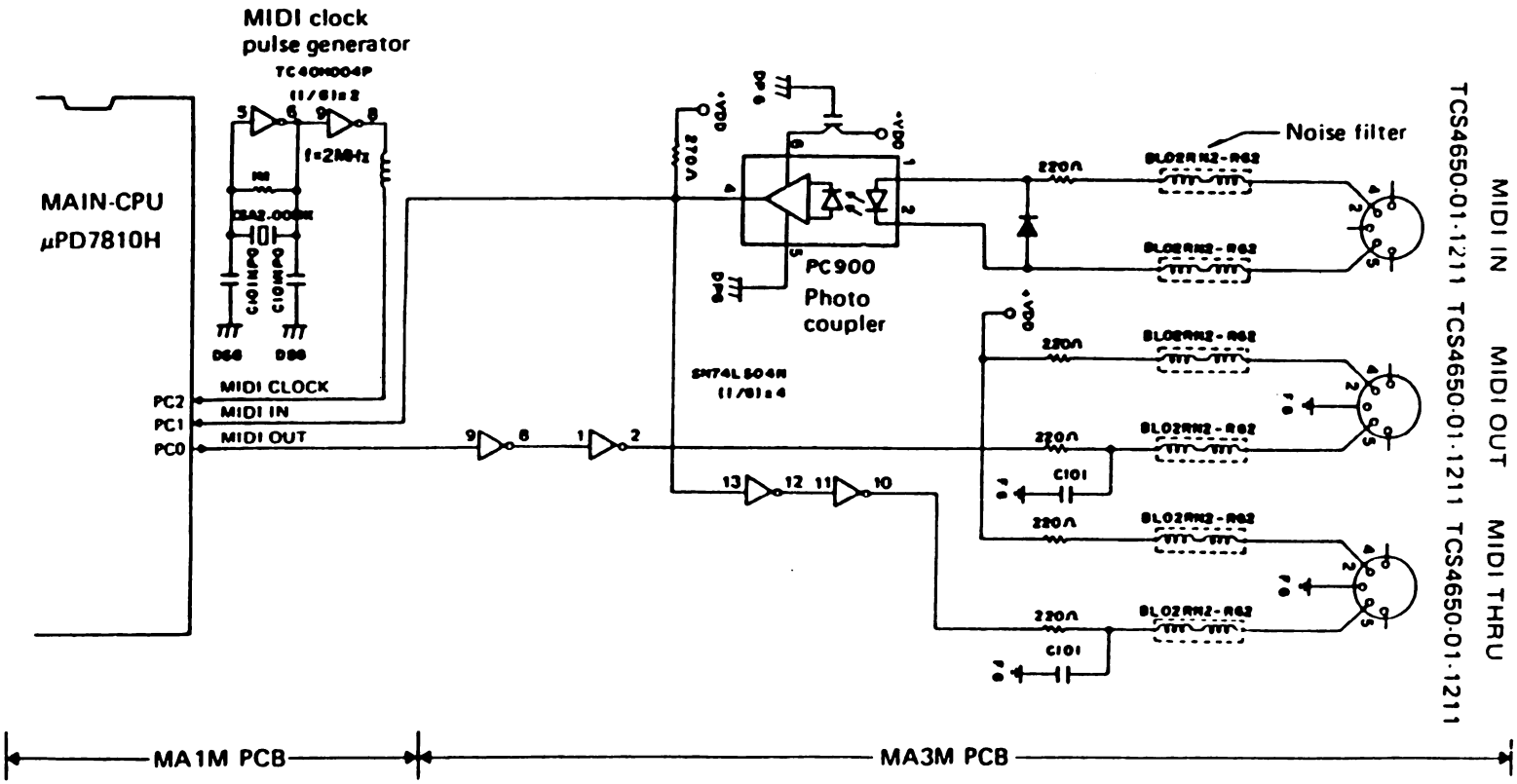


- $\overline{CE2}$ for Sub RAM (μPD4464C-15L-1)
- Timing pulse for Flip/Flop of key touch data transmission
- CE for RAM cartridge RA-6
- $\overline{CE1}$ for Sub RAM (μPD4464C-15L-2)

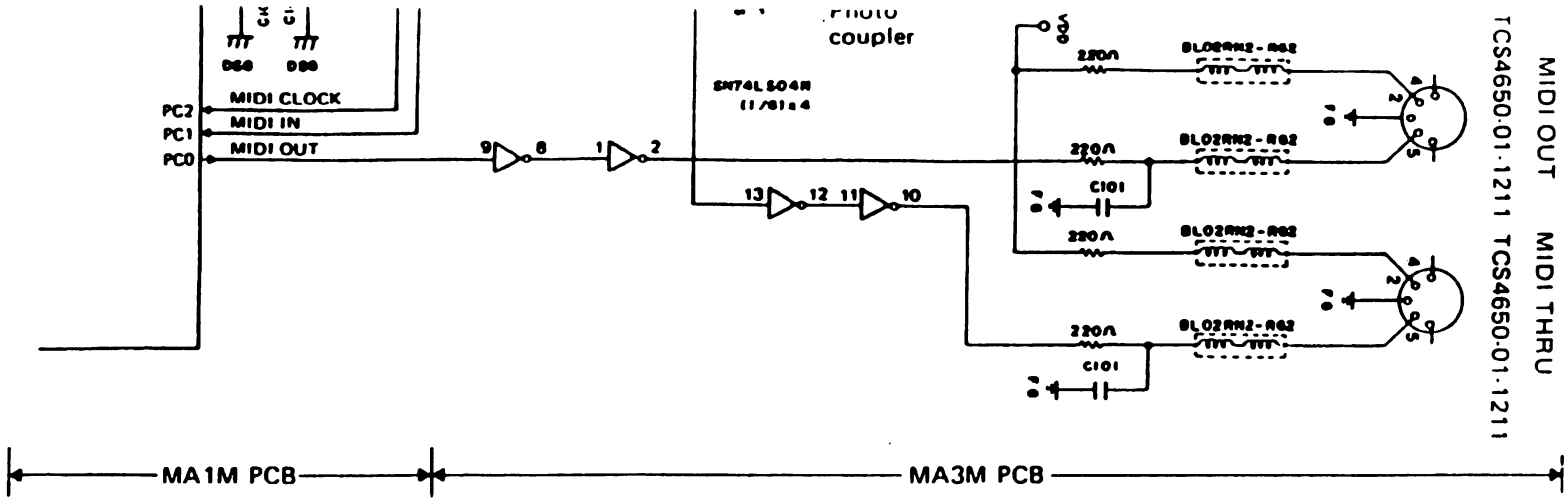


24. MIDI INTERFACE CIRCUIT

MIDI (Musical Instrument Digital Interface) is an international standard for external control of electronic musical instruments. In other words, standardized input and output terminals are equipped with musical instruments, rhythm machines, sequencers, etc. and music information which the machines send and receive via these terminals is made compatible by certain formatting. This standard enables a musical instrument to connect, synchronize, and sequence (memorize) to other models and even to other makes.



Serial data informations from other instruments comes in from MIDI-IN terminal and enters MAIN CPU's PC1 terminal via photo coupler PC900.



Serial data informations from other instruments comes in from MIDI-IN terminal and enters MAIN CPU's PC1 terminal via photo coupler PC900.

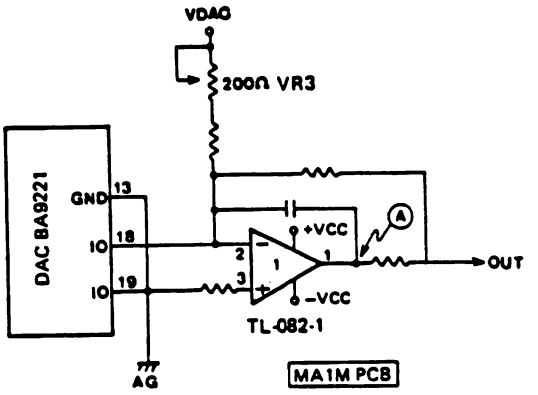
Thus, CZ-1 is not electrically connected with any external instruments to cut electric noises.

Input signal also goes out MIDI THRU terminal through a photo coupler and two inverters.

MAIN CPU transmits MIDI data from PC0 terminal.

25. ADJUSTMENT

25-1. DAC Offset Voltage Adjustment

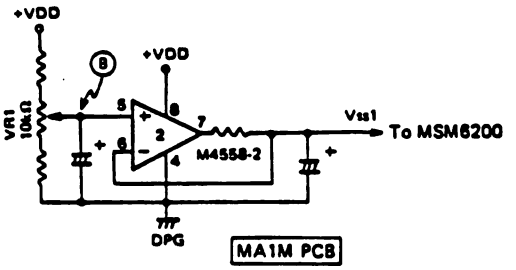


(1) Connect a digital voltmeter between pin 13 of DAC BA9221 and pin 1 of opamp TL082-1.
(Refer to check point Ⓐ on page 11)

(2) While the test unit is not producing any sound, adjust VR3 so that the digital voltmeter reading is −3 ± 3mV.

Note: Be sure to use a digital voltmeter.

25-2. VSS1 Voltage Adjustment (Power Source for MSM6200)



(1) Measure VDD (+5V) accurately.

(2) Connect a digital voltmeter between pin 5 of opamp M4558-2 and ground DPG.
(Refer to check point Ⓑ on page 11)

(3) Adjust VR1 so that Vss1 is 2.25 ± 0.05V.

Note: Be sure to use a digital voltmeter.

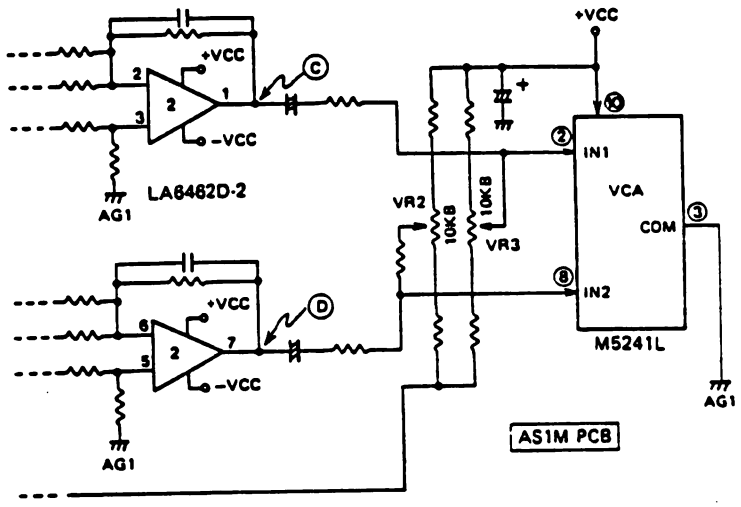
25-3. LCD Brightness Adjustment

Turn the VR2 on PCB MA1M all the way counter clockwise.

25-4. After Touch Adjustment

Turn the VR4 on PCB MA1M all the way clockwise.

25-5. VCA Offset Voltage Adjustment



(1) Connect a digital voltmeter as indicated in the following table.
(Refer to checkpoing Ⓒ and Ⓓ on page 4)

Connection point	VR to be adjusted
Pin 1 of opamp and pin ③ of VCA (GND)	VR2
Pin 7 of opamp and pin ③ of VCA (GND)	VR3

(2) While the test unit is not producing any sound, adjust VR2 and VR3 so that digital voltmeter reading is 0±3mV.

Note: Be sure to use a digital voltmeter.

25-6. BBD Adjustment

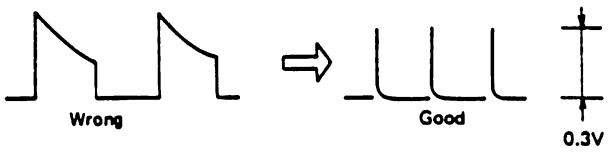
(1) Connect an oscilloscope as shown in the table below.
(Refer to checkpoint Ⓔ, Ⓕ and Ⓖ on page 12)

Connection point (MA2M PCB)	Adjustment VR
Center terminal of VR1 and pin 1 of BBD MN3209-1 (GND)	VR1
Center terminal of VR2 and pin 1 of BBD MN3209-2 (GND)	VR2
Center terminal of VR3 and pin 1 of BBD MN3209-3 (GND)	VR3

MA2M PCB

(2) Set the oscilloscope on AC range, 0.1V/div, and 10μS/div, then observe the waveforms.

(3) Adjust each VR for the minimum width of the waveform.



25-7. Volume Adjustment

(1) Keep pressing "INITIALIZE" button, depress "DC01 WAVEFORM", "DC01 ENVELOPE", "DCW1 KEY FOLLOW", "DCW1 ENVELOPE", "DCA1 KEY FOLLOW", "DCA1 ENVELOPE", "DETUNE", and "OCTAVE" buttons on "NORMAL" mode.

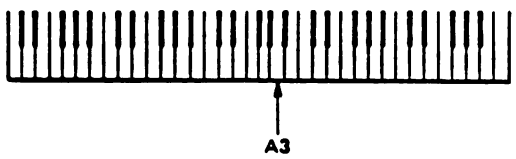
(2) Depress "DCW1 ENVELOPE" and then "END" buttons.

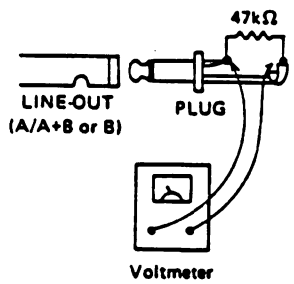
(3) Choose 1+1' by "LINE SELECT" button.

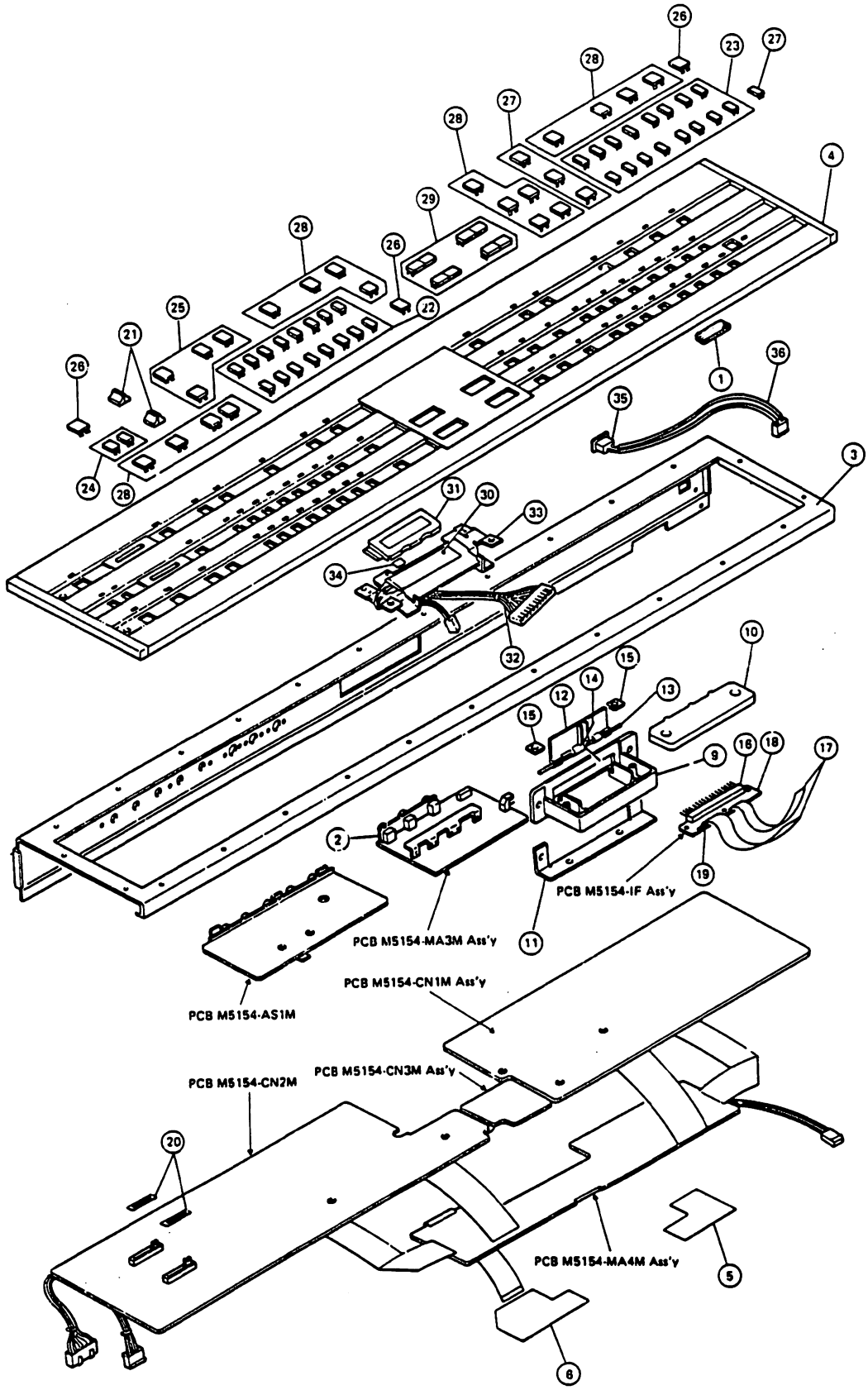
(4) Set the volume control to its maximum and the stereo chorus volume to its minimum.

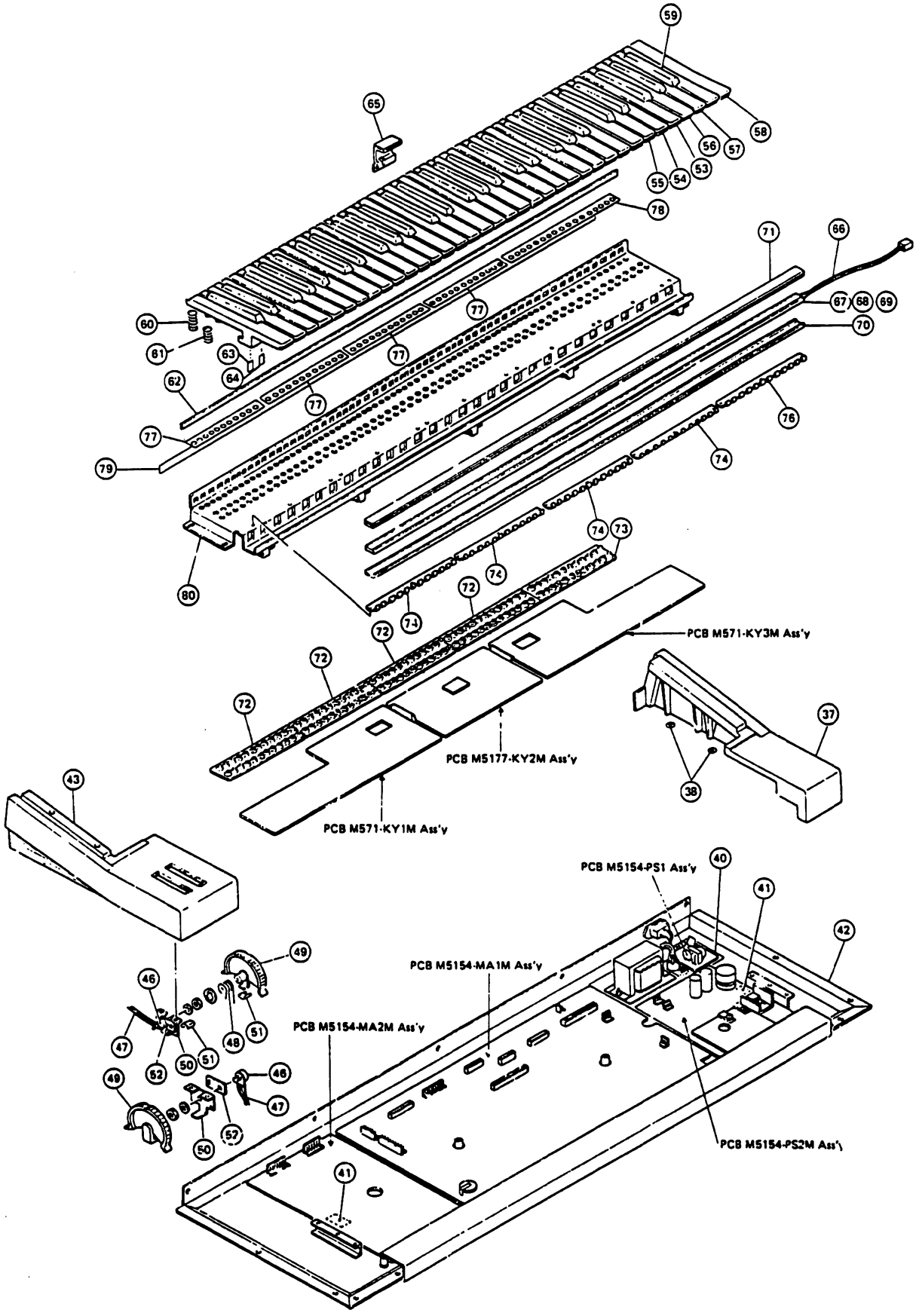
(5) Connect a digital voltmeter and a register of 47KΩ between the ground and LINE-OUT terminal (either A/A+B or B output).

(6) Depressing the key A3, adjust 50K VR on the PCB M5153-AS1M so that the voltmeter reading is 340mV ± 20mV.






PCB M5154-IF Ass'y
PCB M5154-MA3M Ass'y
PCB M5154-CN1M Ass'y
PCB M5154-AS1M
PCB M5154-CN3M Ass'y
PCB M5154-CN2M
PCB M5154-MA4M Ass'y


PCB M571-KY3M Ass'y
PCB M5177-KY2M Ass'y
PCB M571-KY1M Ass'y
PCB M5154-PS1 Ass'y
PCB M5154-MA1M Ass'y
PCB M5154-MA2M Ass'y
PCB M5154-PS2M Ass'y