

# SILICON PLANAR EPITAXIAL N-P-N TRANSISTOR

# BF195

## TENTATIVE DATA

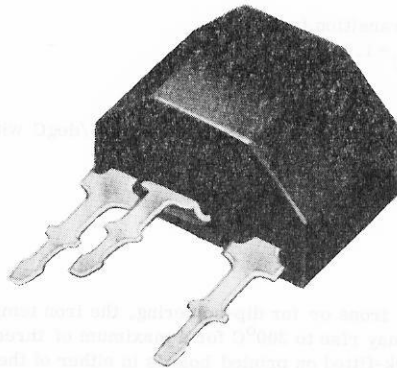
N-P-N low noise transistor in epoxy resin encapsulation with three rigid self-locking strips suitable for insertion into printed circuit boards using standard grids. The transistor is recommended for use in the input stages of a.m./f.m. receivers, also for use in mixer and i.f. stages of a.m. battery operated receivers.

### QUICK REFERENCE DATA

$V_{CBO}$ max.	30	V
$V_{CEO}$ max.	20	V
$I_C$ max.	30	mA
$P_{tot}$ max.	220	mW
$T_j$ max.	125	$^{\circ}C$
$h_{FE}$ typ. ( $I_C = 1.0\text{mA}$ , $V_{CE} = 10\text{V}$ )	67	
$f_T$ typ. ( $I_C = 1.0\text{mA}$ , $V_{CE} = 10\text{V}$ )	200	MHz
N typ. ( $I_C = 1.0\text{mA}$ , $V_{CE} = 10\text{V}$ , $g_s = 20\text{mmho}$ , $f = 1.0\text{MHz}$ )	3.5	dB
( $I_C = 1.0\text{mA}$ , $V_{CE} = 10\text{V}$ , $g_s = 10\text{mmho}$ , $f = 100\text{MHz}$ )	4.0	dB

### OUTLINE AND DIMENSIONS

For details see page 4



## RATINGS

Limiting values of operation according to the absolute maximum system.

### Electrical

$V_{CBO}$ max. ( $I_E = 0$ )	30	V
$V_{CEO}$ max. ( $I_B = 0$ , see curve on page 7)	20	V
$V_{EBO}$ max. ( $I_C = 0$ )	5.0	V
$I_C$ max.	30	mA
$I_{CM}$ max.	30	mA
$P_{tot}$ max. ( $T_{amb} \approx 25^\circ C$ )	220	mW

### Temperature

$T_{stg}$ min.	-65	$^\circ C$
$T_{stg}$ max.	125	$^\circ C$
$T_j$ max.	125	$^\circ C$

## THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	0.45	degC/mW
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## ELECTRICAL CHARACTERISTICS ( $T_{amb} = 25^\circ C$ unless otherwise stated)

		Min.	Typ.	Max.	
$-V_{BE}$	Base-emitter voltage (see note 1) $I_C = 1.0mA, V_{CE} = 10V$	650	-	740	mV
$I_B$	Base current $I_C = 1.0mA, V_{CE} = 10V$	8.0	15	28	$\mu A$
$-C_{re}$	Feedback capacitance $I_C = 1.0mA, V_{CE} = 10V,$ $f = 0.45MHz$	-	0.95	-	pF
$f_T$	Transition frequency $I_C = 1.0mA, V_{CE} = 10V$	-	200	-	MHz

## NOTE

- $V_{BE}$  decreased by approximately 1.7mV/degC with increasing temperature.

## SOLDERING NOTE

For soldering irons or for dip-soldering, the iron temperature or solder temperature may rise to  $300^\circ C$  for a maximum of three seconds, with the transistor lock-fitted on printed boards in either of the possible mounting positions.



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## ELECTRICAL CHARACTERISTICS (cont'd)

		Min.	Typ.	Max.
N	Noise figure			
	$I_C = 1.0\text{mA}$ , $V_{CE} = 10\text{V}$ ,			
	$g_s = 20\text{mmho}$ , $f = 1.0\text{MHz}$	-	3.5	- dB
	$g_s = 10\text{mmho}$ , $f = 100\text{MHz}$	-	4.0	- dB
$N_c$	Conversion noise figure			
	$I_C = 1.0\text{mA}$ , $V_{CE} = 10\text{V}$ ,			
	$g_s = 1.2\text{mmho}$ , $f = 0.2\text{MHz}$	-	4.0	- dB
	$g_s = 1.5\text{mmho}$ , $f = 1.0\text{MHz}$	-	2.5	- dB

## Typical y-parameters

Common base

$I_C = 1.0\text{mA}$ ,  $V_{CE} = 10\text{V}$ ,  $f = 100\text{MHz}$ , lead length = 3.0mm

$g_{ib}$	Input conductance	38	mmho
$-b_{ib}$	Input susceptance	1.0	mmho
$ y_{rb} $	Feedback admittance	440	$\mu\text{mho}$
$\angle_{rb}$	Phase angle of feedback admittance	275	deg
$ y_{fb} $	Transfer admittance	34	mmho
$\angle_{fb}$	Phase angle of transfer admittance	140	deg
$g_{ob}$	Output conductance	12	$\mu\text{mho}$
$b_{ob}$	Output susceptance	1.1	mmho

Common emitter

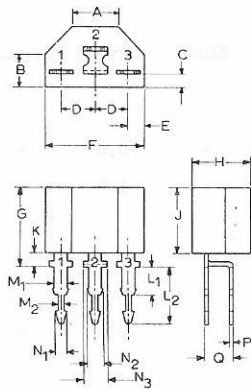
$I_C = 1.0\text{mA}$ ,  $V_{CE} = 10\text{V}$ , lead length = 3.0mm

		$f =$	10.7	0.45	MHz
$g_{ie}$	Input conductance		< 0.96	< 0.86	mmho
$g_{oe}$	Output conductance		< 9.5	< 7.0	$\mu\text{mho}$



OUTLINE AND DIMENSIONS

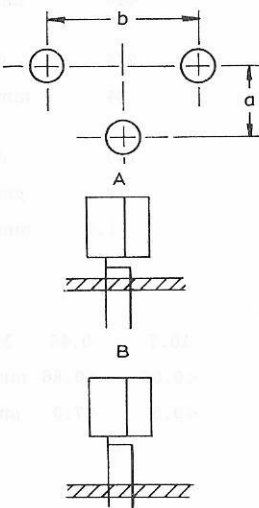
Millimetres



	Min.	Max.
A	3.4	3.6
B	2.4	2.6
C	0.8	1.1
D	2.44	2.64
E	1.1	1.3
F	7.4	7.6
G	6.0	6.4
H	4.4	4.6
J	4.9	5.1
K	1.0	1.3
L1	2.1	2.2
L2	4.0	4.3
M1	0.65	0.80
M2	0.45	0.60
N1	0.70	0.80
N2	1.15	1.25
N3	1.75	2.00
P	0.17	0.25
Q	1.75	2.00

Pin connections 1. Base  
2. Emitter  
3. Collector

Mounting details



$a = 2.49$  to  $2.59\text{mm}$

$b = 5.03$  to  $5.13\text{mm}$

Maximum thickness of printed board =  $1.7\text{mm}$

Hole diameter =  $1.25$  to  $1.35\text{mm}$

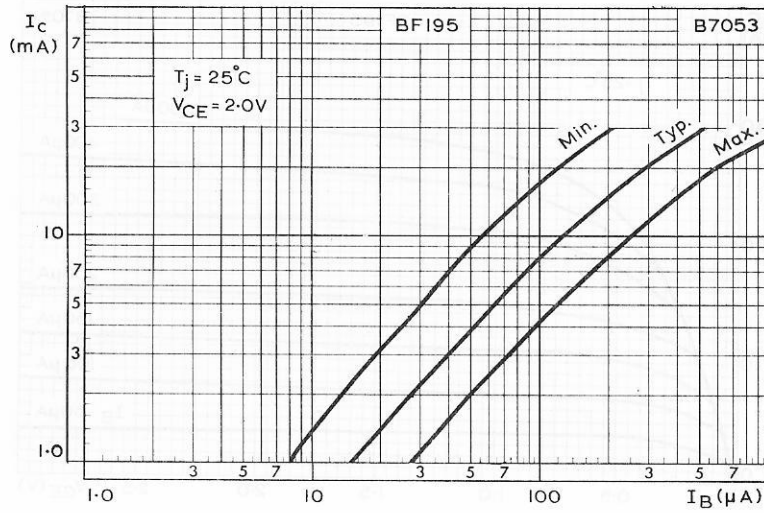
Maximum thickness of printed board =  $1.1\text{mm}$

Hole diameter =  $0.77$  to  $0.83\text{mm}$

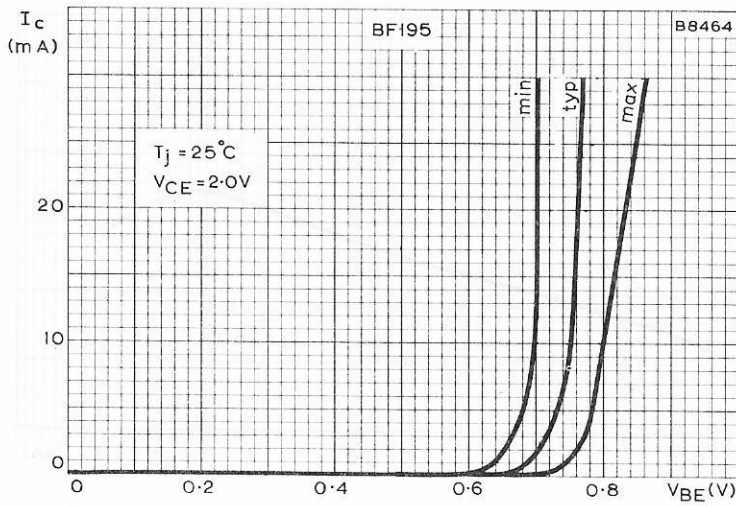


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TRANSFER CHARACTERISTICS,  $T_j = 25^\circ\text{C}$

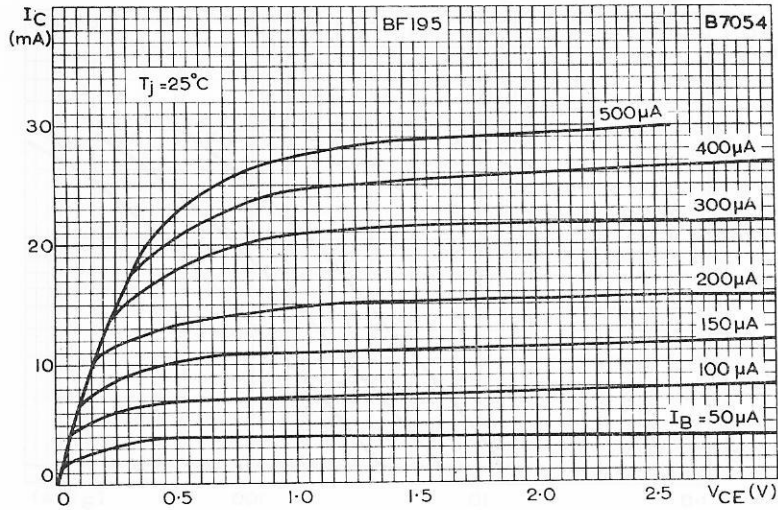


MUTUAL CHARACTERISTICS,  $T_j = 25^\circ\text{C}$

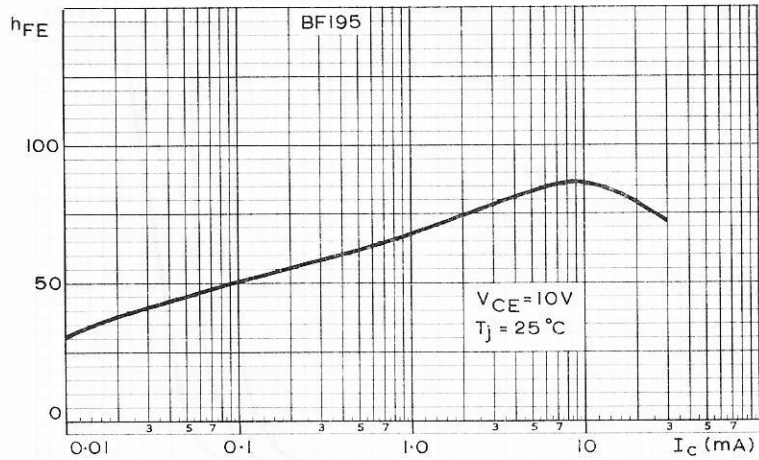


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TYPICAL OUTPUT CHARACTERISTICS,  $T_j = 25^\circ\text{C}$

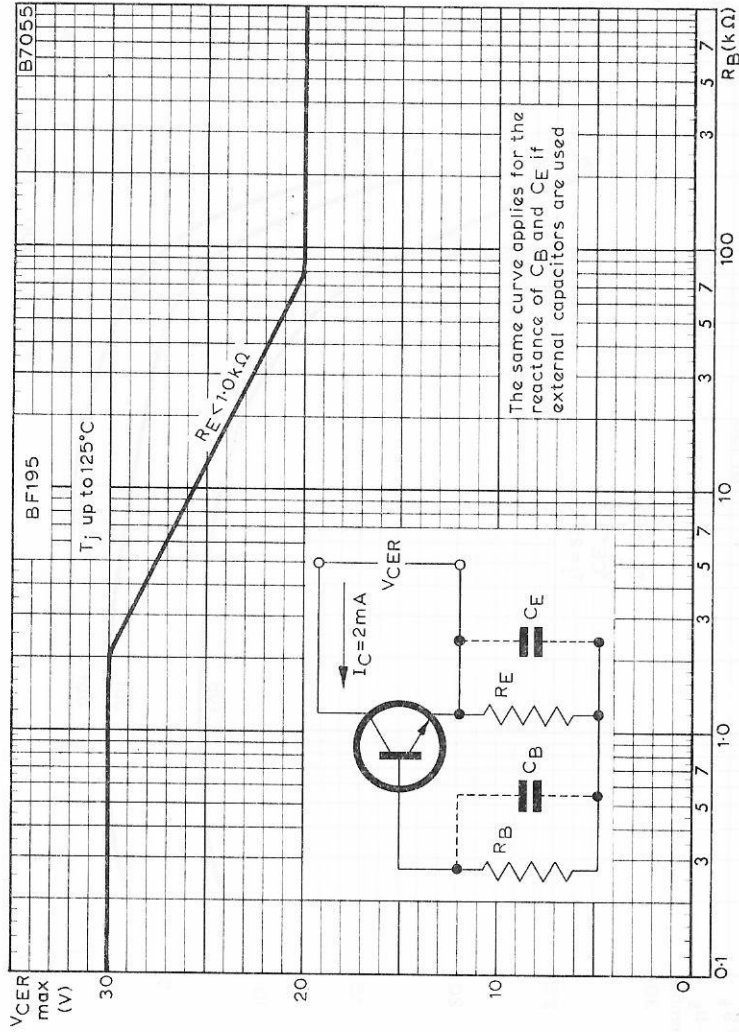


TYPICAL STATIC FORWARD CURRENT TRANSFER RATIO PLOTTED  
AGAINST COLLECTOR CURRENT



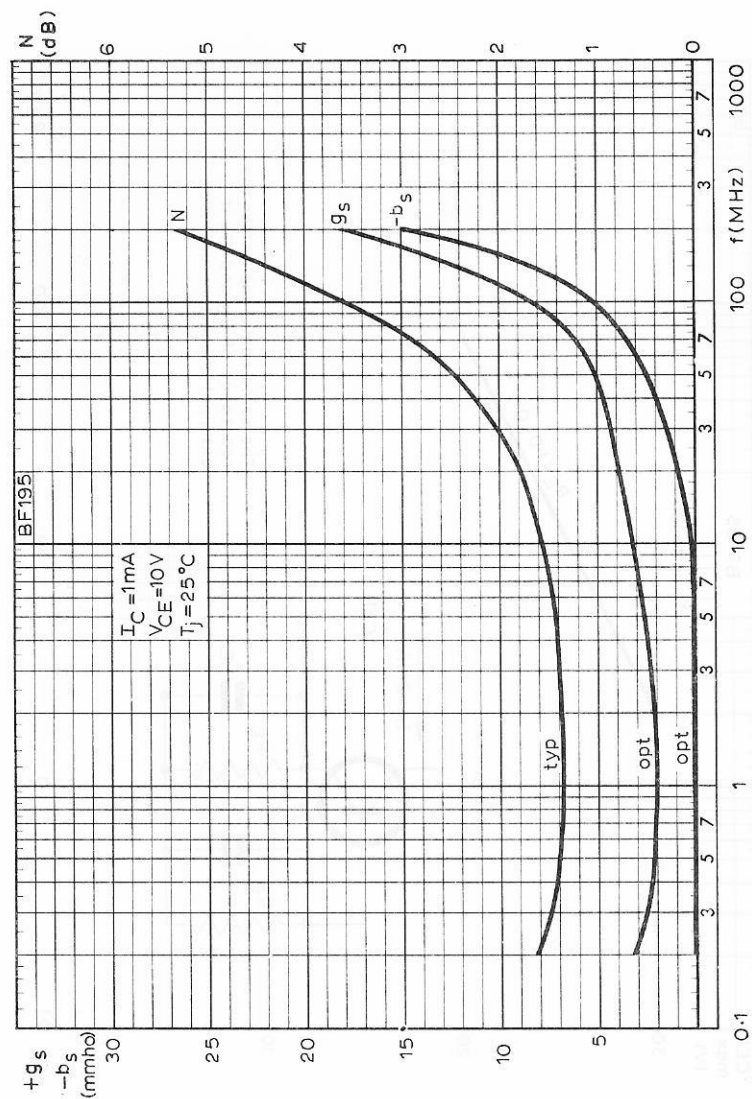
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MAXIMUM COLLECTOR-EMITTER VOLTAGE PLOTTED AGAINST  
EXTERNAL BASE RESISTANCE



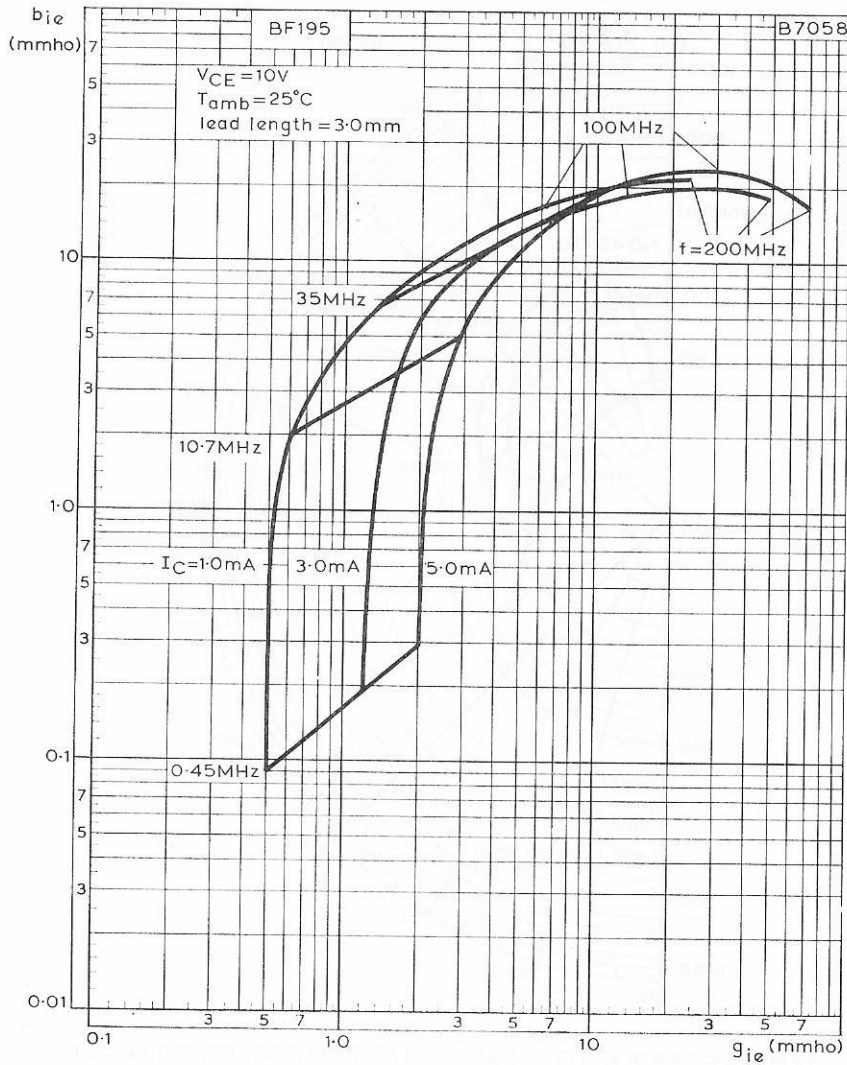


TYPICAL SOURCE CONDUCTANCE AND SOURCE SUSCEPTANCE  
 PLOTTED AGAINST FREQUENCY AT OPTIMUM SOURCE ADMITTANCE  
 TYPICAL NOISE FIGURE PLOTTED AGAINST FREQUENCY AT  
 OPTIMUM SOURCE CONDUCTANCE



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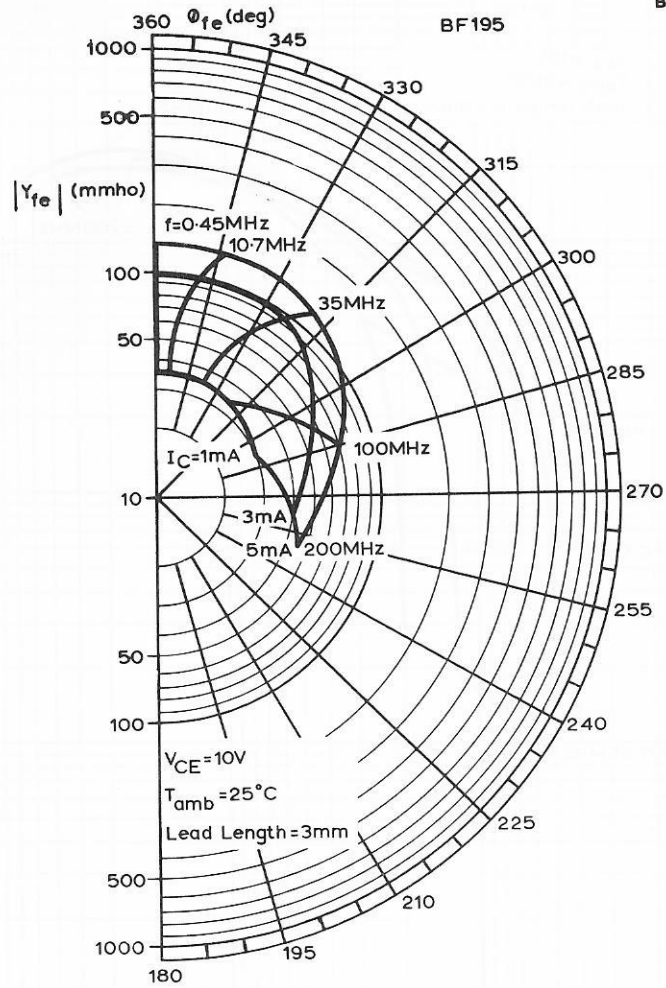
TYPICAL COMMON EMITTER INPUT ADMITTANCE WITH COLLECTOR  
CURRENT AND FREQUENCY AS PARAMETERS



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TRANSISTOR DATA  
MULLARD

B7059



TYPICAL COMMON EMITTER TRANSFER ADMITTANCE WITH COLLECTOR CURRENT AND FREQUENCY AS PARAMETERS

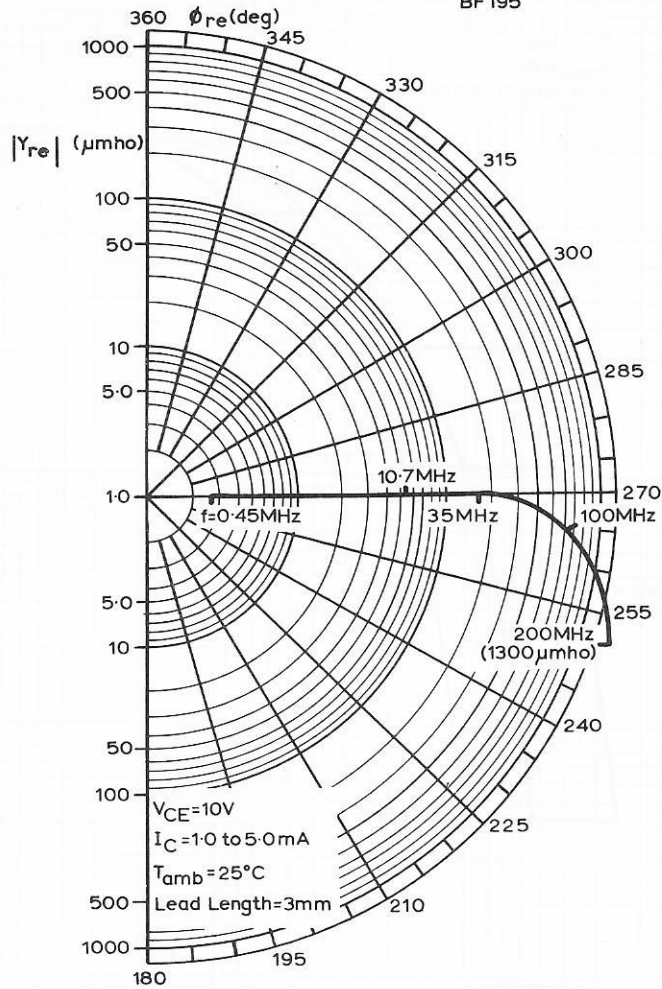


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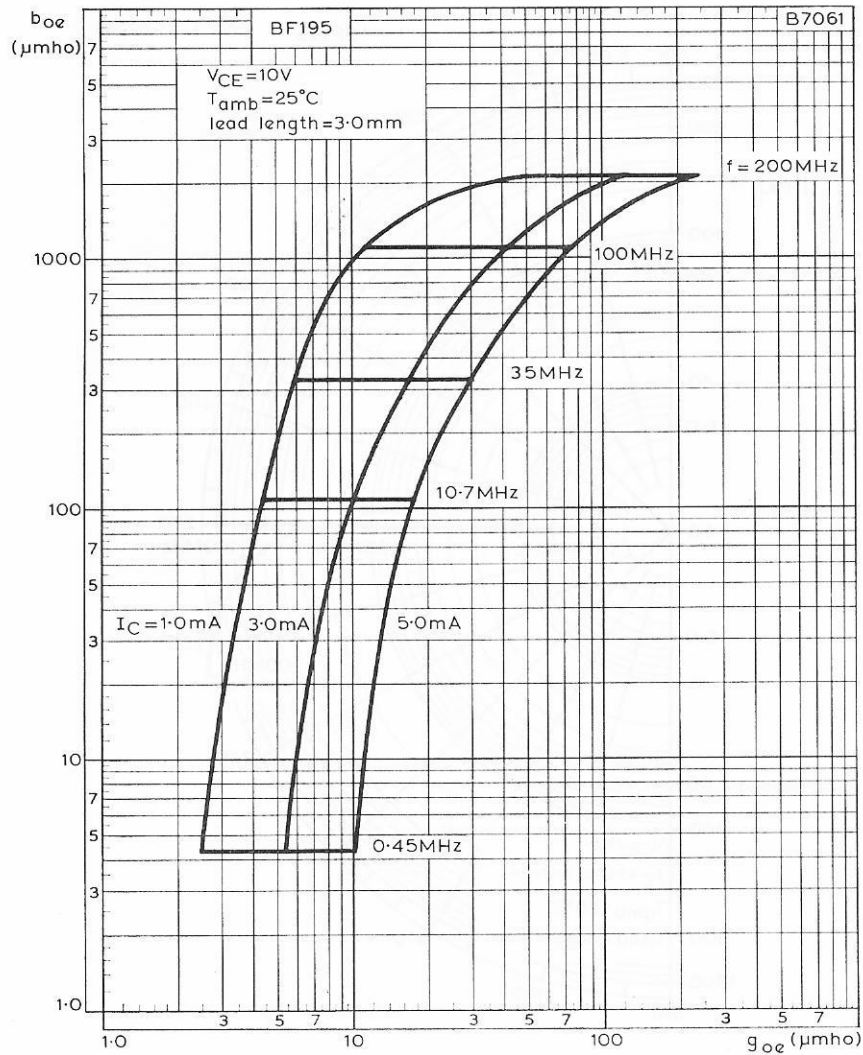


TYPICAL COMMON EMITTER FEEDBACK ADMITTANCE WITH COLLECTOR CURRENT AND FREQUENCY AS PARAMETERS



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TYPICAL COMMON EMITTER OUTPUT ADMITTANCE WITH  
COLLECTOR CURRENT AND FREQUENCY AS PARAMETERS

