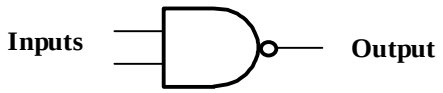
Understanding Open-collector Outputs

If you're not already familiar with the basics of logic gates and how to determine their output state based on their input states, I suggest checking out the underlined blue links provided throughout this document.

In order to well understand what an **open-collector** output is and when it might be used, let us first consider a common gate that does *not* employ it: the venerable and ubiquitous 7400 quad NAND gate.[1] (Of course, the actual part number on the chip will be something like LM7400N, SN74HC00, or any of dozens of variations on this theme, and many of these will have special properties such as employing high-speed CMOS or Schottky technology, but then you knew that already, right?) Its output will be a logic high under all input conditions until both inputs are high simultaneously. Under this condition the output will go low.



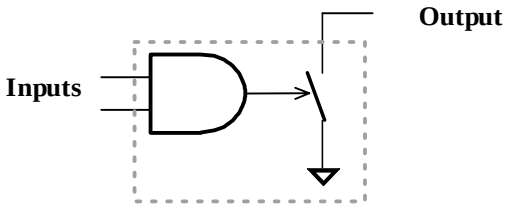
1/4 7400 NAND gate

Simple enough.

(The actual voltages involved in a logic state can vary, particularly in CMOS devices, although *usually* high will be near +5VDC, and low will be near 0VDC, standard TTL levels.)[2]

Now, let's consider its sister chip, the 7401, which is a quad **open-collector** NAND gate. Some datasheets will say "**open-drain**," which is a MOS version of the same concept, and they work basically the same way.

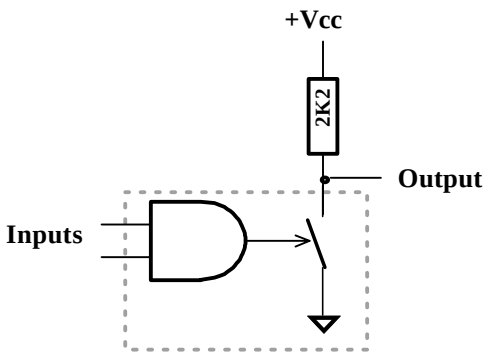
In order to consider it, envision an AND gate, not NAND, whose output is connected to a switch in such a way that the switch closes whenever the gate's output goes high, like this:



So what would you read if you measured across the switch? When it closes or opens, how would your reading change?

It wouldn't, of course.[3] In fact, such an output, by itself, appears pretty much useless.

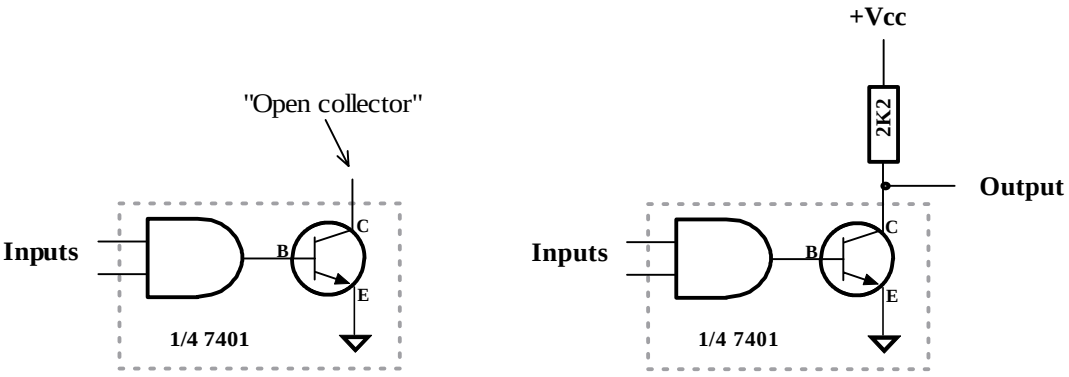
Ah, but an open-collector output is *far* from useless. You just have to apply it as it was designed to be applied, which is with a **pull-up resistor** on the output. Something like this:



Now what will you read when the switch closes? When it opens? And do you see why it's called a "pull-up" resistor?

What you actually get, in spite of this being an AND gate with a switch after its output, is a NAND function. When both inputs are high, the switch closes--and the output reads 0V, or logic low. In any other input condition the switch is open, and you read essentially +Vcc, which is logic high, since the output is "pulled up" to +Vcc by the resistor.

This is implemented with a semiconductor switch, of course, not a mechanical one like the above drawing implies.



Gate with open-collector output: A. Raw gate **B. Connected in circuit**

When the AND gate's output goes high, the transistor turns on fully saturated, and the collector-to-emitter resistance drops nearly to zero. The result is obviously the same: you end up with NAND functionality. And this is the reason for the term "**open-collector,**" since that's exactly what we have here. The output consists of a transistor whose collector is *open*, i.e. not connected to anything until *we* connect something to it (such as a resistor and voltage source).

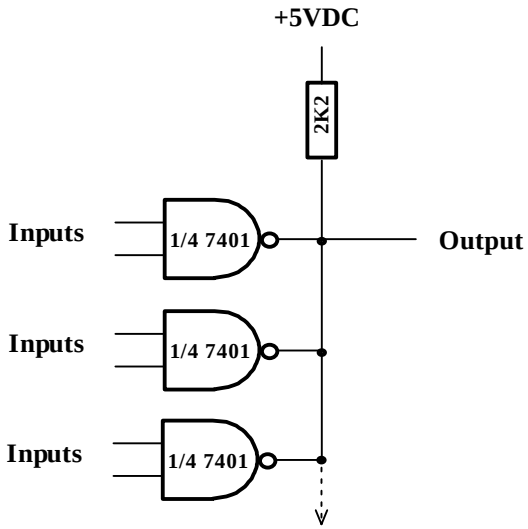
You do need to make sure that the current-sinking capacity of the gate can handle the current set by the resistor (2.3mA in this case, which is easily within the specs of most 7401s). And the value of the resistor is not critical, although it will affect things like the speed at which the output can switch. But that's a bit beyond our purview here.

Now I know you're just *dying* to ask, "why?" Why go to all the trouble of adding a resistor and extra connections to a gate to make it work when you can just use a 7400 and be done with it?

Good question.

There are two basic reasons, with many variations.

First, and most importantly, you can connect several such devices so that their outputs are in parallel and achieve something called "**wire-OR**" functionality.



"Wire-ORed" Outputs

Note that I'm no longer explicitly drawing the output transistor. It's still there, of course, inside the gate package, where it always was.

This configuration has the advantage that when any one--or any combination--of NAND outputs goes low, the whole output bus goes low. What we've done is added the functionality of an extra three-or-more-input gate simply by wiring the outputs together. And you certainly don't have to stop at just three gates as shown above.

I realize that, technically, I've just described an AND function, not OR. But these devices are active-low, so in an intuitive sense, it's OR functionality--when any single gate, or any combination of them, goes active, the output goes active. In fact, many do indeed call this arrangement "**wire-ANDed,**" which, while true, seems a bit confusing to me. Your choice.

This is how those mysterious **tri-state** gates work, too. Notice that when an individual open-collector output is off, it will neither sink nor source any current. This state, called **high-impedance** (or Hi-Z) **output**, allows it to sit on a bus somewhere neither affecting nor being affected by the state of the bus, and even leads to gates that are **bi-directional**, serving as both inputs *and* outputs, depending on the need of the moment. I^2C and SMBus both work this way.

A second reason to use open-collector outputs is that many of them (not all) are designed specifically to sink much larger amounts of current, and handle higher voltages, than other output types can. The 7406 hex inverter buffer/driver is one example, but there are many others. This comes in very handy when one wants to drive LEDs, several gate inputs, or even small relays. It saves you the trouble of using discrete driver transistors, for example, as they're already built into the device. And, as mentioned, many of these devices allow the pullup resistor to be connected to a different voltage than that which the chip itself uses, permitting you to interface the output to higher--or lower--voltage levels, or drive devices that other chips could not drive directly.

Lots of other devices employ open-collector outputs too, not just logic gates. Some voltage comparators have them. Sensors such as solid-state proximity switches sometimes use them. They're everywhere, because they're both useful and easy to use. And remember that open-drain devices work the same way, with MOSFET outputs instead of bipolar ones.

The web contains a lot of information on this subject besides what has been linked here. As they say, "Google is your friend!" So is Wikipedia, one of my favorite places to browse for obscure and arcane information on all manner of subjects. You know, the kind of stuff that only Alien Steve would otherwise know.

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1 *Okay, perhaps the 7400 isn't quite so common any more, in this age of microprocessors and ASICs and all. But it's certainly* been *common enough for decades, and you'll still see it often in vintage electronics dating from the early 60s (when a single 7400 quad-NAND package could cost $1000. Yes, apiece).*

2 *I recently worked for an employer who vigorously disdained the use of the terms "*high*" and "*low*" by his employees on the grounds that they were nebulous words that indicated sloppy, imprecise thinking. His point, which was well-taken, was that many technicians take both terms way too loosely and don't really think about what they're saying--much as many non-technical people say that something has a "short" in it, without really knowing (or caring) what a short is. My point to him was that, in the context of digital logic, the words "*high*" and "*low*" are actually very rigorously defined, and that while anyone can misuse any term, there is nothing at all wrong with the words themselves.*

*While he seemed to mollify his stance in response, his original point remains. Don't be guilty of calling a gate's pin "*high*" or "*low*" as if you were scoring a game of vertical horseshoes. "Close don't count" in electronics, at least not if you want to be good at it.*

3 *In the case of devices that use bipolar transistor outputs, you may in fact read a small voltage, on the order of about 0.6VDC, when the transistor is off (switch open and disconnected from all other circuitry), but this is hardly a valid logic high, of course. Just don't be tempted to let this be the extent of your testing of the device; to truly test an open-collector output, you must verify that it will both saturate, sinking the required current to pull the output to within 0.1VDC or less of zero, in most cases, plus turn off completely enough to allow the output to pull up to within a similar distance of +Vcc.*