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Switching Voltage Transient Protection Schemes for High Current IGBT Modules

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Abstract: *The emergence of high current and faster switching IGBT modules has made it imperative for the designers to look at ways of protecting these devices against detrimental switching voltage transients that are a common side effect of these efficient transistors. This paper will discuss protection criteria for both normal switching operation and short circuit operation and will cover in detail some of the protection schemes that were designed to address these problems.*

Introduction

When a power device is abruptly turned off, trapped energy in the circuit stray inductance is dissipated in the switching device, causing a voltage overshoot across the device. The magnitude of this transient voltage is proportional to the amount of stray inductance and the rate of fall if turn-off current. Large IGBT modules switch high magnitudes of currents in a short duration of time, giving rise to potentially destructive voltage transients. These higher current modules normally consist of several IGBT chips in parallel. Each individual chip switched its share of the load current at a di/dt that is determined by the gate drive circuit. The total current and di/dt seen by the external power circuit is the sum of currents and di/dts through each IGBT chip. The situation is at its worst when a short circuit current is rapidly turned off to protect the IGBT. The di/dts produced could easily be a few thousand A/us. If proper attention is not paid to minimize resulting switching voltage transients, any attempt to save IGBTs, by shutting them down under fault conditions, may destroy the device.

This paper discusses various protection schemes. A transient voltage protection scheme optimized to protect IGBTs during normal switching operation may not protect the IGBTs under the fault current shut off process. Separate schemes would normally be required to achieve both goals.

It is determined that the snubbers and clamps offer optimized protection against voltage transients during normal switching operation. Operation of an RCD clamp circuit is described in detail. All illustrated in Fig. 1, protection circuits allow faster yet safer operation by containing operating loci within the boundaries of the rated Safe Operating Area (SOA).

Fault current shut off transients are more effectively protected by considerably slowing the rate of fall of fault current. Two novel protection schemes are introduced which protect IGBTs from potentially destructive voltage transients by slowing the rate of fall of fault current, only under fault conditions. Circuit operations are analyzed and the test results are illustrated. Usefulness of an active clamp is also discussed in this section.

Voltage Transients During Normal Switching Operation

As mentioned earlier, the magnitude of transient voltage depends on the trapped energy in the circuit stray inductance, also call “DC loop” inductance LS. As a preventive measure, steps should be taken to improve the circuit layout. Usage of capper plates separated by a thin sheet of insulating material, tightening the “DC loop” and choosing source capacitance with inherently low self inductance are ways to lower stray inductances [1]. Decoupling capacitors, connected across the module terminals, can also be used to achieve this goal. High frequency polypropylene capacitors designed for low internal lead inductance are found to be effective. Care should be taken in the selection of the decoupling capacitor value to avoid oscillations in the DC loop which otherwise may result in excessive heating in the high frequency capacitors. For modules raised up to 100A or so, decoupling capacitors may provide optimal protection against voltage transients during normal switching.

One other way to prevent high voltage transients from occurring is to slow down the switching process, by choosing a greater value of gate resistor. While this is an attractive method for the fault current turn-off protection, it is not practical for protection against voltage transients during normal switching operation as the efficiency of device operation is adversely affected.

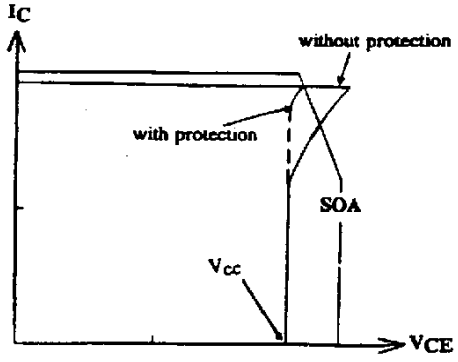

Figure 1. Rated SOA curve and operating loci with and without Switching Voltage Transient Protection circuit.

In the following discussion more efficient ways of protecting devices will be presented.

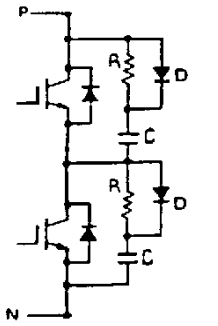

Figure 3. RCD Charge/Discharge Snubber

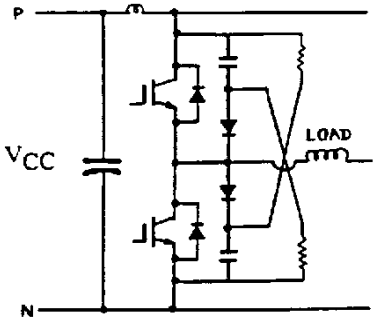

Figure 2. RCD Voltage Clamp

RCD Snubber and clamp circuits

Figures 2 and 3 are two principal examples of RCD snubbers for high current IGBT applications. While both circuits are employed to reduce transient voltages across switching devices, the charge/discharge snubber circuit in Fig. 3 is targeted also for reducing IGBT turn off losses. During IGBT turn on, the snubber capacitor is fully discharged and during turn off, it is charged. This circuit, unlike the circuit in Fig. 2 which essentially acts as a clamp, reduces the rate of rise of voltage across the IGBT at turn-off, imposing a softer switching and therefore reducing losses in the IGBT. The losses in the snubber, however are substantially increased and are equal to $\frac{1}{2} \cdot C \cdot V_{pk}^2$, where V_{pk} is the voltage across snubber capacitor at the end of turn-off process and is equal to the DC bus plus an allowable overshoot voltage.

Due to the dual purpose that the circuit in Fig. 3 serves, the trade-offs involved are complex. Since this paper concentrates only on the switching voltage transient protection, discussion will be focused to the circuit in Fig. 2. The effects of this snubber on turn off and turn on will be discussed separately in the following.

Turn-off

The RCD clamp of Fig. 2 acts as a voltage clamp. During IGBT conduction period the snubber capacitors are charged to the bus voltage. As the IGBT is turned off the voltage across it, V_{CE}, rises rapidly. The circuit "DC loop" stray inductance, L_s, may cause V_{CE} to rise above the bus voltage. As this occurs, the snubber diode is forward biased and the snubber is activated. The energy trapped in the stray inductance now is diverted to the snubber capacitor which absorbs this incremental energy without substantial rise in its voltage. The waveforms shown in Fig. 4 clearly illustrate the turn-off behavior with and without the RCD clamp. The voltage overshoot has been substantially reduced from 210 Volts to only 50 volts. Initially a small stray inductance in the snubber circuit causes V_{CE} to peak slightly above V_{CC}.

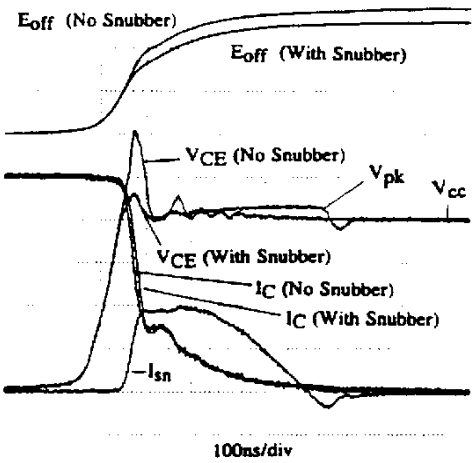

Figure 4. Turn-off waveforms with & without RCD snubber.
Tested at: 400V, 100A, 25°C ; L_S = 100nH,
$V_G/R_{G(off)}$ = -8V/33Ω
C_{sn} = 0.22μF, R_{sn} = 12Ω
V_{CE}: 100V/div, I_C/I_{sn}: 20A/div, E_{off}: 2mJ/div

Fig. 5 displays the waveforms generated for two different stray inductances (100nH, 340nH). As illustrated in the figure the initial V_{CE} peak - which is dependent on the stray inductance within the snubber circuitry - is the same for the two cases. The final voltage peak (V_{pk}) for the higher inductance does reach a higher value as

expected since there is more trapped energy ($\frac{1}{2}\cdot L_S \cdot I^2$)diverted to the same snubber capacitor. This value however is well within the voltage rating of the device and only marginally influences the losses in the IGBT, since it occurs when the current has reached to a smaller value. The V_{pk} magnitude can be calculated from the formulae given in the following section.

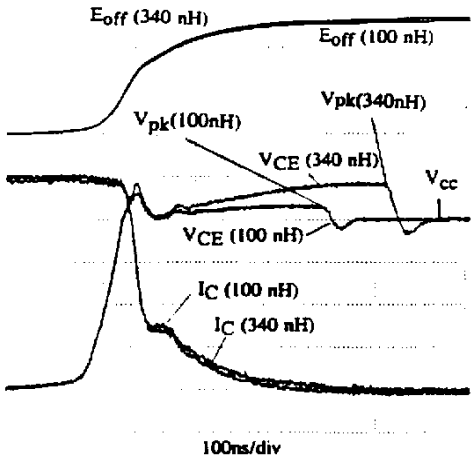

Figure 5. Turn-off waveforms with RCD snubber for two different L_S values (100nH, 340nH).
Tested at: 400V, 100A, 25°C; $V_G/R_{G(off)}$ = -8V/33Ω
C_{sn} = 0.22μF, R_{sn} = 12Ω
V_{CE}: 100V/div, I_C: 20A/div, E_{off}: 2mJ/div

Turn-on

Fig. 6 displays the turn on waveforms for an unprotected IGBT with a gate resistor (R_G) of 5.1 Ohms. The rapid rise in the IGBT current (1200 A/μs) combined with the circuit stray inductance (300 nH) caused the FWD to go through severe reverse recovery process. As seen in the figure, the FWD recovery voltage (=630V) actually exceeded the rated voltage of the module.

In order to bring this voltage down to a safe value, the turn on di/dt was lowered by using a higher R_G. The results are shown in Fig. 7. The increase in R_G, however had profound effect in increasing the switching losses, as expected [2], [3].

The RCD clamp shown in Fig. 2 is also effective in reducing turn-on voltage transients. As the IGBT current rises, the $L_S \cdot di/dt$ voltage loss causes the voltage across the positive and negative terminals of the module, V_{ab}, to drop by the same amount (i.e. to $V_{CC} - L_S \cdot di/dt$). The snubber capacitors that were fully charged to V_{CC}, now find a discharge path through the forward biased Free Wheel Diode (note that the FWD is on, freewheeling the load current), the IGBT and the snubber resistors. Fig. 8 shows the equivalent circuit during turn on. The snubber diodes are reverse biased and therefore not shown. The current paths are shown in the figure. This snubber discharge current (I_{sn}) partially provides for the reverse recovery charge of the FWD, thus the total current seen by L_S is modified. This has a favorable effect on the magnitude of the reverse recovery voltage transient.

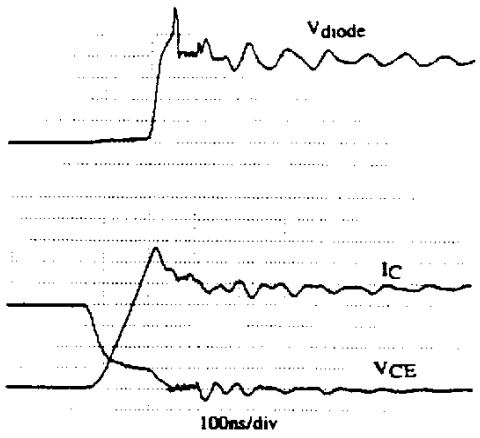

Figure 6. Turn-on waveforms for an IGBT with no RCD snubber protection .
Tested at: 400V, 100A, 25°C ; L_S = 240nH,
V_G/R_G (on) = 15V/5.1Ω
V_{CE}: 100V/div, I_C: 20A/div, V_{diode}: 100V/div

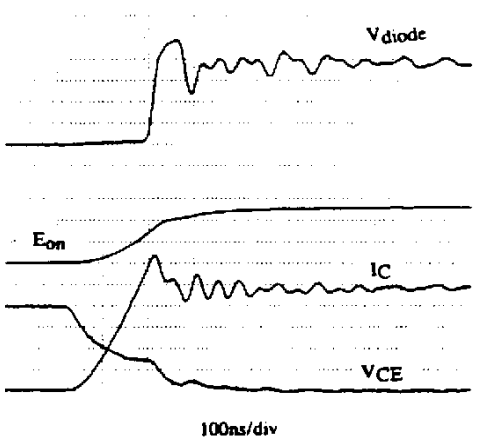

Figure 7. Turn-on waveforms for an IGBT with no RCD snubber protection .
Tested at: 400V, 100A, 25°C ; L_S = 240nH ,
V_G/R_G (on) = 15V/33Ω
V_{CE}: 100V/div, I_C: 20A/div, V_{diode}: 100V/div, E_{on}: 1mJ/div

The waveforms shown in Fig. 9 illustrate the snubber operation. Notice the complete elimination of the voltage

transient and also reduction in the oscillations following turn on. Another interesting fact is that this waveform was generated with R_G of 0.5 Ohm which reduced the energy losses from 2.41 mJ in Fig. 7 to 1.25 mJ, a savings of almost 50%! Therefore this snubber, not only clamps the turn on voltage transient, but also enables the user to choose a value of R_G that produces minimal turn on losses.

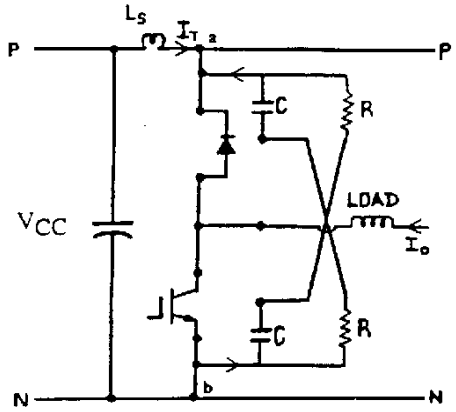

Figure 8. Equivalent circuit under turn-on conditions. Low-side IGBT is switched on.

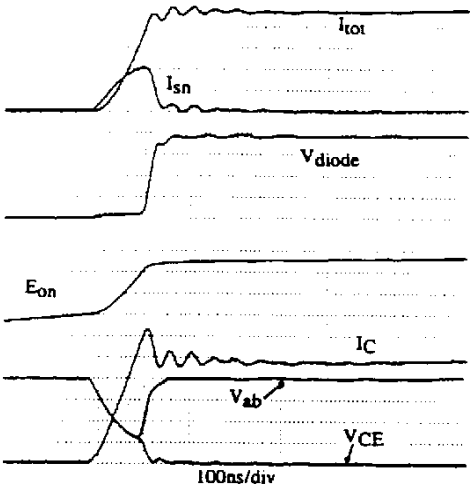

Figure 9. Turn-on waveforms with RCD snubber.
Tested at: 400V, 100A, 25°C ; L_s = 240nH,
$V_G/R_{G(on)}$ = 15V/0.5Ω
C_{sn} = 0.22μF, R_{sn} = 12Ω
V_{CE}/V_{diode}: 100V/div, $I_C/I_{sn}/I_{total}$: 20A/div, E_{on}: 0.5mJ/div
V_{ab}:100V/Div

Fig. 10 Shows the effect of changing the snubber resistor (R_{sn}) on turn on waveforms. Lower R_{sn}s provide for better snubbing action.

The value for the snubber components can be approximated from the expressions given below, based on circuit stray inductance L_s, switching frequency f_{sw}, maximum switching current I_o, turn-on current rise time t_r, DC rail voltage V_{CC} and allowable peak voltage V_{pk} (Appendix I).

Snubber capacitor :

$$C_{sn} = L_s \cdot I_o^2 / (V_{pk} - V_{CC})^2 \quad (1)$$

Snubber resistor:

$$R_{sn} = 1 / (6 \cdot C_{sn} \cdot f_{sw}) \quad (2)$$

Losses in Snubber resistor :

$$P_R = [\ ½ \cdot C_{sn} \cdot (V_{pk}^2 - V_{CC}^2) + 1.125 \cdot L_s^2 \cdot I_o^2 / (t_r \cdot R_{sn})] \cdot f_{sw} \quad (3)$$

The snubber diode should be of fast and soft recovery type to avoid severe oscillations following V_{pk} at turn off. The resistor should be of non-inductive type to avoid oscillations at turn-on.

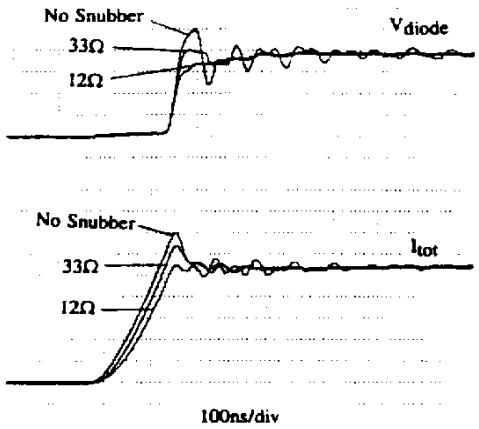

Figure 10. Effect of changing R_{sn} values.
Tested at: 400V, 100A, 25°C; L_s = 240nH,
$V_G/R_{G(on)}$ = 15V/33Ω
C_{sn} = 0.22μF, R_{sn} = 12Ω, 33Ω
V_{diode}: 100V/div, I_{total}: 20A/div

Voltage Transients during Fault Current Turn-off

The short circuit current generated during fault conditions can be up to five to ten times the rated current. Shutting off such high currents too quickly can produce extremely high di/dts that are potentially detrimental to the IGBTs[4].

The RCD clamp circuit discussed in the above section is not as practical when it comes to protecting transient voltages generated during short circuit conditions. As seen from the above expressions, the

required snubber capacitor value is proportional to the square of the device current. This means that the capacitor required will have to be 25 to 100 times larger than in normal switching operation. High capacity, high voltage snubber capacitors are large and expensive (as for snubber capacitors required for GTO thyristors!), making the RCD scheme unattractive for high current IGBT modules. Also voltage clamps connected external to the modules do not address the problem of internal inductive voltage spike.

In the following we will discuss more practical methods. This involves slowing down the turnoff of the IGBTs under fault conditions.

The IGBT fault current rate can be reduced by slowing the turn-off gate voltage signal. The simplest way of achieving this, is to increase the gate resistor, but this is inefficient, since the tradeoff is increased switching losses during normal conduction.

In order to address the above problem two novel circuits are introduced that, through electronic gate control, effectively decrease the V_{GE} rate of fall only when a fault current is sensed, thereby avoiding any losses during normal switching operation. The first of these circuits utilizes a resistive method, and the other uses a capacitive method. In the resistive method, a considerably higher value of gate resistor is switched-in in series with the IGBT gate. In the capacitive method, a considerably higher value of external capacitor is switched-in in parallel with the IGBT gate input capacitance.

Resistive method

The circuit in Fig. 11 is composed of de-sat sense diode D1 and a P-Channel MOSFET to switch-in higher value of resistor, RG2, upon occurrence of a fault.

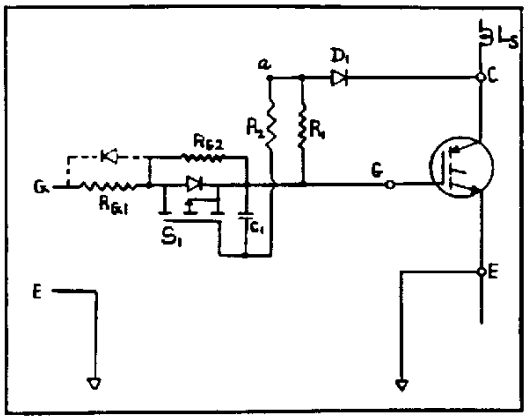

Figure 11. Circuit for the Resistive Method

Initially, when the IGBT is in the off state, the P-MOSFET is turned off. During normal turn on, a step rise in voltage is applied to the IGBT gate through RG1 and the inherent body diode of the P-MOSFET. As V_{CE}, after normal turn-on delay period, drops to its low on-state level, diode D1 is forward biased and input capacitance of the P-MOSFET starts to charge up. During normal conduction therefore, the P-MOSFET remains gated on.

During normal turn off operation, the gate drive output voltage is switched to its low state. The P-MOSFET gate capacitance begins to discharge. The values of C1, R1 and R2 are adjusted such that the MOSFET is kept on, at least until the IGBT turn off is completed (for example, 1μs). Therefore the IGBT turn off losses are not affected.

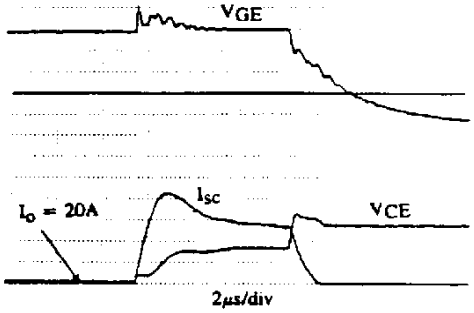

Figure 12. Short circuit waveforms with resistive protection scheme for "Fault Under Load" condition
Tested at: 280V, 25°C ; L_S = 240nH, V_G/RG1 = -8V/33Ω
V_{CE}: 100V/div, V_{GE} = 5V/div, I_{SC}: 200A/div

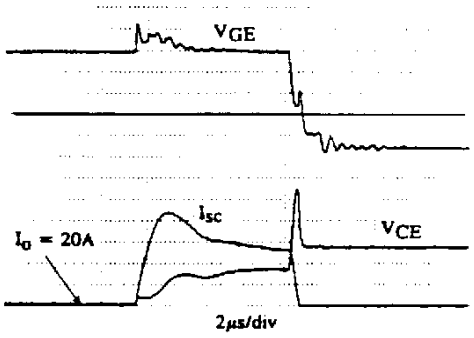

Figure 13. Short circuit Waveforms with no protection scheme for "Fault Under Load" condition
Tested at: 280V, 25°C ; L_S = 240nH, V_G/RG1 = -8V/33Ω
V_{CE}: 100V/div, V_{GE} = 5V/div, I_{SC}: 200A/div

Fault Under Load

When a fault occurs during normal conduction, diode D1 goes into blocking mode and the P-MOSFET input capacitance starts to discharge through resistors R1 and R2. The MOSFET is turned off as its gate voltage drops below the threshold value. Thereafter the V_{GE} rate of fall is reduced significantly as the discharge is now

forced to take place through RG2. The fault current fall rate is decreased accordingly. Note that if the IGBT is turned off while the MOSFET is still on, the circuit will not be effective, since RG2 is bypassed. The above consideration places an upper limit on the discharge time constant of the MOSFET (to say, 5μs).

Figs. 12 and 13 display short circuit switching waveforms with and without the protection circuit. The initial current through the IGBT is 40 A. Upon occurrence of the fault, the current shoots up to 800 A initially, but settles down to 600 A once the Miller effect on the gate voltage is diminished (see gate waveforms). The MOSFET discharge time constant was adjusted to be 2.5μs [(R1+R2) · (C_{iss}+C1)] Fault current was turned off after 6μs. As seen from the aforementioned figures the IGBT gate discharge rate was considerably slowed by the addition of RG2 (200 Ohms), thereby reducing the voltage overshoot from 270 V down to 60 V.

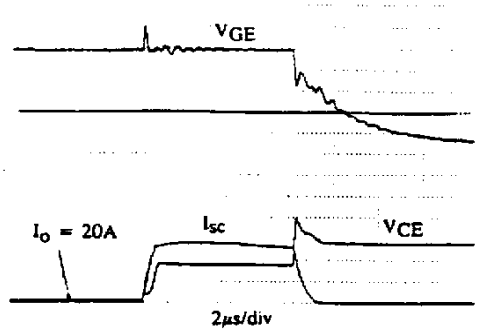

Figure 14. Short circuit waveforms with resistive protection scheme for "Fault Under Load" condition, with bypass diode across RG1
Tested at: 280V, 25°C ; L_S = 240nH, V_G/RG1 = -8V/0Ω
V_{CE}: 100V/div, V_{GE} = 5V/div, I_{sc}: 200A/div

The Miller effect can be filtered out by bypassing RG1 with a diode. The IGBT gate voltage is now clamped to the gate drive output voltage. Fig. 14 displays the resulting waveforms. Compare the results to Fig. 12 (same protection circuit without the R_{G1} bypass diode). The initial surge of current is eliminated. The slight increase in the turn-off voltage overshoot, as the RG1 is now bypassed during the IGBT turn off, can be compensated for by readjusting RG2 value.

Hard Fault

This is the case where the device turns on directly into a fault. The MOSFET is never turned on in this case. Therefore the discharge path for the V_{GE} is through RG2. Figs. 15 and 16 show the waveforms with and without protection circuit. The voltage overshoot was brought down to only 10 V from 190 V.

Note that this circuit increases the effective gate bias impedance during IGBT off time. This effect imposes an upper limit on RG2; value of which is governed by the IGBT characteristics and gate bias voltage.

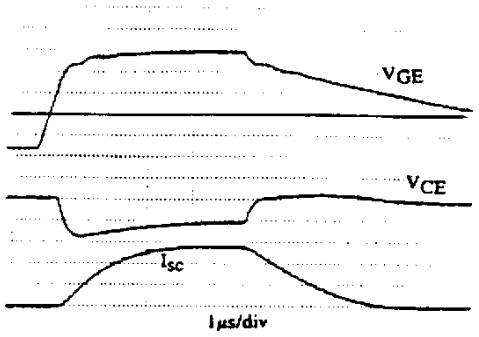

Figure 15. Short circuit waveforms with resistive protection scheme for "Hard Fault" condition
Tested at: 400V, 25°C ; L_S = 240nH, V_G/RG1 = -8V/33Ω
V_{CE}: 100V/div, V_{GE} = 5V/div, I_{sc}: 200A/div

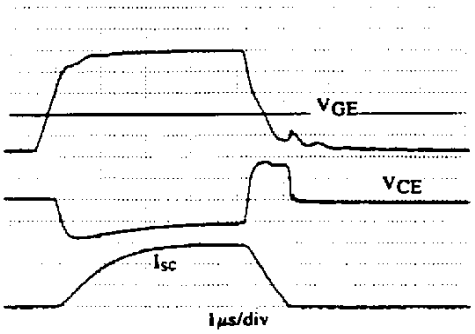

Figure 16. Short circuit waveforms with no protection scheme for "Hard Fault" condition
Tested at: 400V, 25°C ; L_S = 240nH, V_G/RG1 = -8V/33Ω
V_{CE}: 100V/div, V_{GE} = 5V/div, I_{sc}: 200A/div

Capacitive Method

The circuit in Fig. 17 is composed of de-sat diode D1, used to sense a fault condition, and a N-Channel MOSFET to switch-in a higher value of capacitor, C1, in parallel with the IGBT input capacitance upon occurrence of a fault.

During normal turn-on after the normal turn on delay, V_{CE} drops to its low on-state level and diode D1 is forward biased. The MOSFET gate charge time constant [(RG + R1 + R2) · R3 · (C_{iss}+ C3) / (RG+ R1 +R2 +R3)] is adjusted such that it is not turned on prior to the IGBT turning on (for example, 1μs). Therefore during the conduction period the MOSFET is in its off state. Zener diode Z2 is selected to offset large V_{CE}(on) voltages. False triggering of the MOSFET is therefore prevented.

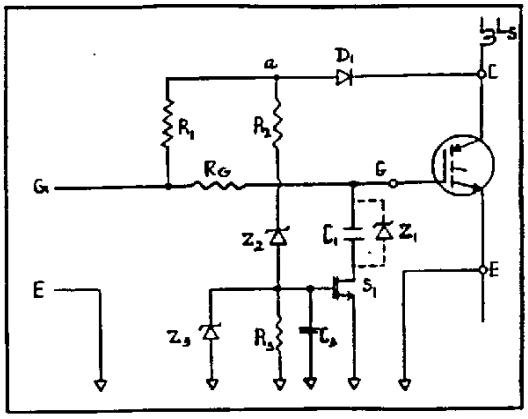

Figure 17. Circuit for the Capacitive Method

When the gate drive is switched to its off state to turn IGBT off, MOSFET remains turned off. The normal switching operation is therefore not affected by the existence of this protection circuit.

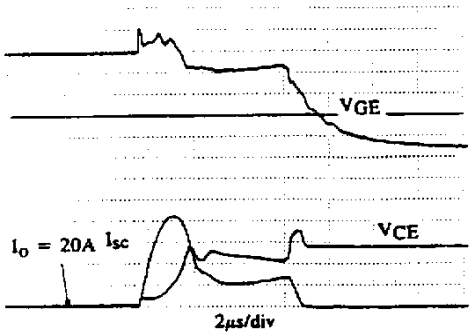

Figure 18. Short circuit waveforms with capacitive protection scheme for "Fault Under Load" condition
Tested at: 280V, 25°C ; L_S = 240nH, $V_G/R_{G(off)}$ = -8V/33Ω
V_{CE}: 100V/div, V_{GE} = 5V/div, I_{SC}: 200A/div

Fault Under Load

Once a fault occurs, the sense diode becomes reverse biased and the MOSFET gate input capacitance is charged by the gate drive power, through the voltage divider provided by R_G, R1, R2, and R3. When the MOSFET turns on, capacitor C1 is switched-in in parallel with the IGBT input capacitance. A drop is seen in the IGBT gate voltage since some charge is removed to charge the capacitor C1, which was initially charged to the off-bias voltage. This in turn lowers the value of the I_{SC} momentarily, reducing the energy losses during the short circuit period. The IGBT discharge time constant has increased since it now includes capacitor C1 in parallel with the IGBT input capacitance. The fault current turn off di/dt is therefore slowed and the transient voltage is brought down substantially. Fig. 18 shows the waveforms for the IGBT with the protection circuit. Compare this to the waveforms in 13 without the protection circuit. Once again turn off voltage overshoot was reduced from 270 V to 60 V.

Hard Fault

The operation of this protection circuit under hard fault is the same as described above. The upper limit of the MOSFET's gate charge time constant should be adjusted such that the MOSFET is fully turned on before the fault current is turned off (e.g. in less than 5μs). Fig. 19 displays the waveforms with and without the protection circuitry. As seen from the figure, the voltage overshoot was brought down from 160 V to 50 V.

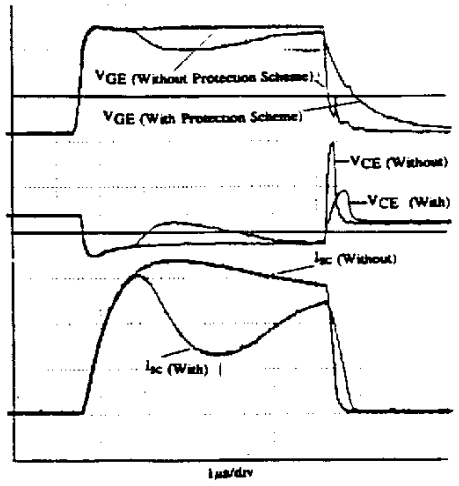

Figure 19. Short circuit waveforms with & without capacitive protection scheme for "Hard fault" condition
Tested at: 340V, 25°C ; L_S = 240nH, $V_G/R_{G(off)}$ = -8V/33Ω
V_{CE}: 100V/div, V_{GE} = 10V/div, I_{SC}: 200A/div

The functional usefulness of the circuit in Fig. 17 can be increased by simple addition of zener diode Z1 across capacitor C1 (indicated in the figure). The circuit now serves the dual purpose of preventing turn-off voltage transient as well as limiting fault current amplitude. The complete discussion on such a fault current limiting circuit is presented elsewhere [5].

Active Voltage Clamp

The circuit in Fig. 20 contains avalanche diode Z1 in series with blocking diode D1, connected between IGBT collector and gate. The avalanche diode is selected such that its voltage rating is less than the maximum allowable voltage at the IGBT module terminals. If this voltage limit is exceeded at the turn-off, the avalanche current I_{Z1} in $R_{G(off)}$ would raise the gate-emitter

voltage above its threshold level, therefore maintaining IGBT in conducting state. This feedback mechanism clamps V_{CE} to a safe value. The rate of decay of I_C is then equal to $(V_Z-V_{CC})/L_S$; where V_Z is the clamp voltage and V_{CC} is the DC bus voltage. Fig. 21 illustrates operation of this clamp circuit. For comparison, results obtained without this protection circuit are shown in Fig. 22. The peak turn-off voltage across 600V rated IGBTs was reduced from 580V to a safer level of 460V.

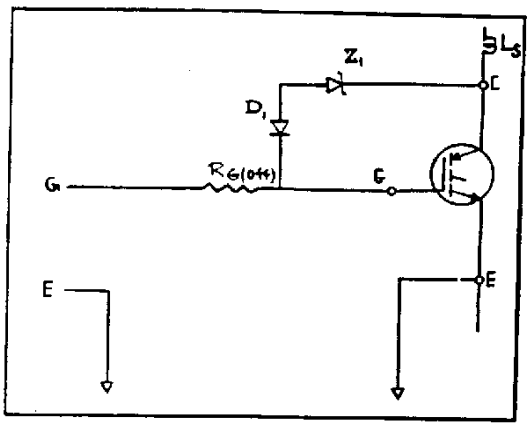

Figure 20. Circuit for Zener Clamp Protection Scheme

While the previously discussed (resistive and capacitive) circuits are activated immediately upon commencement of a fault, the circuit presently under consideration reacts only at turn-off. A slightest delay in re-gating of IGBT would result in potentially dangerous voltage spike. It was found that the combined junction capaciatances of Z1 and D1, if high enough, quickens charging of the IGBT gate by providing a dV_{CC}/dt feedback. At the same time, these capacitances, if too high, would noticeably contribute to the adverse Miller effect under normal operating conditions. Proper selection of these components is therefore extremely crucial to assure successful operation of this circuit. Also note that the value of $R_{G(off)}$, if too low, will make operation of this circuit less effective.

Except for unclamped inductive load applications, this circuit is not appropriate to protect against voltage transients during normal switching operation as substantial losses are incurred in the IGBT due to operation of the voltage clamp. The losses per pulse are given by the following equation:

$$P_{SW} = \tfrac{1}{2} \cdot I_o^2 \cdot L_S \cdot [V_Z/(V_Z - V_{CC})] \cdot f_{SW}$$

The value $\tfrac{1}{2} \cdot I_o^2 \cdot L_S$ is the energy trapped in the "DC loop" stray inductance. For V_Z of 550V and V_{CC} of 400V, the additional losses per pulse in the IGBT are almost four times that value.

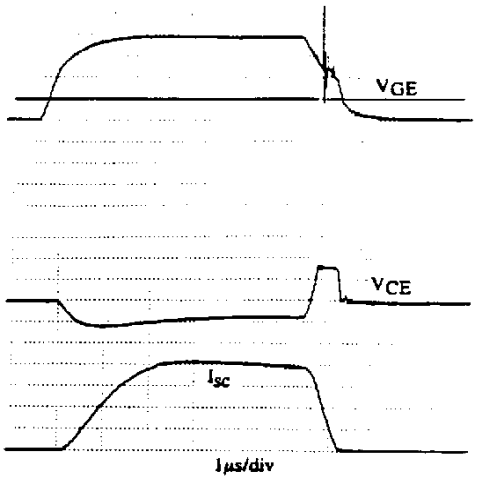

Figure 21. Short circuit waveforms with Zener clamp protection scheme for "Hard Fault" condition
Tested at: 300V, 25°C ; L_S = 240nH, $V_G/R_{G(off)}$ = -5V/33Ω
V_{CE}: 100V/div, V_{GE} = 5V/div, I_{SC}: 200A/div

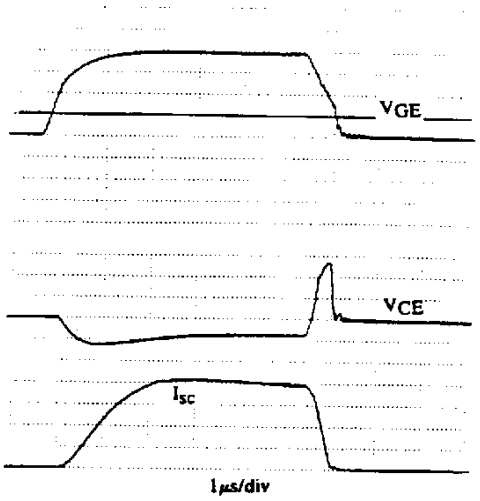

Figure 22. Short circuit waveforms without Zener clamp protection scheme for "Hard Fault" condition
Tested at: 300V, 25°C ; L_S = 240nH, $V_G/R_{G(off)}$ = -5V/33Ω
V_{CE}: 100V/div, V_{GE} = 5V/div, I_{SC}: 200A/div

The additional losses inflicted by the slower turn-off is not a major consideration during the fault operation as it is only a one time operation. Usefulness of this circuit is therefore restricted to fault current protection.

Conclusions

The problem of switching voltage transients is an important subject that can not be ignored, especially in applications where high current IGBT modules are used. The paper discussed principal sources of voltage transients. Protection schemes that were designed and tested on high current IGBT modules under normal switching operation and fault condition were described.

An RCD clamp circuit was the focus for the over voltage protection during normal switching operation. This low-loss circuit offers effective protection against voltage transients during normal turn-on and turn-off switching.

Voltage transients during fault current shut off are more effectively protected by slowing the rate of fall of fault current. Two novel protection schemes, Resistive and Capacitive techniques, were introduced. These circuits, through electronic gate control, slow the rate of decay of gate voltage, thereby slowing the rate of fall of fault current. Operational characteristics of an active clamp circuit were also discussed in this section. Circuit operations were analyzed and the test results were illustrated.

Appendix I

The expressions 1 to 3 are derived as follows:

At turn-off (see Fig. 2) as one of the two conducting IGBTs is gated off, collector to emitter voltage $v_{ce}(t)$, rises to the DC bus voltage, V_{CC}. Beyond this point, load current freewheels through the diode across the other IGBT. The stray inductances (L_S) however prolong flow of current in the "DC loop". Two components of currents make up for the current i(t) in L_S. They are IGBT turn-off current ($i_C(t)$) and the snubber current ($i_{sn}(t)$), as marked in Fig. 4.

For simplicity of calculations it is assumed that the IGBT turns off "instantly". i.e. $i_{sn}(t)$ is equal to i(t). This assumption is justified on the grounds that it only renders somewhat conservative estimate of snubber capacitor value.

The equations governing various circuit variables are:

$v_{ce}(t) = V_{CC} + 1/C \int i(t)\,dt$

i.e. $V_{CC} - v_{ce}(t) = -1/C \cdot \int i(t)\,dt$ ----------(a)

$v_{ce}(t) = V_{CC} - L \cdot di(t)/dt$

i.e. $di(t)/dt = [V_{CC} - v_{ce}(t)] / L_S$ ----------(b)

From (a) & (b),

$di(t)/dt = -1/L_SC \cdot \int i(t)\,dt$ ----------(c)

The following is the solution to the above equation:

$i(t) = I_0 \cdot \cos(t / \sqrt{L_SC})$ ----------(d)

Where I_0 is the load current at the turn-off. The current is thus a cosine function. In Fig. 4. it can be observed that the combination of $i_C(t)$ and $i_{sn}(t)$ does follow cosine wave shape.

Differentiating (d),

$di(t)/dt = -I_0/L_SC \cdot \sin(t / \sqrt{L_SC})$ ----------(e)

From (b) & (e),

$v_{ce}(t) = V_{CC} + I_0 \cdot \sqrt{L_S/C} \cdot \sin(t / \sqrt{L_SC})$ ----------(f)

v_{ce} is at maximum when $t / \sqrt{L_SC} = \pi/2$.

Therefore,

V_{CM} = maximum desired voltage across IGBT

$V_{CM} = V_{CC} + I_0 \cdot \sqrt{L_S/C}$ ----------(g)

From (g),

Snubber capacitor

$C_{sn} = L_S \cdot I_0^2 / [V_{CM} - V_{CC}]^2$ ----------(1)

The snubber capacitor is therefore charged to V_{CM} at the end of turn-off. Before the next turn-off event, i.e. $1/f_{sw}$ later, C_{sn} should discharge back to its initial value of V_{CC}. The snubber resistor (R_{sn}) selected according to the following expression fulfills above requirement.

$R_{sn} = 1 / (6 \cdot C_{sn} \cdot f_{sw})$ ----------(2)

The losses in R_{sn} at turn-off are therefore given by:

$P_R(off) = [\ ½ \cdot C_{sn} \cdot (V_{pk}^2 - V_{CC}^2)] \cdot f_{sw}$ ----------(f)

At turn-on (see Fig. 8 & 9) as an IGBT is turned on, the switching di(t)/dt causes voltage at module terminals $v_{ab}(t)$ to drop from its initial value of V_{CC} to an amount equal to $L_S \cdot di(t)/dt$. As explained in the article, this causes the snubber capacitors to discharge through R_{sn}s.

For simplicity it is assumed that the turn-on di/dt is linear. It is further assumed that the peak turn-on current is 25% above the load current I_0 at the switching instant. These assumptions will result in conservative estimate of snubber losses.

The snubber discharge current is:

$i_{sn}(t) = [V_{CC} - V_{ab}] / R_{sn}$ ----------(g)

where $V_{ab} = V_{CC} - L_S \cdot di/dt$ ----------(h)

where di/dt (a constant) = $di/dt = .9\ I_0/t_r$ ----------(i)

t_r is the rise time, specified under inductive load conditions. From (g), (h) & (i),

$i_{sn}(t) = I_{sn} = [L_S \cdot 0.9\ I_0 / t_r] / R_{sn}$

$I_{sn} = 0.9 \cdot L_S \cdot I_0 / (t_r \cdot R_{sn})$----------(j)

The losses in R_{sn} at turn-on are,

$P_R(on) = [0.9 \cdot L_S \cdot I_0/(t_r \cdot R_{sn})]^2 \cdot R_{sn} \cdot T \cdot f_{sw}$----------(k)

where T, the snubber discharge time, is approximated to be interval between the beginning of the current rise and the point where current reaches its peak value ($\approx 1.25 I_0$).

$T = 1.25\ I_0/[.9I_0/t_r] = 1.39 t_r$ ----------(l)

Combining (k) & (l),

$P_R(on) = [1.125 \cdot L_S^2 \cdot I_0^2/(t_r \cdot R_{sn})] \cdot f_{sw}$ ----------(m)

From (f) & (m),
The total losses in Snubber resistor are,

$$P_R = [\,½ \cdot C_{sn} \cdot (V_{pk}^2 - V_{CC}^2) + 1.125 \cdot L_s^2 \cdot I_o^2/(t_r \cdot R_{sn})] \cdot f_{sw} \text{ ----------(3)}$$

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