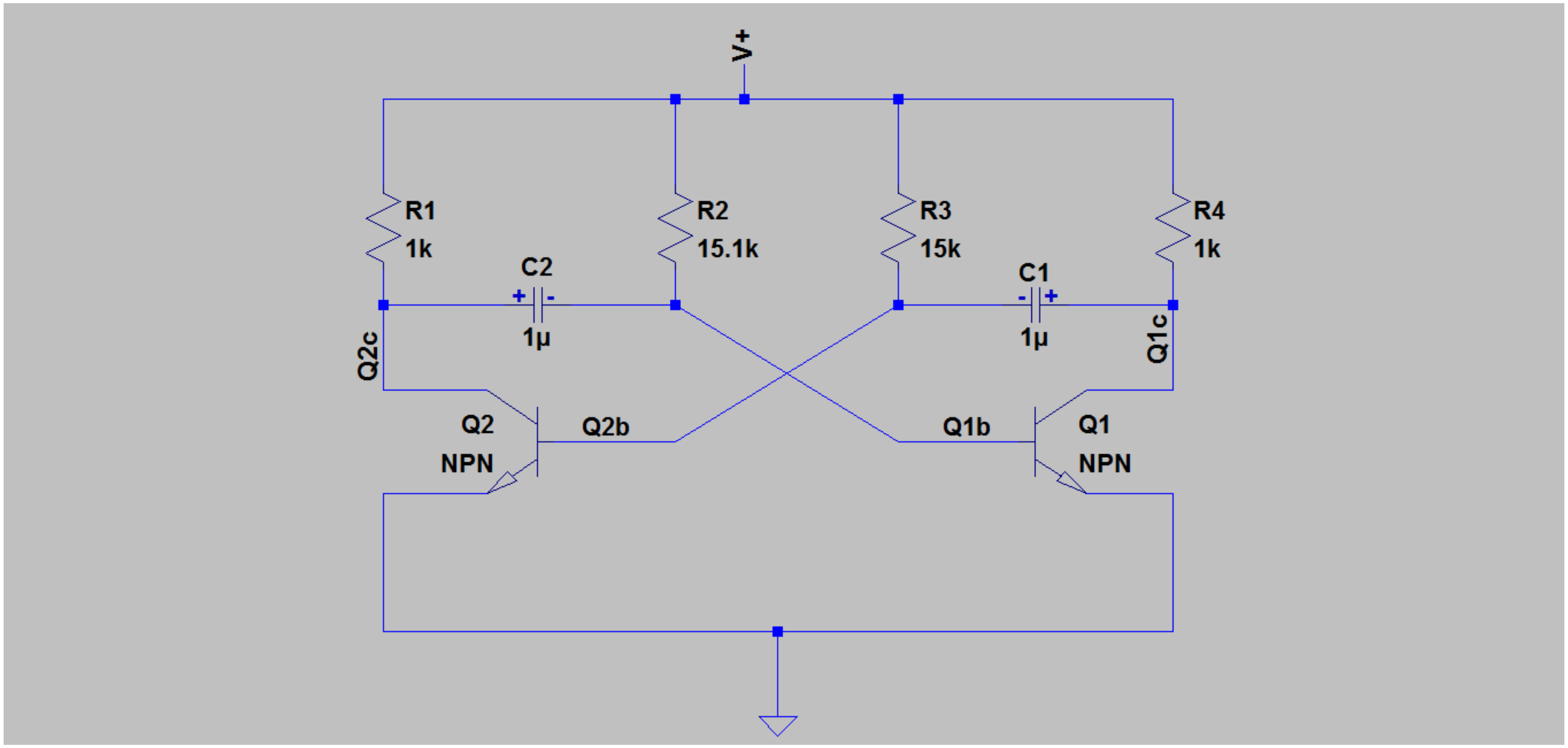
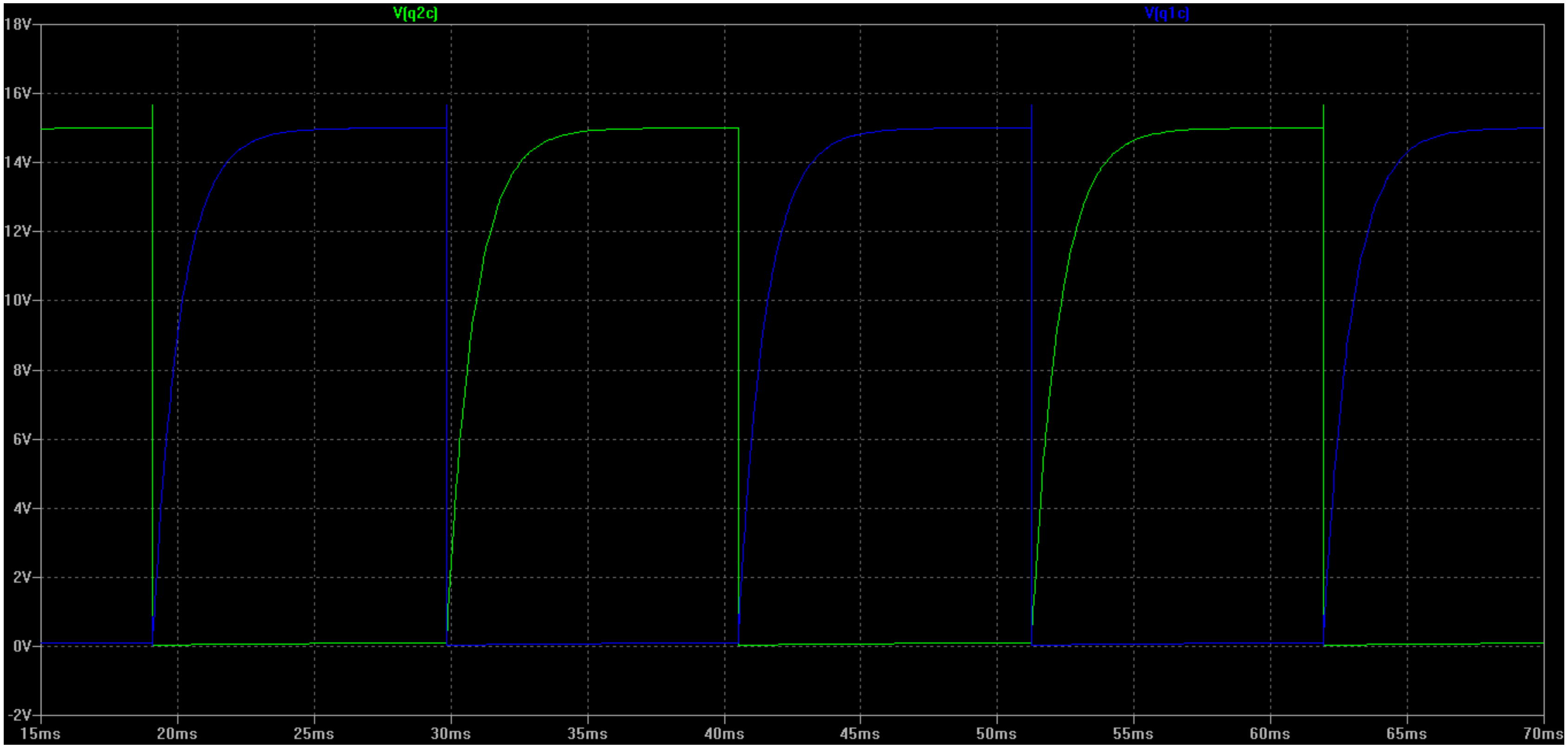


Schematic 1

This is a classic 2 NPN oscillator (Astable Mutlivibrator). The thing to keep in mind is that the left side is identical to the right side. And all the voltage levels are "mirrored" (left vs. right and in time – see below). The very important components are the transistors (Q1 and Q2) and capacitors (C1 and C2). The difference in R2 and R3 values are to make the Spices simulator (LTspice) start to oscillating. Many PERFECTLY balanced analog oscillators will ***not*** start. But in real life circuits no components are perfect and will start automatically.

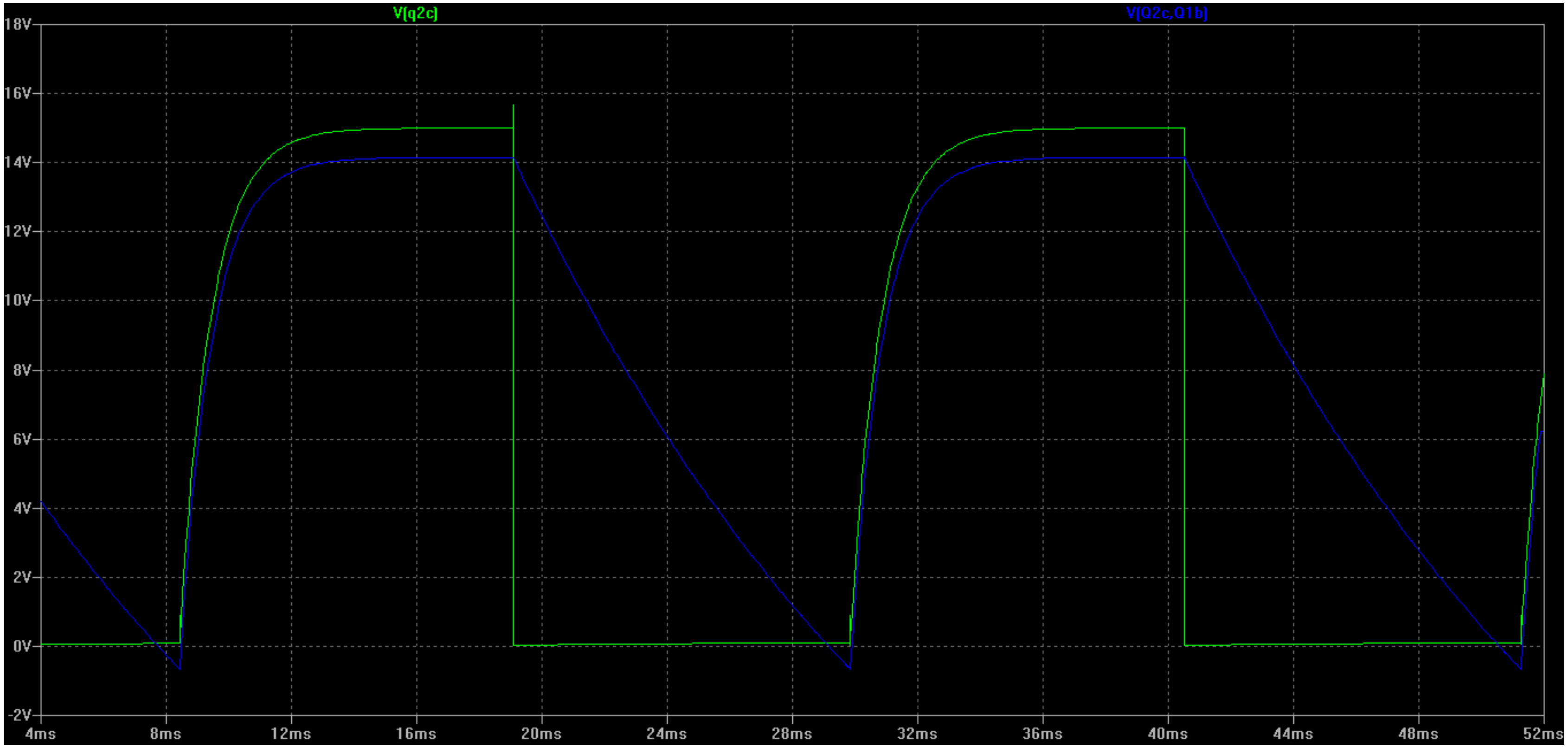
NOTE1: Q2c wire is the same as C2+.
NOTE2: Q1b wires is the same as C2-.



GRAPH 1

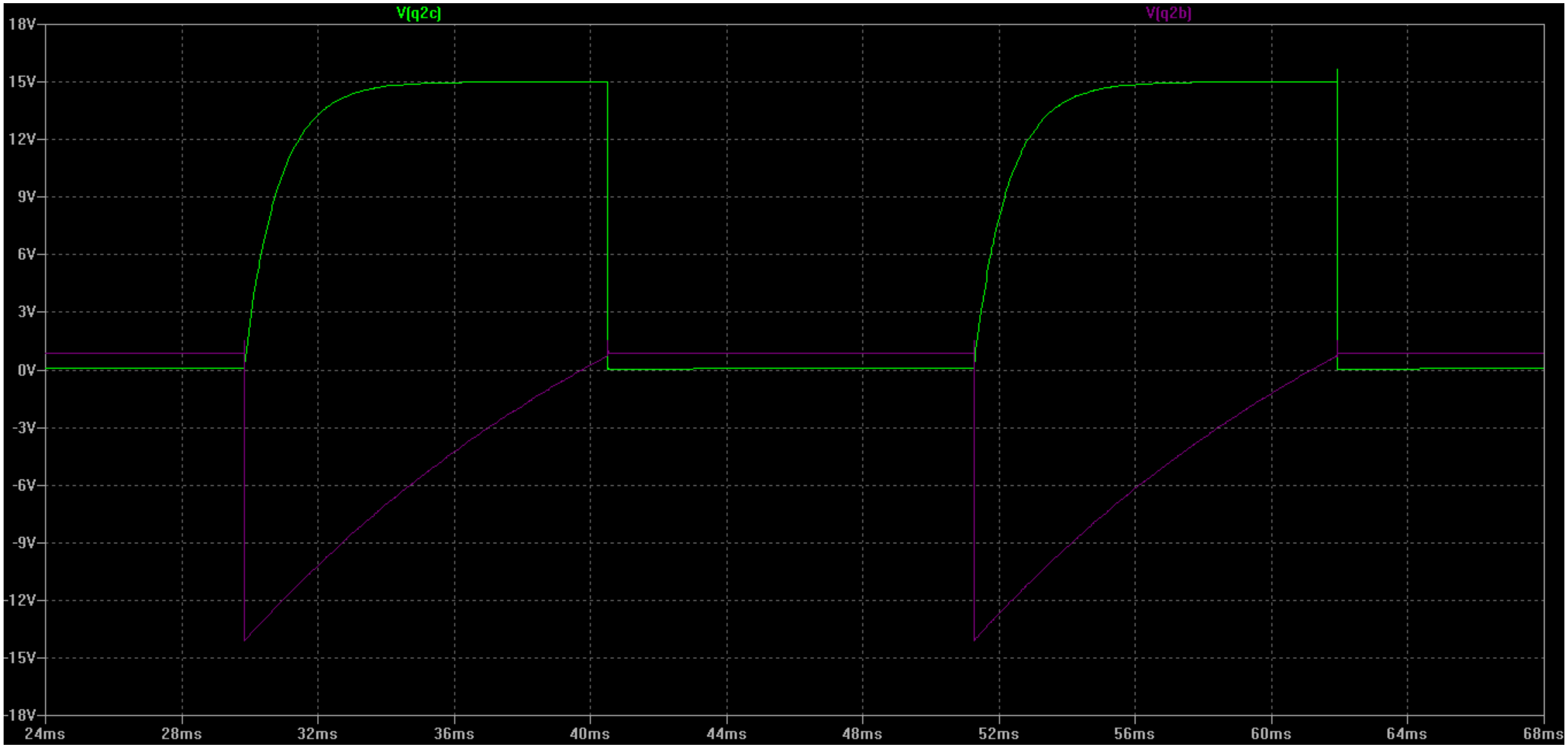
This is the voltage traces at the collectors of Q1 and Q2. Notice they are the same, except when one is ON the other is OFF. When blue trace is held low (Q1 is ON or held down to ground) the green trace is allowed to charge (Q2 is OFF). They are "mirrored" (repeated) in time. So for now we will just discuss only one side for simplicity sakes.

Note: In this circuit when a transistor is turned ON, it conducts and the voltage at collector is actually held ***down*** to ground level.



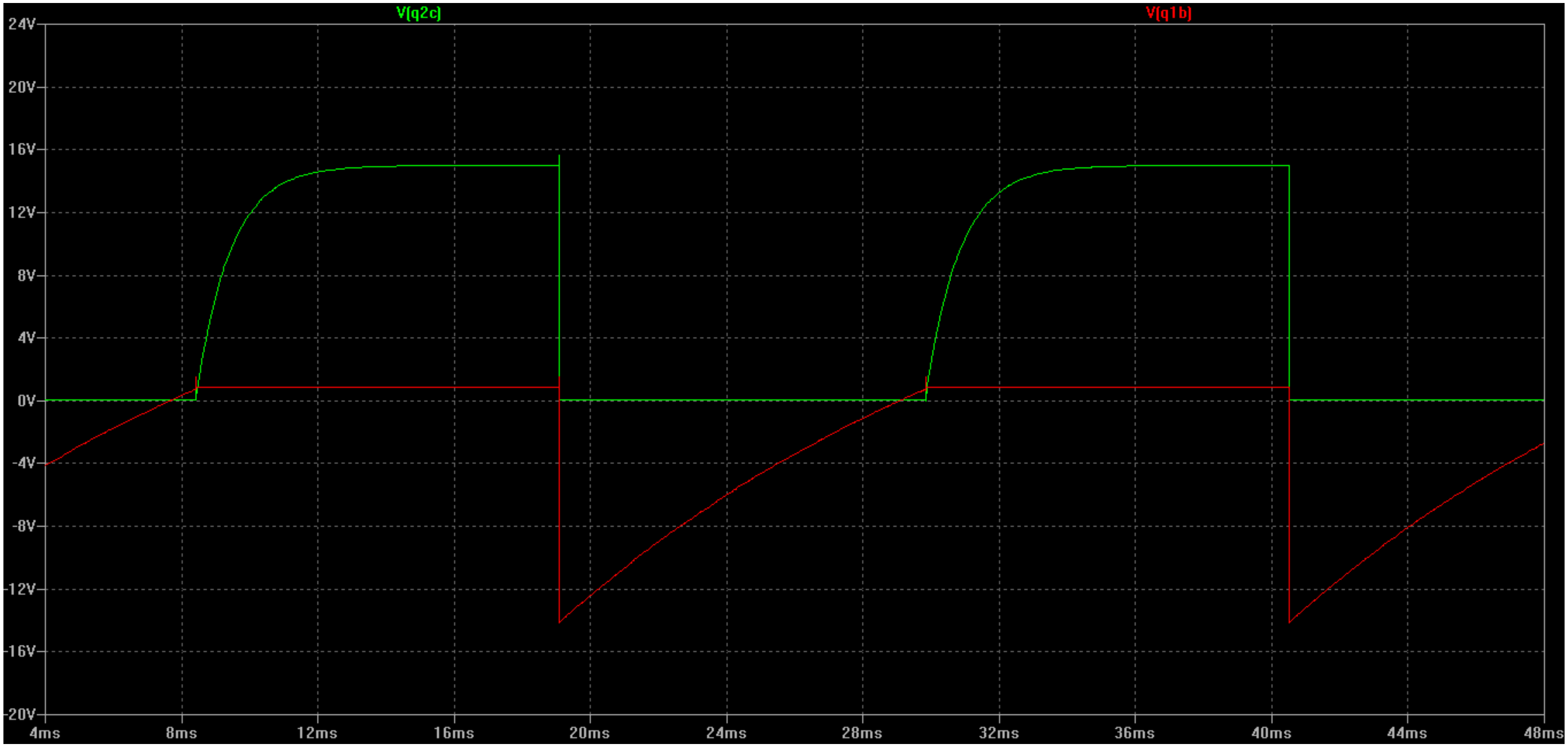
GRAPH 2

The blue trace is ***relative*** voltage across C2. It is important to note that it is relative voltage across C2 (***not*** absolute to ground level). It shows the C2 is charging and discharging in relationship to Q2 collector (green). The green trace is here so you can compare the timing / when things are happening in relationship to each other (also the reason why you need dual trace scope).



GRAPH 3

Notice that the voltage at the ***base*** of Q2 goes negative (violet trace). At this point the Q2 is switched off and C2 is allowed to charge up (green trace). Once the base voltage (violet) reaches about 0.6v, it switches ON Q2 and holds the Q2 collector to ground. The base is not allowed to rise above 0.6v because base voltage of NPN transistor is ***at most*** (approx) 0.6 volts above the NPN transistor's emitter voltage (ground level in this case). I write "*at most*" because it can go negative (as seen in the graph).



GRAPH 4

So why does base voltage go negative? In this graph you can see that as Q2 suddenly conducts and the collector (green) is held down to ground, the other side of C2 (C2- ***or*** Q1b) suddenly goes negative. That's because there's a charge difference C2+ (Q2c) and C2- (Q1b) and that charge just doesn't disappear (see graph 2). This graph shows that as Q2 switches ON, it switches OFF Q1. This is what is happening on the other side also as Q1 and Q2 are identical.

Note: Graph 3 and Graph 4 are identical except that Q2b (purple) is a repeat of Q1b (red), shifted in time. Graph 3 shows base voltage switching the Q2 ON, and Graph 4 shows the same event holding the Q2c to ground, and in turn switching OFF Q1.

I hope you enjoyed this little explanation – Jong Kung.

Additional explanations by the GREAT John Popelish:

Very pretty pictures. My only and temporary confusion was your use of the words "relative voltage of C2" to describe the voltage across C2 (voltage at one end with respect to the other end, while both change voltage with respect to zero). But the LTspice voltage notation for the trace at the top of the graph cleared that up. V(Q2c,Q1b) is collector voltage of Q2 minus the base voltage of Q1, which is the voltage across C2.

NOTE: additional text added to “fix” the confusing text - Jong

Some additional details;

The reason the collector swings go negative very fast, but rise more slowly has to do with both the impedance of the drive side (collector to emitter conduction and pull up resistor) and also the nonlinear character of the load or base side (base emitter diode and base pull up resistor).

When the driving transistor turns on, the transistor is saturated on, so is a very low impedance path to ground, while the base emitter diode on the other side of the timing capacitor is reverse biased, so the only capacitor current path is through the base pull up resistor. So the transistor easily drives a small current through the capacitor and the pull up on the far side of the capacitor and also easily drives current through the lower value collector pull up resistor.
Bam!

Then, while the collector end is held at zero volts by the saturated transistor, the base voltage is climbing from its negative peak toward turn on at about +.6 volts with a time constant of the base pull up resistance times the capacitance. This is slow, because of the relative high base pull up resistance, and produces almost all of the half cycle time.

But when the drive transistor turns off, all there is to raise the voltage on the driven end of the capacitor is the collector pull up resistor, while the base emitter diode on the far side of the capacitor is already right at the point of being forward biased (because that is what caused the drive transistor to turn off, to begin with). So the base voltage cannot go up much at all, without lots of base current passing through the capacitor. While the base diode holds the output end of the capacitor ti about +.6 volts, the collector pull up must charge the capacitor at its RC time constant (collector pull resistance up times capacitance) . That time constant curve is what you see at the collector voltage. If you look at the collector current on another trace, you will see that it is zero the whole time that rise is settling, proving it is not what is shaping the voltage rise. But the base timing that is going on at the other capacitor takes place, almost completely independent of the collector voltage rise time (because it is based on the other transistor holding the driven end of the other capacitor steady at zero volts), so this rounded voltage rise has little effect on the half cycle time.

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Regards,

John Popelish