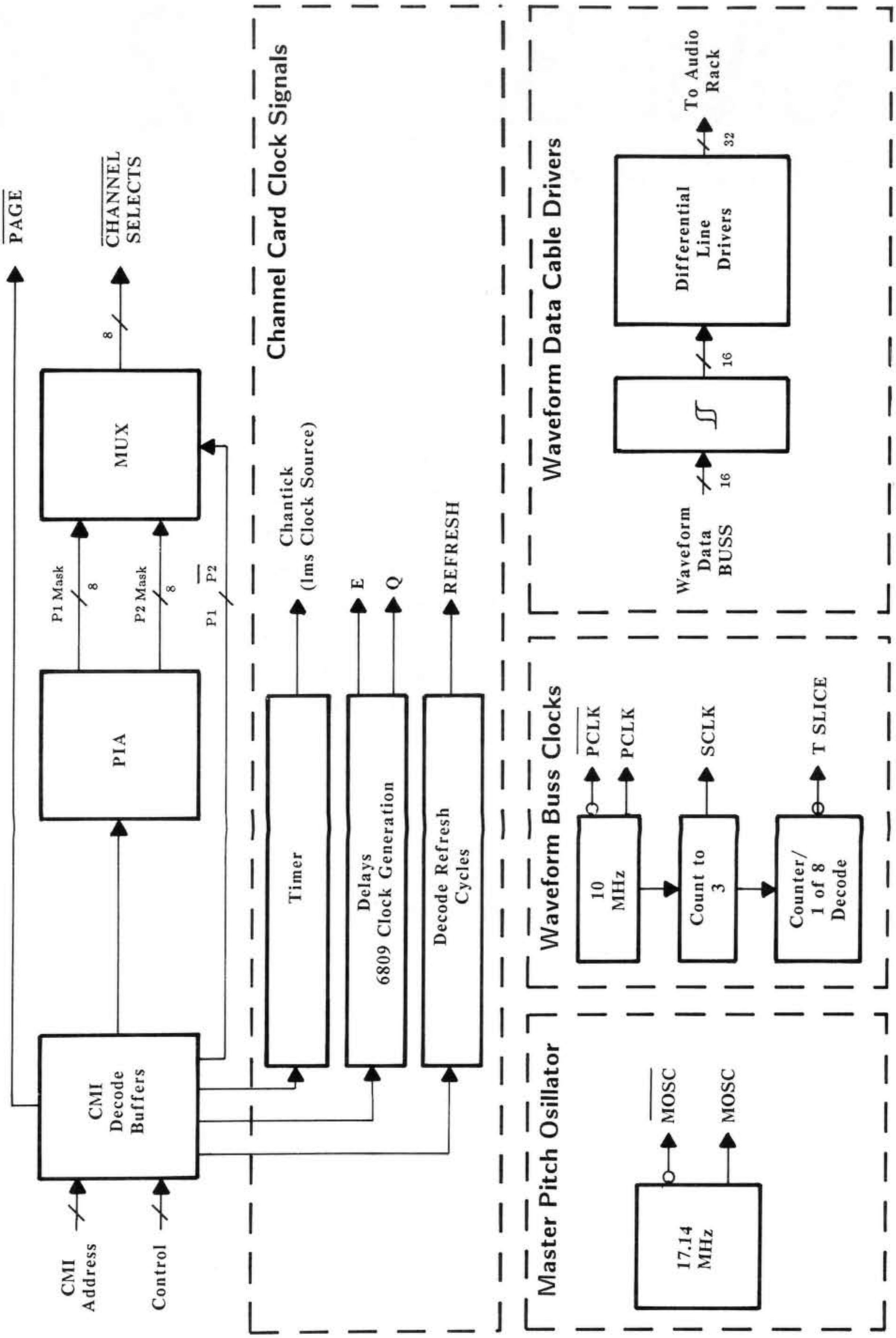
CMI-32 2.10

Channel Support Card


PAGE
CHANNEL SELECTS
8
MUX
P1 Mask
8
P2 Mask
8
P1 P2
PIA
CMI Decode Buffers
CMI Address
Control
Channel Card Clock Signals
Chantick (1ms Clock Source)
E
Q
REFRESH
Timer
Delays 6809 Clock Generation
Decode Refresh Cycles
Waveform Data Cable Drivers
To Audio Rack
32
Differential Line Drivers
16
16
Waveform Data BUSS
Waveform Buss Clocks
PCLK
PCLK
SCLK
T SLICE
10 MHz
Count to 3
Counter/ 1 of 8 Decode
Master Pitch Osillator
MOSC
MOSC
17.14 MHz

Introduction

The Channel Support Card (CSC) provides the main timing signals for the control of the Waveform buss, Waveform Processor and Channel cards. It also contains the data drivers to connect the Waveform data buss to the audio board DACs. These functions are independent of each other.

Channel Card Access and Control

The Channel Cards (CCs) are accessed from the dual CPU buss via the CSC. The CSC decodes the dual CPU busses upper address lines to form CC select lines. The CCs may be accessed either individually to set their control registers or selectively simultaniously to their memory. This is done so that common data may be written to more than one channel cards memory at once.

The channel mask, that allows simultanious access, contains a bit for each channel card. Channels with their mask bit set, will be accessed when a device on the dual buss accesses the locations for the channel cards. As there are 2 distinct and independent buss states on the dual buss, there are two mask registers, called MASK1 and MASK2.

The CSC also generates the 2Mhz E and Q signals that the 6809E requires. These signals are generated externally so that the CCs on board proccessor is syncronized with the dual CPU buss. This is required to make all external accesses to the channel card transparent to the on board 68B09Es.

Waveform Buss Control

The timing of the Waveform Buss (WBUSS) is dependent on just one signal, SCLK, Slice Clock. This divides the WBUSS into 300nsec slices to be shared between the WP, CCs and refresh. It is used by the WRAM, WP and CCs.

Waveform Buss access by Channel Cards

The Channel cards are allowed access to the WBUSS in a "round robin" fashion. The WBUSS is divided into 8 300nsec time slices. The signal TSLICE defines the first slice in the sequence and is input into CC number 1, the most right hand CC. Each CC forms a bit in a shift register that passes this TSLICE signal to the next CC. Thus allowing them on SCLK cycle every 8 to access the WBUSS.

Address decoding and Masks

(refer schematic CMI-32-00)

Address lines MA8 to MA15 are buffered and gated with VMA and Peripheral enable, ENBL, to generate the card select at B2 pin 9. Decoder B3 and OR gates in A1 decode for the timer, Pia, CC register selects and CC memory page select. The Page select signal is qualifierd by BRA at B10 to drive all the CCs.

The multiplexers at C7 and B7 select the Mask register appropriate to the current buss cycle. This is achieved by routing the adress phase signal, ADD1, to the select input of C7 and B7, pin 1.

The multiplexer outputs are ANDed with the outputs of decoder A7, after which they are qualified by latch A10, and bussed to the Channel cards. A7 decodes address lines MA4 to MA6 to generate the 8 selects for the register mode access on the 16 byte boundaries required.

The enable for C7 and B7 can be generated under two conditions. When the Channel registers are accessed via the mask, and when the channels memory is accessed, always by the mask. Hence the AND gate driving the enable, pin 15, of C7 and B7.

Timing Generation

(refer schematic CMI-32-01 and timing diagram)

The 2Mhz E signals is generated by ORing buss signals RA and RAS. The Q signal is E delayed by 125ns by a delay line.

Because of the delays involved in multiplexing internal buss signals on the CCs, the CCs require a $\overline{RAS}$ signal delayed by 25ns with respect to the equivalent RA buss signal. This is also generated by a delay line, and bussed to all CCs.

Refresh for the CCs and the WBUSS is synchronized to system refresh by detecting when the first device on the P1 DMA daisy chain requests the CMI buss. This is done by gating REFEN, ADD1 and ACK1 with F/F C1 and NAND gate C2. This generates an active high pulse 500ns long every 16 microseconds, during the P1 refresh cycle.

The master pitch oscillator for all the channel card pitch generation, is based around the 34MHz crystal and transistor Q2. This is divided by 2 and driven to all channel cards via the differential line drivers in D6.

The WBUSS timing chain starts with the 20MHz crystal and transistor Q1. This is divided by two and bussed to the WBUSS via differential line drives.

SCLK is generated in D1 which is a counter that counts to 3. It is bussed to the WBUSS via a buffer in A11 and series resistor R42. R42 cuts down the ringing and undershoot, on the bussed line.

SCLK is then fed to counter E1 to generate the inputs to the 1 of 8 decoder E2. This generates the TSLICE signal used in buss arbitration by the CCs. It goes low once every 8 SCLKs.

Timer Mask Registers

(refer schematic CMI-32-03)

The 6840 is used to generate a real time clock interupt to all the channel cards via its counter 1. This results in a 1KHz square wave on pin 27 of the 6840.

The PIA is used for the MASK registers as it allows the current MASK value to be read by the software.

Bidirectional Data buffer buffers the CMI data buss to the 6840 and 6821 only.

The latches B4 and B10 hold the addresses and 6840, 6821 chip select signals across the data phase of the CMI buss.

Data cable drivers

(refer schematic CMI-32-04)

The WBUSS data is buffered in schmitt receivers A8 and A9 and feed to the differential line driver devices, MC3487, and then to the 34 way IDC socket. The most significant bit of the data is inverted by the connections to E10 pins 13 and 14, to allow the data in WRAM to be 2's compliment and the audio DACs to be offset binary. The data is differential to evade corruption of the 3.3MHz data stream.

Channel Card Addressing
Via the MASK
Channels may be accessed via the channel mask at $E091 to $E093. The mask registers are the two sides of the PIA. A channel is selected when its mask bit is set to 1. Bit 0 is channel 1, bit 7 is channel 8.

$E080	channel cards via mask
$E090	6821 Channel Mask PIA base address
MASK1	A side is P1 mask
MASK2	B side is P2 mask

There is no hardware to stop reading from multiple channels .
DO NOT READ WITH THE MASK WITH MORE THAN ONE CHANNEL SELECTED.

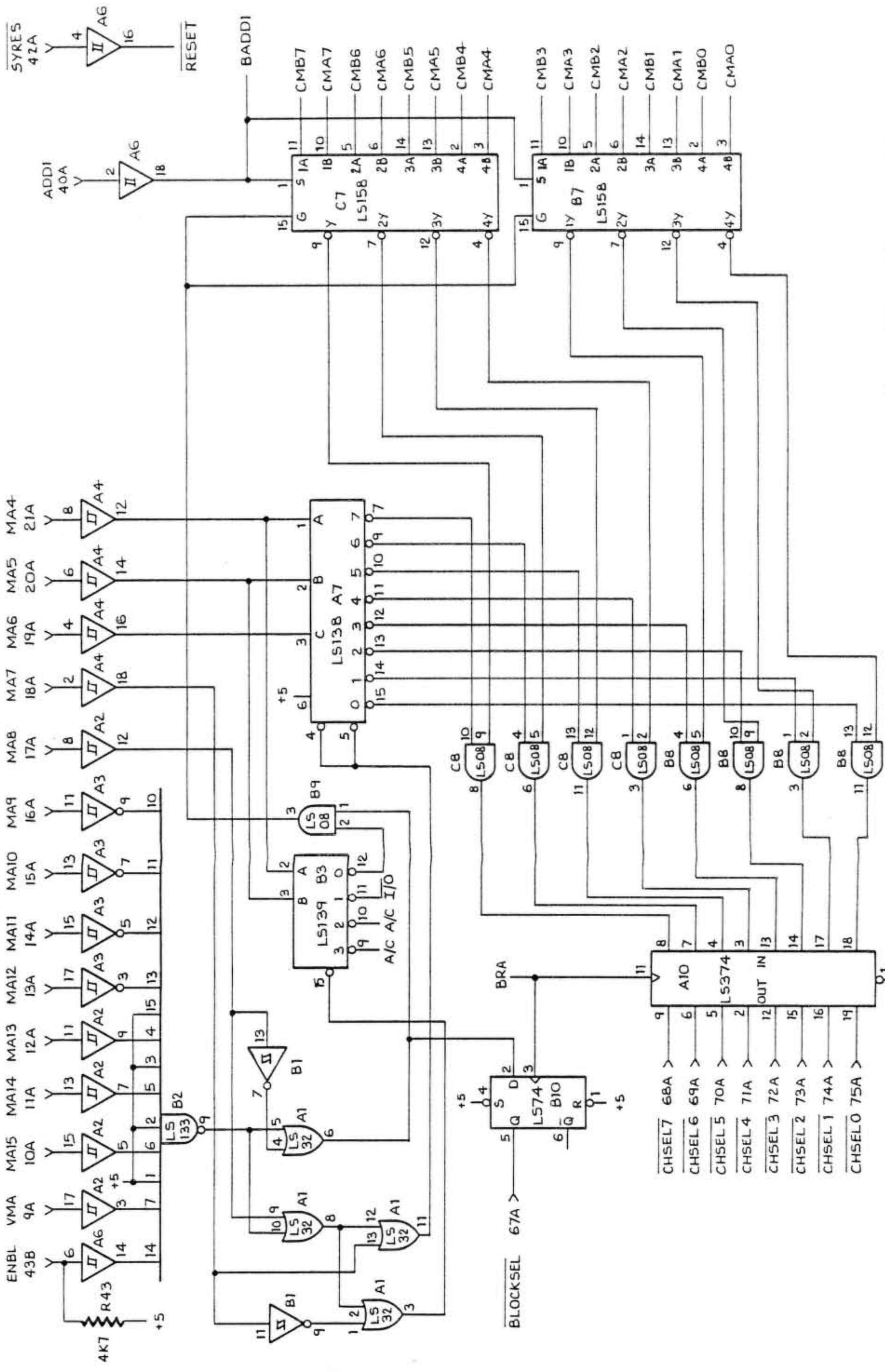
Direct Channel Card Register Access
The channel cards registers may also be accessed individually with the cards having the following base addresses.

$E000	channel card 1
$E010	channel card 2
$E020	channel card 3
$E030	channel card 4
$E040	channel card 5
$E050	channel card 6
$E060	channel card 7
$E070	channel card 8

Channel Card Memory Access
The channel cards 64k memories are accessed in 256 byte PAGEs.
The PAGE to be accessed is written to the register in the channel card, one register for P1, another for P2.
The upper 8 bits of address of the channel cards page registers are used as the upper address bits of the accessed location. The lower 8 bits of the LD or ST instructions address determines the byte within the block.

$E100 to $E1FF Page of Channel Memory

Timer
Timer 1 has its output bussed to all channel cards for its real time clock. Timer 1 is set to run continously at 1KHz. This results in channel card ramps being updated at 1ms intervals. Timer 2 has its input connected to the 1 MHz ADD1 buss signal. Timer 3 has no input or outputs connected. The 6840's IRQ output is connected to an interrupt input on the CPU Control Card.



Decoding Channel Masks

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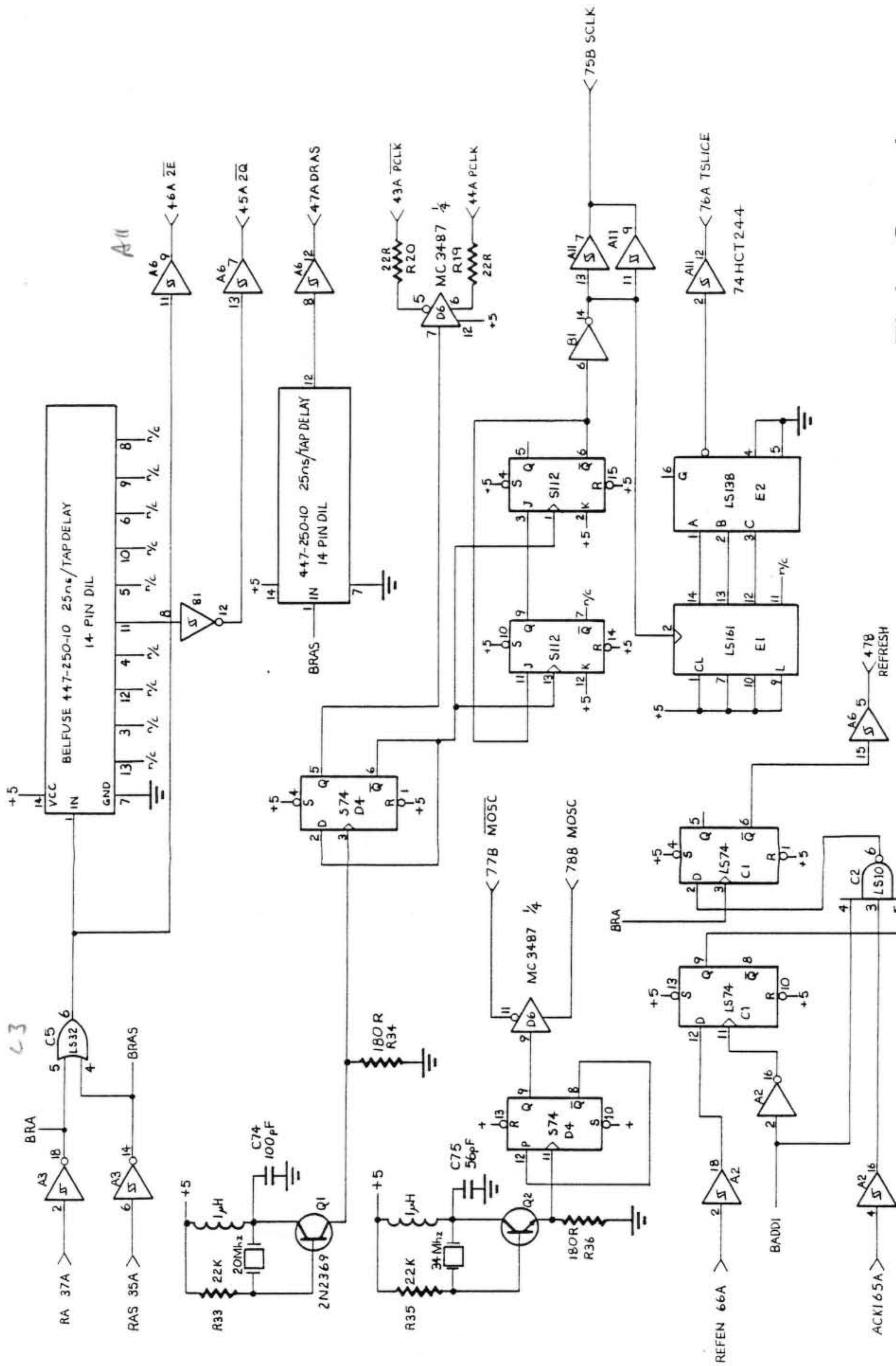

Timing Generation

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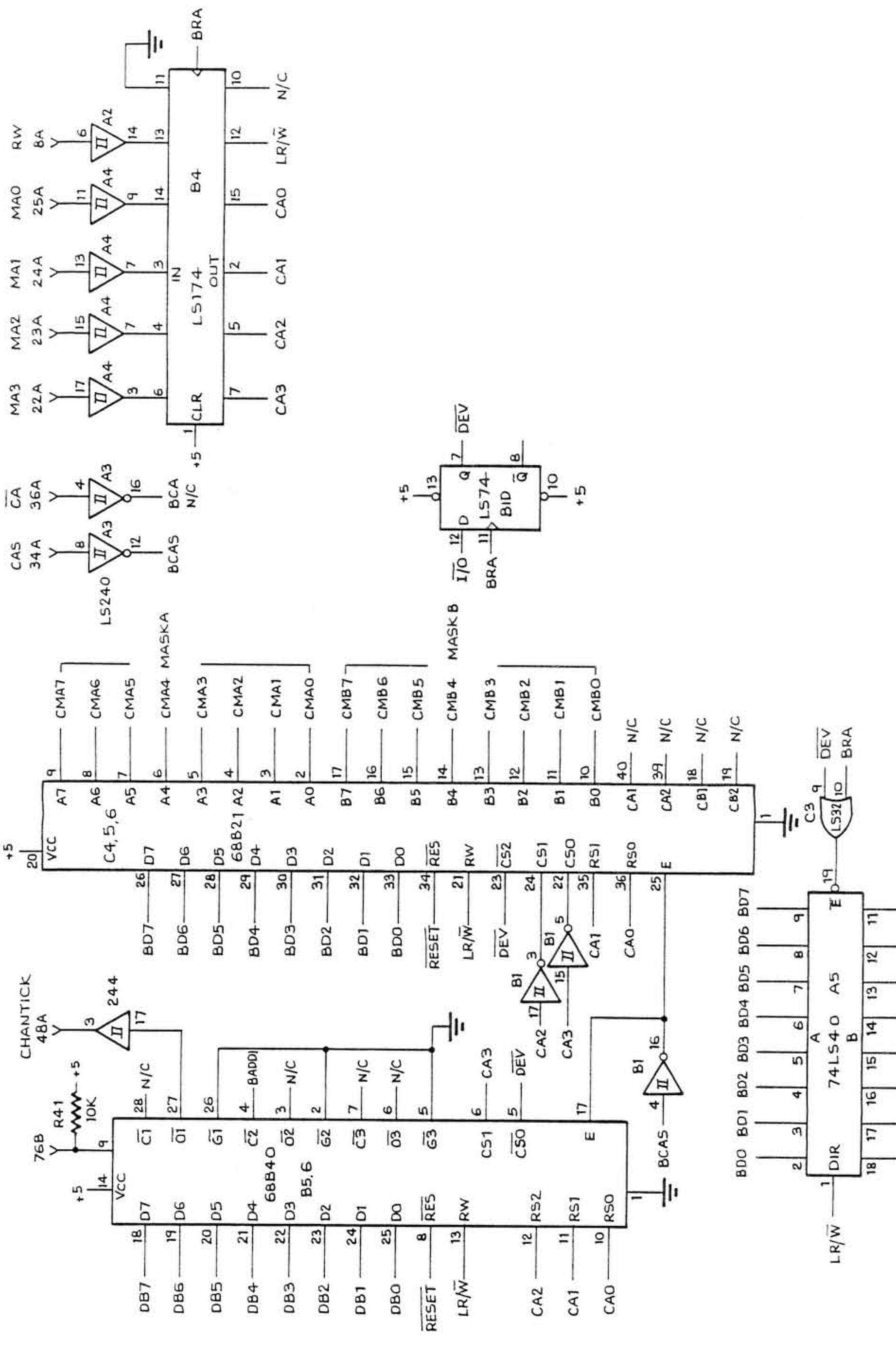

Timer, Mask Registers

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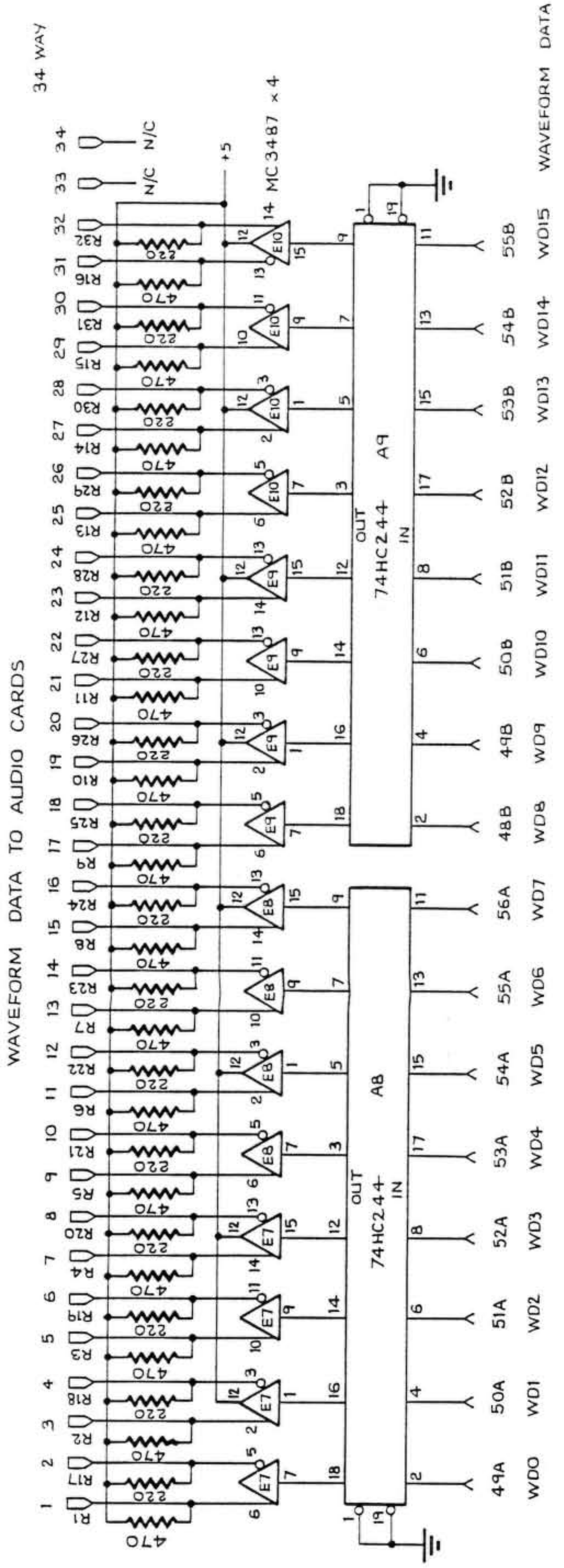

Data Cable Drivers

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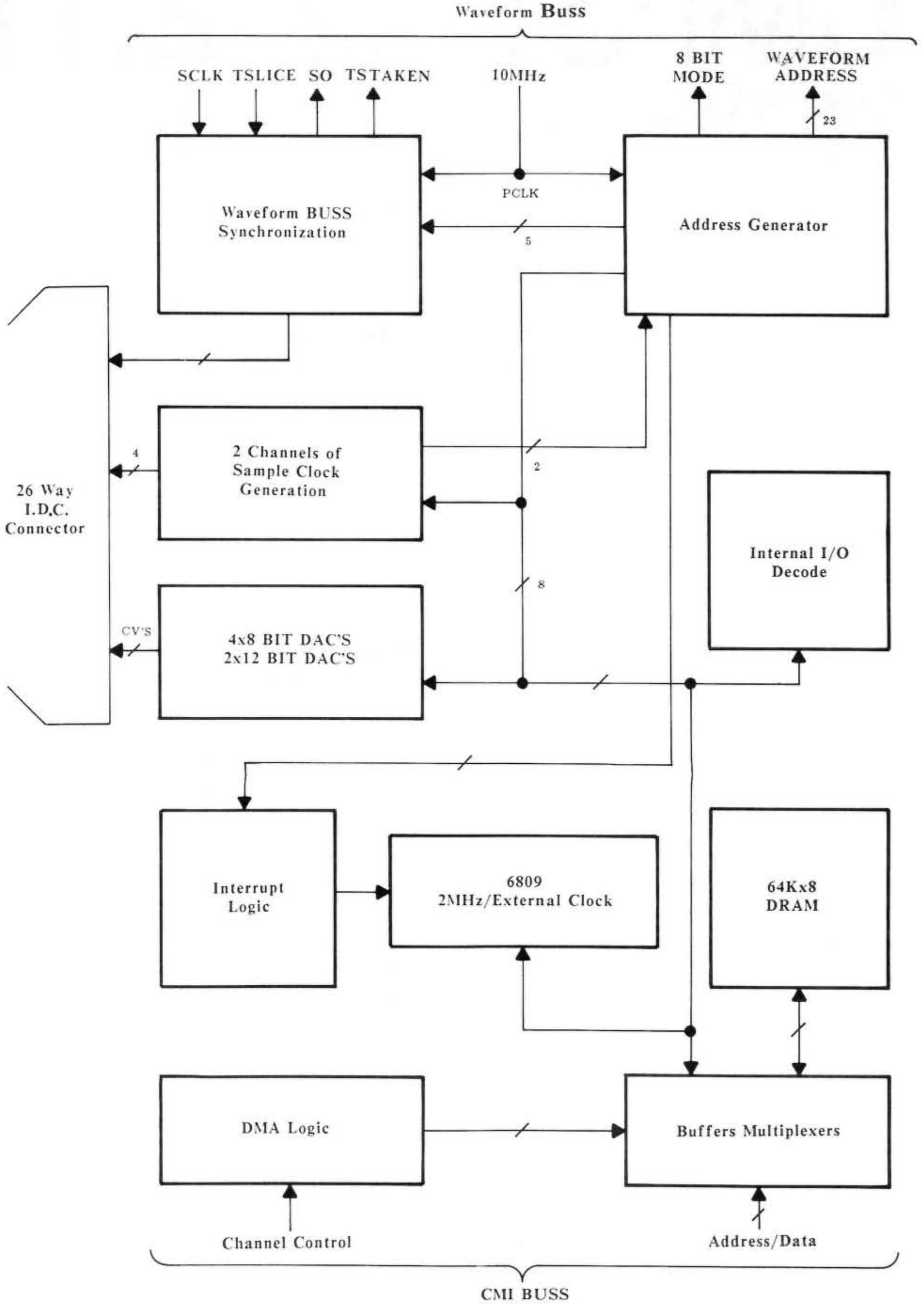
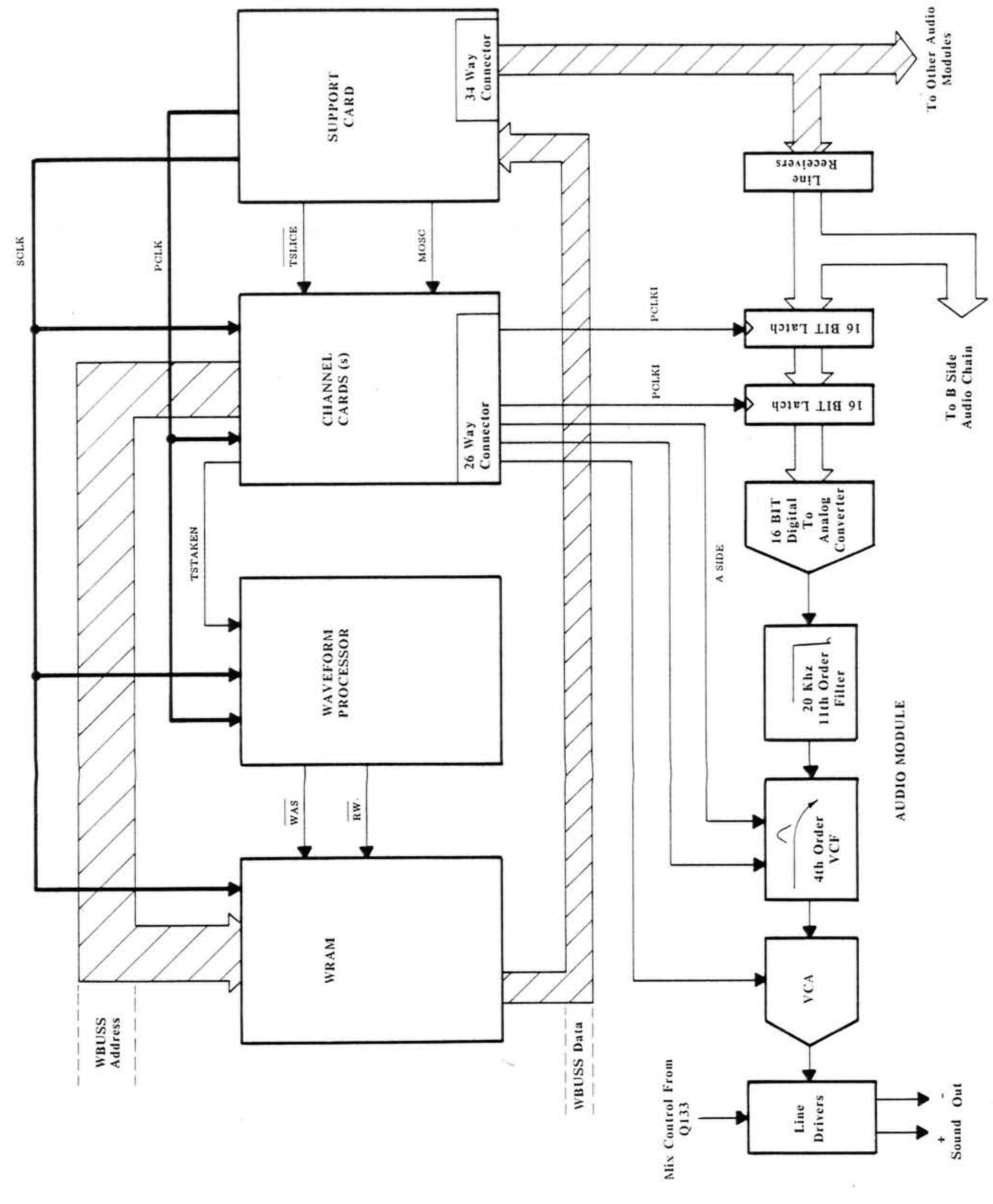
CMI-31 2.11
Channel Card

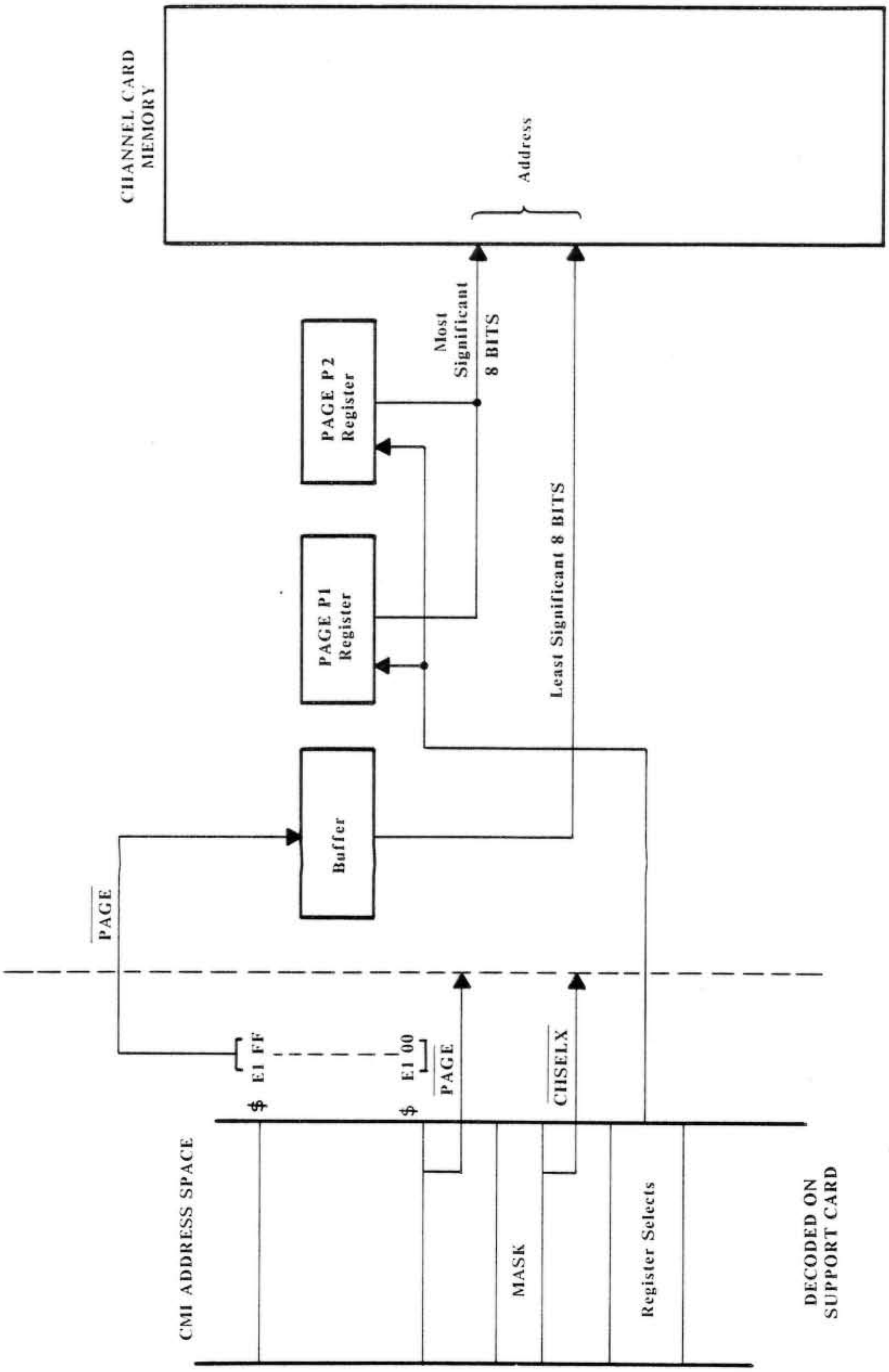
Channel Card Block Diagram



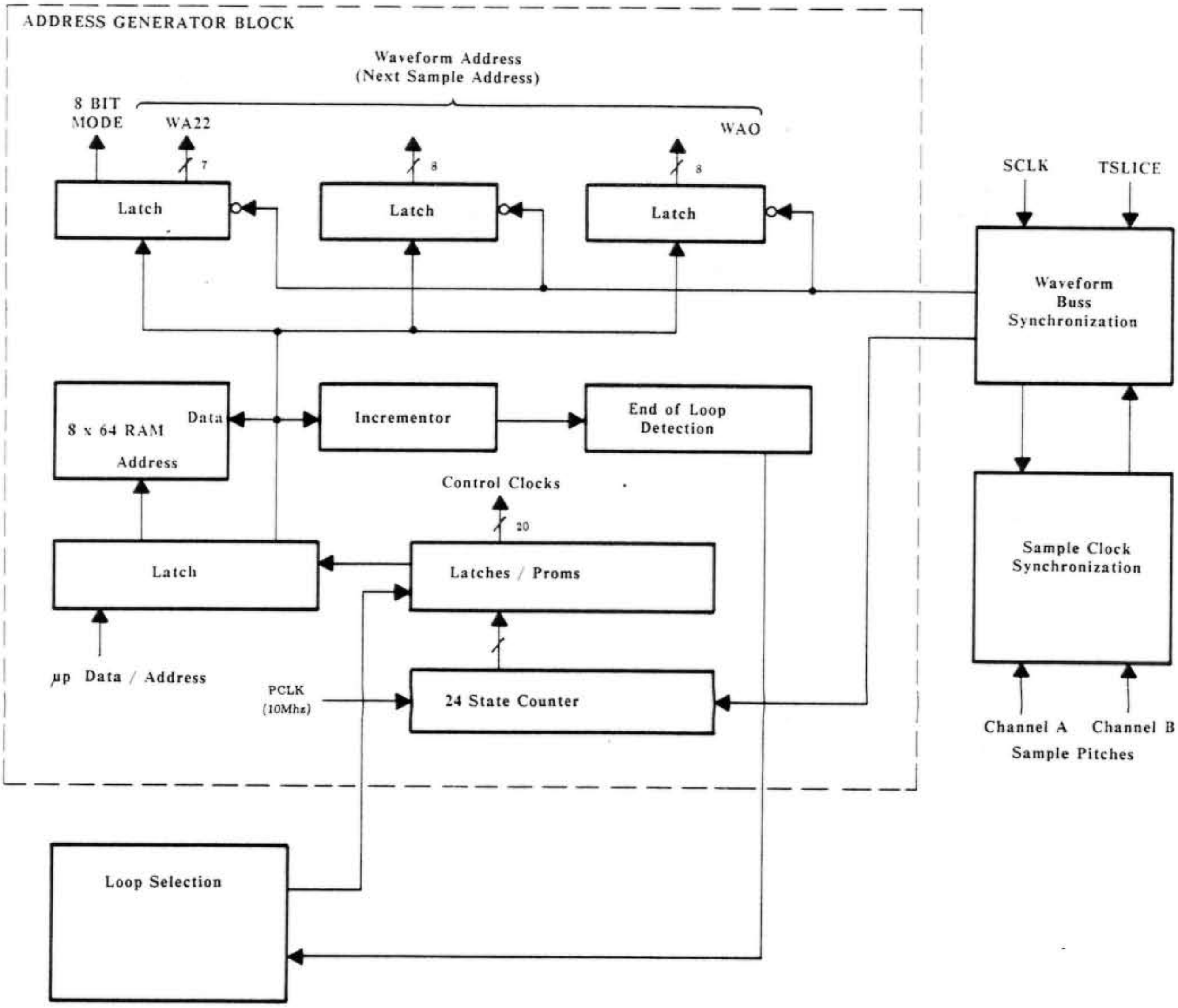
Important Modules during Sound Playing



Memory Access Block Diagram



Address Generator Block Diagram



Terminology
WP: Waveform Processor
GIC: General Interface Card
WBuss: Waveform Buss
WRAM: Waveform RAM (2M - 14Mbytes)
CC: Channel Card
CCP: Channel Card Processor
CSC: Channel Support Card
CPU: Dual 6809 processor system running OS9.
Hexidecimal numbers are in the form nnnnnnH.
Active low signal names are preceded by a "/" character

Introduction

The Channel Card (CC) provides the sample addresses, sample clocks and control voltages used in outputing data to the Audio Modules and controlling the resulting audio waveforms amplitude and high frequency content. It carries on these functions as a self contained computer, once instructed what functions to perform by the WP, GIC or CPU.

The CC can be divided into 2 main sections. The control of the 6809 and its memory by the main CPUs through the CPU buss interface, and the on board 6809s I/O, which generates signals for the WBUSS and the Audio Rack.

Channel Control

The CC contains a 2MHz 68B09E and 64K of dynamic ram. To the main CPUs it looks like a block of 16 registers and two pages of 256 bytes of memory, mapped into its peripheral space.

The generation of the CC select signals occurs on the CMI-32, Channel Support Card (CSC).

The CCs registers allow the main CPUs to reset and interrupt the on board 68B09E and select which two pages of memory are mapped into the main CPUs address space.

All accesses to the CCs registers and memory are made transparently to the Channel Card Processor (CCP) by cycle stealing. This allows the fastest update of control parameters with the minimum overhead.

Refresh also steals one cycle every 16 microseconds from the CCP.

Channel Card Peripherals

The CCP initializes and controls the sample address and clock generating hardware collectively referred to as the Address Generator (ADDGEN). It also addresses 6 DACs used to generate control voltages used in the control of the Voltage Controlled Filters (VCF) and the Voltage Controlled Amplifiers (VCA) on the Audio Modules.

Waveform Buss Interface.

CCs are allowed access to the WBUSS in a "round robin" buss sharing scheme. The CCs internally share their WBUSS grant between the two audio channels contained on each CC.

The ADDGEN is granted access to the WBUSS via the CSCs buss arbitration signal, TSLICE. During active CC WBUSS cycles, the WP is informed via TSTAKEN that it or refresh cannot access the WBUSS.

Processor, Address Registers and Multipexers
(refer schematic CMI-31-01)

The CPU's data buss is buffered at A6 to form the internal Memory Data Buss (MDB). The CCPs data buss is connected to the MDB via bidirectional buffer B8. All onboard RAM access occurs via the MDB. B8 is only disabled during CC access by external CPUs, during ram refresh and when the CCP accesses the ADDGEN and DACs. The buss between B8 and the CCP is the peripheral buss (PB) and is where the DACs and ADDGEN are connected. External CPU data cannot get onto the PB from the MDB, and hence control the ADDGEN.

The MDB also connects to the octal latches at A8 and A7 which are the PAGE registers used in external access to the CC's RAM. Latch A7 contains the page address for P1, A8 for P2.

The addresses from the CCP, via buffers B6 and B7, the page registers, and buffer B5 (connected to the least significant 8 bits of the dual CPU buss) all connect together to form the 8 bit address buss for the dynamic RAMs.

During refresh cycles, the least significant 7 bits of the CPU address buss contain the contents of the refresh counter from the CMI-133. During CC memory accesses by external CPUs, the least significant 8 bits of the CMI address buss contains the address within the page to be accessed. The Buffer B5 is enabled during these memory cycles to form the row address for the RAMs.

When the CC is accessed, the two card select control signals, $\overline{\text{CHSEL}}$ and $\overline{\text{PAGE}}$ become active. The channel select is buffered and ANDed with the refresh signal in D9, which in turn is ANDed with the externally generated E and Q to feed the CCP. During refresh and external accesses, the CCP has its clock stopped (D9 pin 11 low), allowing a memory cycle for refreshing and updating of memory or registers.

Address Decoding
(refer schematic CMI-31-02)

The CCs control registers are decoded from the CPU buss by 1 of 8 decoder C3. It is enabled when the channels $\overline{\text{CHSEL}}$ is low and $\overline{\text{PAGE}}$ is high. From this decoder the external CPU can read the channels run status, reset the CCP, write to the PAGE registers and interrupt the CCP. The CCP loses one cycle for each access.

The LS133 at C6 decodes the CCP address buss to define the ADDGEN and DAC I/O locations.

The CCPs I/O is decoded in 2 64 byte blocks starting at FE80H. The first block contains the control latch, pitch registers, CCPs interupt status register, real time clock acknowledge and DACs. The second decodes the ADDGEN registers.

Whenever these I/O loactions are accessed, pin 9 of C6 will go low and disable the CCP's MDB transiever.

Channel B Pitch and Card Status Register
(refer schematic CMI-31-03)

The latches at E5 and E6 contain the pitch for the B audio channel. There are 3 bits to select which octave and 12 bits to select the pitch within the octave. The pitch within the octave bits feed Rate Multipliers at F6 and F5.

The Rate multipliers are clocked at 17.14 MHz. The output of this chain is pin 6 of F6. This is a train of pulses with an average frequency of the required pitch, but in a much higher octave. This clock has considerable jitter as the rate multipliers effectively drop clock pulses from the 17.14 MHz stream to change frequency.

This clock feeds a binary counter E3 that generates the clocks for 8 octaves, at 16 times the required sample rate. The 1 of 8 selector E4 uses the octave select bits to select the appropriate output of E3.

The selector feeds a divide by 16 counter which acts as a jitter filter, to average out the periods of the sample clock, to reduce distortion in the output waveform.

The output of the jitter filter, E9, is ANDed with the RUNB control signal to generate the sample clock for channel B.

The 4 bit latch and buffer at B11 and A11, are used by the external CPUs to determine the current status of the channel card. The upper 4 bits of this register allow the external CPUs to determine if an interrupt came from this channel card, that the CCP is reset, and if either of the two audio channels controlled by this card are currently being used.

The least significant 4 bits allow the CCP to send 4 bit status codes to the external CPUs.

Channel A Pitch and the control registers
(refer schematic CMI-31-04)

The pitch generation for channel A is identical to Channel B but uses the components at E8, E7, F8, F7, D6, D5 and E9.

The main pitch oscillator is bussed from the CSC as a differenti-al line. This is received at A9 by a 26LS32. This receiver then drives the two channels of pitch generating ratemultipliers.

The control latch is located at C10. This octal latch outputs all the control lines to control, channel running, zippa filter time constant, enabling of end of loop interupts and selection of the ADDGENs loops. It is reset when the CMI is turned on to stop the channels running, and making any sound before they are initialized.

The F/F at D2 is used to control the $\overline{\text{RESET}}$ input of the CCP. It can only be written to by external CPUs and is reset, the CCP stopped, at power on.

Control Voltage Generation
(refer schematic CMI-31-05)

The Control Voltage DACs all use a precision 10.000V source as their voltage reference. The +15V, -15V and analog ground (AGND) are cabled to the CCs via 26 way flat cables. There is no connection between the CCs digital ground DGND and AGND on the CC. They are connected together in the Audio Rack. The back to back diodes and resistor on the CC connecting DGND and AGND are to stop the two from drifting too far apart if the AGND and DGND connection is broken.

The DACs cannot be accessed by external CPUs, only the CCP.

The AD7226 at F3 is a quad 8 bit voltage output DAC. It receives the 2 least significant address lines to select its 4 DACs on byte boundaries. This DAC produces 2 channels of filter cutoff and resonance Control Voltage (CV). Each is 0 to 10 volts.

The filter cutoff frequency range is from 20Hz to 20kHz with control values of 0V (00H) to 10V (FFH).
The filter resonance changes from flat, 0V (00H) to oscilation at 10V (FFH).

The AD7548s at F1 and F2 are 12 bit, right justified DACs with an 8 bit buss interface. They are connected so that the 16 bit value written to them is only latched into the 12 bit DAC after pin 15, DACOUT, is accessed as a seperate operation. The output of the current to voltage converters is a CV with the range 0 to -10 Volts. The control range is approximately 95db. 0V (X000H) is maximum attenuation. -10V (XFFFH) is no attenuation, 0db.

When a sound is being played out, its amplitude control voltage will be updated every 1ms and thus the DAC should be accessed at that rate.

These CVs have a software selectable time constant or "zippa filter" .This allows for fast attacks on envelopes and "quiet " amplitude control at other times. This is selected by the SATA and SATB control latch outputs.

Program Ram And Address control
(refer schematic CMI-31-06)

The 64k of DRAM and the address multiplexors are controlled from the PAPLA, (Page Addressing Programable Logic Array). The PAPLA has as inputs CPU buss signals and the 2 CC select signals. The DRAMs require 16 address lines and to get these into the 16 pin package they are latched internally and use an external 8 bit buss and 2 latching strobes, refered to as Row Address Strobe (/RAS) and Column address strobe (/CAS). The $\overline{\text{CAS}}$ signal also doubles as the data enable strobe. Refer to the Memory data books for exact details.

Because of the propagation delay in the PAL, the Row Address Strobe for the RAMs must be delayed in time with respect to the buss RAS signal. This is done on the CSC to generate ABRAS.

Depending on the state of the PAPLA inputs, it will enable to the DRAM's address inputs , the CCPs addresses, P1 PAGE register and the least significant bits of the external address buss, P2 PAGE register and the least significant bits of the external address buss, or the refresh address from the external address buss.

When there are no external accesses or refresh, then the CCPs address is enabled to the RAM.

$\overline{\text{CAS}}$ to the RAMs is disabled whenever an external access to the CCs control registers occurs.
RAM refreshes use dummy reads from the current refresh address.

Address Generator and Control

(refer schematics CMI-31-07,08, Address Generator and Control Signals)

The address generator (ADDGEN) calculates the sample addresses when playing out waveform ram. It calculates 24 bits of waveform address for the 2 audio channels on the card.

The ADDGEN's 24 bit output is interpreted as 23 bits of address and a "mode" bit by the WRAM. The most significant bit is used to select 8 or 16 bit sounds, and must be set accordingly when issuing loop start addresses.

Each audio channel has 2 loops associated with it. Each loop is initialized with a start address and a loop length, in samples. Two loops are needed to allow the contents of one loop to be played while the other is being initialized.

This allows such things as playing the sound in segments that are not sequential. The switching from one loop to the other only occurs at the end of the loop.

The hardware that generates the 24 bit addresses for the waveform does so 8 bits at a time. The machine is basically a small 8 bit wide RAM, B13 and B14, incrementer, B11 and B12 and logic to generate the sequence of clock and enable signals to do the required operations. The sequence of clocks results in operations on 24 bit numbers of load, store, NOP and add 1.

To do a 24 bit increment with this hardware the following sequence must be performed.

The least significant byte is loaded into the incrementer and incremented by one, by enabling the count input of the counter and clocking the counter. The ripple carry out (RCO) of the incrementer is clocked into a F/F to determine if the counter overflowed. This incremented byte is then written back to its original RAM location.

The middle byte is then loaded into the incrementer. The output of the F/F that clocked the RCO from the first byte increment is then fed into the count enable input of the incrementer and the counter clocked. This byte will only be incremented if the least significant byte overflowed. The RCO from the incrementer is then clocked into another F/F and the middle byte written back to its original RAM location.

The most significant byte is then loaded into the incrementer. The outputs of the two RCO F/Fs are ANDed together and feed into the count enable input of the incrementer, and the counter is clocked. The most significant byte will only be clocked if the middle and least significant bytes overflowed. The most significant byte is then written back to its original location.

Address increments, however, are syncronized to the channnels pitch clocks. This means that not all cycles allocated to incrementing the addresses, actually result in the address being incremented. A signal syncronizing the pitches to the ADDGEN hardware disables the incrementing of the address bytes on unused address calculation cylces.

The following is a general outline of the address calculation sequence for one channel.

```
while power applied
do
  write 24 bit waveform address to address latches A14,A12,A13

      if end of loop flag is 1, F13
        then
            reset loop counter to start
            value and clear end of loop flag
        else
           inc loop counter

      end

      if end of loop
        then
            reset wave address to start
            value and set end of loop flag
        else
            inc wave address
            clear end of loop flag
      end
end
```

Address Generator Clock generation

The state counters are E14 and E13. They are made to count to 24 by being reset after 24 clock cycles by the waveform buss syncronization logic, via signal $\overline{\text{SRES}}$. The output of the counters go to the address inputs of the control PROMS, at D14, D15 and D13. These Bipolar PROMS contain the clock and address sequences needed to control the clocking and enabling of the ADDGEN hardware. The PROM outputs are deglitched by the octal latches on their outputs, C14, C15 and C13. There are 15 clock signals generated by the clock generating PROMs. There are 6 address bits generated by the ADDGEN PROM and loop select and channel select lines.

Pitch Clock Synchronization

The sequence of F/Fs and multiplexer at F9, F11 and F15 syncronize the incrementing of waveform addresses to the rising edges of the pitch clocks. The calculation of the next sample address is carried out by the address generator on the next cycle allocated to that calculation after the rising edge of that channels pitch clock. The result is that COUNTEN goes active for one cycle.

The COUNTEN signal is used to enable the increment operation. The ADDGEN is normally going through the sequence that does the address calculations, but nothing in fact is incremented because of the inactive COUNTEN signal.

Active COUNTEN will also pull the TSTAKEN (time slice taken) active and inform the WBUSS control logic on the Waveform Processor that the next waveform memory cycle will be used by a CC.

At the end of the memory cycle the channel card will also generate the clock to clock data into the Audio Rack, via the DCLK1, DCLK2 and PCLK1, PLCK2.

The operations performed in each clock cycle are:-

0 read WADDRESS1 write to output latch 1
1 read WADDRESS2 write to output latch 2
2 read WADDRESS3 write to output latch 3

	if endofloopflag set	if no endofloopflag
3	read looplenght1	read WORDCOUNT1
4	nop	inc
5	write WORDCOUNT1	write WORDCOUNT1
6	read looplength2	read WORDCOUNT2
7	nop	inc
8	write WORDCOUNT2	write WORDCOUNT2
9	read looplength3	read WORDCOUNT3
10	nop	inc
11	write WORDCOUNT3	write WORDCOUNT3

12 nop

The end of loop F/F is set here if the end of a loop has been reached. It is clear otherwise.

	if end of loop then set endloopflag	if not end of loop clear endloopflag
13	read STARTLOOP1	read WADDRESS1
14	nop	inc
15	write WADDRESS1	write WADDRESS1
16	read STARTLOOP2	read WADDRESS2
17	nop	inc
18	write WADDRESS2	write WADDRESS2
19	read STARTLOOP3	read WADDRESS3
20	nop	inc
21	write WADDRESS3	write WADDRESS3

22 write to control ram from proccessor

23 nop

The parameters are organized in the ADDGEN ram so that changing the upper two address lines to the ram, makes the ADDGEN calculate values for the other channel or the other loop.

The current loop for channel A and B is set in F/F C16 by the CCP. These F/F are set to loop1 whenever the channel is stopped.

The end of loop flags, F13, are also set when a channel is stopped. This is done because the only time the loop values are initialized is when an end of loop occurs.

When the CCP writes the loop values to the ADDGEN ram, the CCP's data and least significant 6 bits of address are latched at C11 and C12. This has to be done because the write cycle for the CCP last for 500ns while that for the ADDGEN lasts 100ns. The ADDGEN and the CCP are also not synchronized, so the CCP's data is latched until the ADDGEN is able to write it to its RAM, which happens every 2.4 microseconds. When the write to ADDGEN ram occurs, the latch containing the CCP's address (C12) is enabled instead of the addresses from the ADDGEN PROM (C13).

The 20 test pins are used to connect a logic analyser to the ADDGEN machine for debugging,

Waveform Buss Syncronization

(refer schematic CMI-31-09)

The WBUSS is controlled by the SCLK signal. The Channel cards take turns in using the WBUSS by only using the cycle following an active TSLICE signal on their TSLICE input. Each card uses half of F/F F14 as a bit in a shift register that is shifted left on each rising edge of SCLK. So that only one CC has an active TSLICE signal at a time.

The current channel being calculated by the ADDGEN is determined by half of G15. The other half of G15 is used to steer the data clock to the correct audio channel on the audio board.

CCs only use their allocated WBUSS slice, if COUNTEN is valid. If a WBUSS cycle is granted and COUNTEN is active then TSTAKEN and ATB will be generated as will the DCLKs to the Audio rack.

This will result in a read from Waveform RAM and the data being clocked into the first set of latches on the audio board for the apropriate channel. The WP generates the read and waveform address strobe signal, to the RAM on receiving the TSTAKEN signal from the channel card.

The gated sample clocks are cabled to the Audio Rack via differentian lines.

Channel Card Processor Interupts

(refer schematic CMI-31-10)

The "chantick" from the 6840 on the Channel Card Support is used to provide a real time clock reference to all channel cards. This is an FIRQ to the channel card processors at the 1 msec rate set by the CSC. The FIRQ is used to time the VCA (and VCF) ramp generating software. The rising edge of chantick sets half of F/F E1 which causes an FIRQ to the CCP. This is the only source of FIRQ on the card. The CCP resets this F/F in its interupt service routine by accessing the RTC location.

The CC can interrupt the CMI by accessing its /$\overline{ACK}$ location which will reset F/F D2. This interupt will be reset when the CMI reads the CC's status register.

There are 3 sources of IRQ on the CC to the CCP. They are the interrupt from the CMI, the end of loop interupt from channel A and the end of loop interupt from channel B. Because of this, a status register is required to determine the source of the IRQ. This is half of the buffer at A5. Valid interupts are cleared when the status register is read. Shortly after the status read pulse occurs, pin 8 of E1 will go low briefly. This will reset the interupt F/Fs D1 and half of F10, that were valid before the previos CCP cycle. This double buffering of interupts is to stop interupts from being lost, if they occurred during the status register read.

Channel Card Equates and Definitions
Addressing from external CPUs.
The hardware equates for the card are:-

CNTRL	EQU	2	0= reset CCP
STAT	EQU	0	processor interupt and status byte
PAG2	EQU	5	Page of CC RAM to be accessed by P2
PAG1	EQU	6	Page of CC RAM to be accessed by P1
ATT	EQU	A	access to interupt CCP

STAT bit definitions

0	command bit
1	"
2	"
3	"
4	RUNB
5	RUNA state
6	channel card processor reset line
7	active interupt from this channel card

Support card Mask related equates

CHANS	EQU	E080	access channels via the masks
CHAN1	EQU	E000	direct access to channel 1
CHAN2	EQU	E010	"
CHAN3	EQU	E020	"
CHAN4	EQU	E030	"
CHAN5	EQU	E040	"
CHAN6	EQU	E050	"
CHAN7	EQU	E060	"
CHAN8	EQU	E070	direct access to channel 8

On board Processor's I/O

The Channel Card Processors equates

Control voltage DACs

AFILT	EQU	FE80	8 bit filter cutoff channel A
BFILT	EQU	FE82	8 bit filter cutoff channel B
ARES	EQU	FE81	8 bit filter Q at cutoff
BRES	EQU	FE83	8 bit filter Q at cutoff
AVOL	EQU	FE85	12 bit right justified
BVOL	EQU	FE89	12 bit right justified
DACOUT	EQU	FE8C	access to output above two to DACs

Rate multipliers

APITCH	EQU	FE90	15 bits, right justified
BPITCH	EQU	FE92	15 bits, right justified

Control latch

CNTRL EQU FE8E

0	channel B loop select 0= loop 1
1	channel A loop select 0= loop 1
2	enable end of loop channel B IRQ
3	enable end of loop channel A IRQ
4	volume zipper noise filter B (1= on)
5	volume zipper noise filter A (1= on)
6	run channel B
7	run channel A

Address Generator

Each location is write only and each byte must be written no faster than every 2.4 microseconds

All are 24 bit values, stored least significant byte first.

The most significant bit of the start addresses determine 8 or 16 bit accesses

0 = 8 bit

1 = 16 bit

ASTRT1	EQU	FEC0	start address channel A loop 1
ALOOP1	EQU	FEC3	length loop 1 channel A
ASTRT2	EQU	FED0	start address channel A loop 2
ALOOP2	EQU	FED3	length loop 2 channel A
BSTRT1	EQU	FEE0	start address channel B loop 1
BLOOP1	EQU	FEE3	length loop 1 channel B
BSTRT2	EQU	FEF0	start address channel B loop 2
BLOOP2	EQU	FEF3	length loop 2 channel B

Communications Interrupts

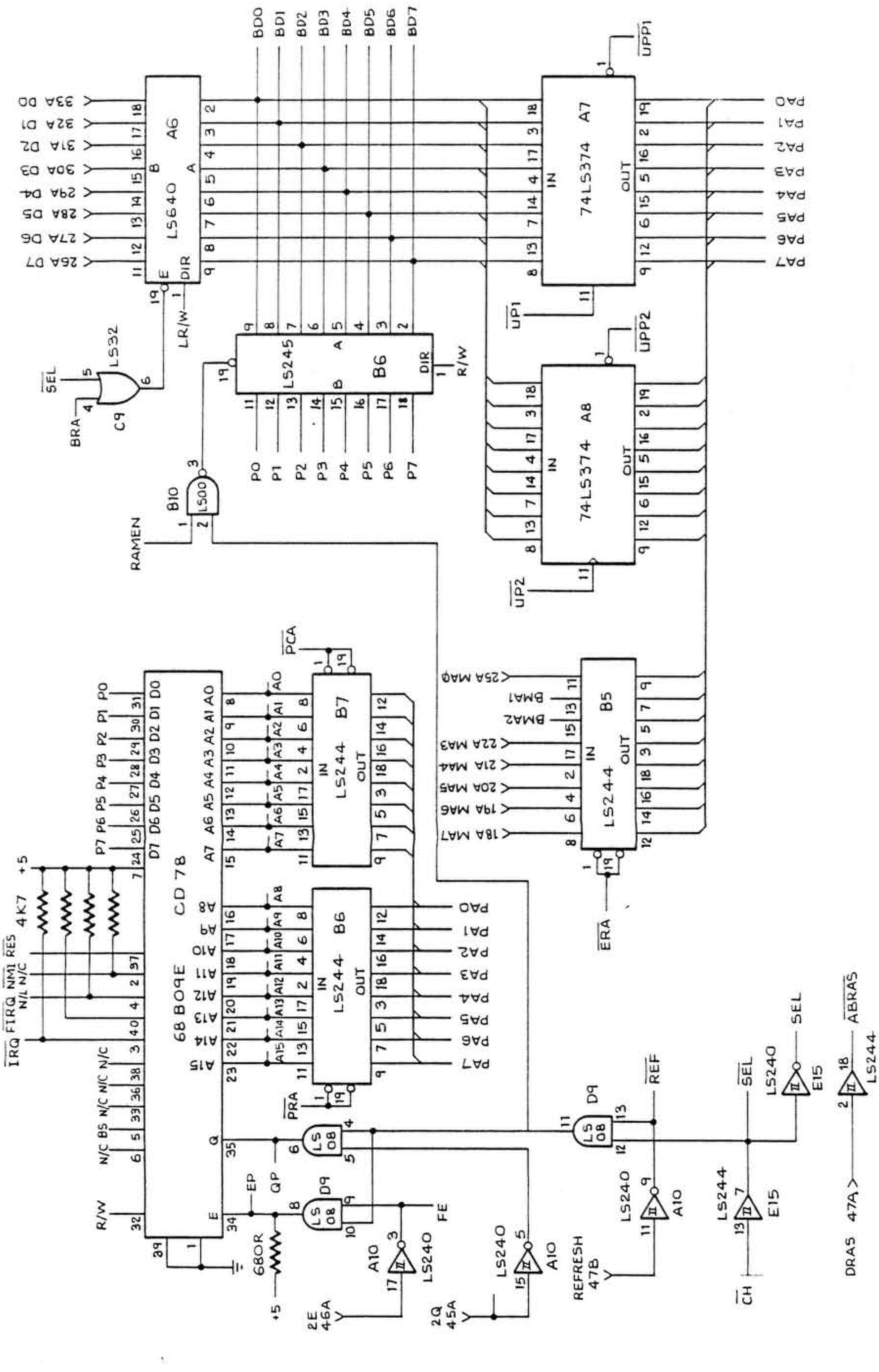
```
COM    EQU    FE96   read or write to interrupt CMI

STAT   EQU    FE97   read for interrupt status
*      Bit definitions
*      4      chantick happened
*      5      end of loop B  interrupt happened
*      6      end of loop A  interrupt happened
*      7      command interrupt happened

RTC    EQU    FE94   access to reset real time FIRQ
```

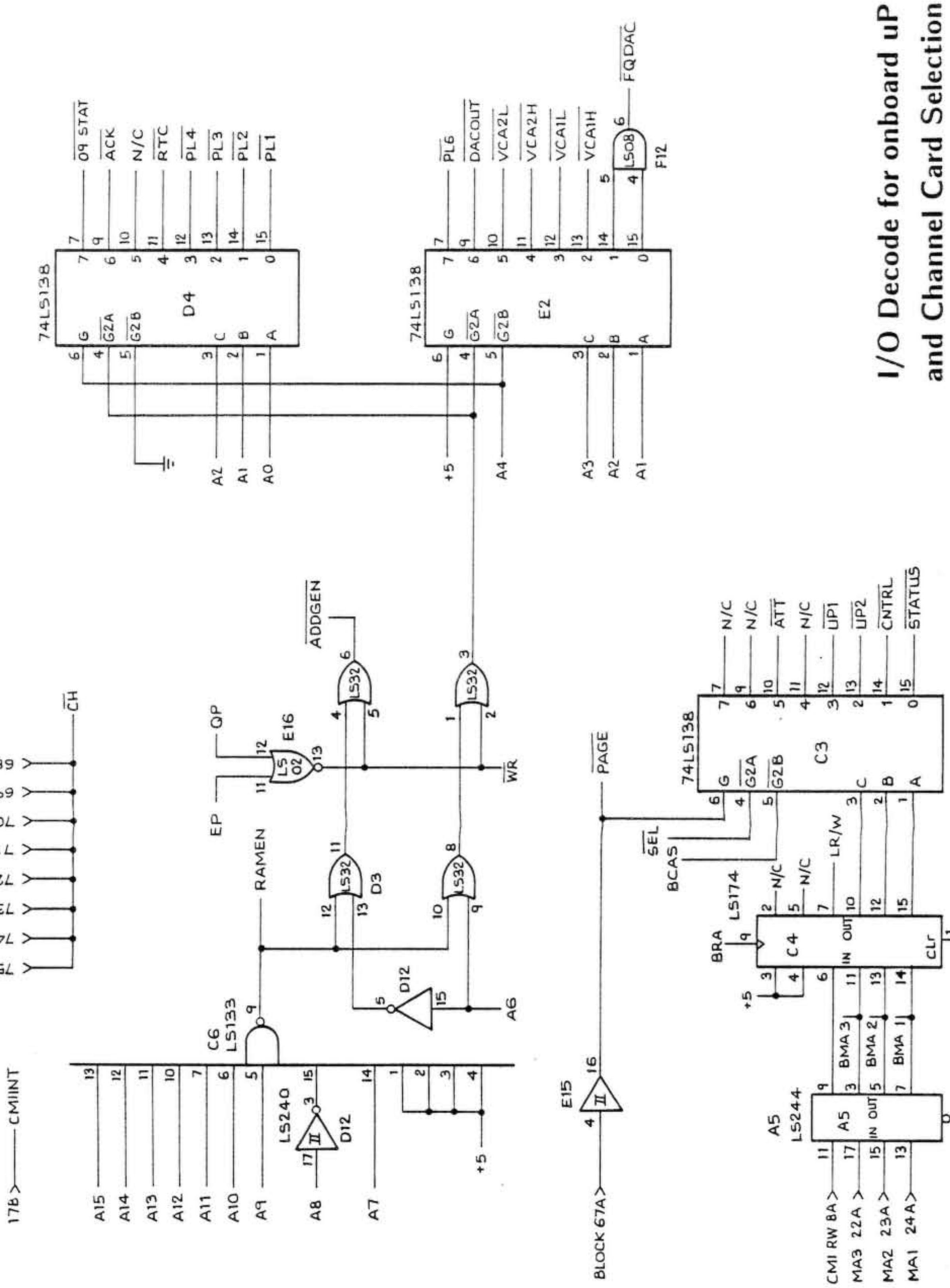
Address Generator 64 Byte RAM Organization.
Unlabeled locations are unused.

	Channel A		Channel B
0	start loop1 lsb	20	start loop1 lsb
1	" mb	21	" mb
2	" msb	22	" msb
3	loop length 1 lsb	23	loop length 1 lsb
4	" mb	24	" mb
5	" msb	25	" msb
6	word count 1 lsb	26	word count 1 lsb
7	" mb	27	" mb
8	" msb	28	" msb
9	waddress lsb	29	waddress lsb
A	" mb	2A	" mb
B	" msb	2B	" msb
C		2C	
D		2D	
E		2E	
F		2F	
10	start loop 2 lsb	30	start loop 2 lsb
11	" mb	31	" mb
12	" msb	32	" msb
13	loop length 2 lsb	33	loop length 2 lsb
14	" mb	34	" lsb
15	" msb	35	" msb
16		36	
17		37	
18		38	
19		39	
1A		3A	
1B		3B	
1C		3C	
1D		3D	
1E		3E	
1F		3F	



Processor, Data Buffers, and Pointer Registers

DRAWN: AB REVISION: 1



I/O Decode for onboard uP and Channel Card Selection

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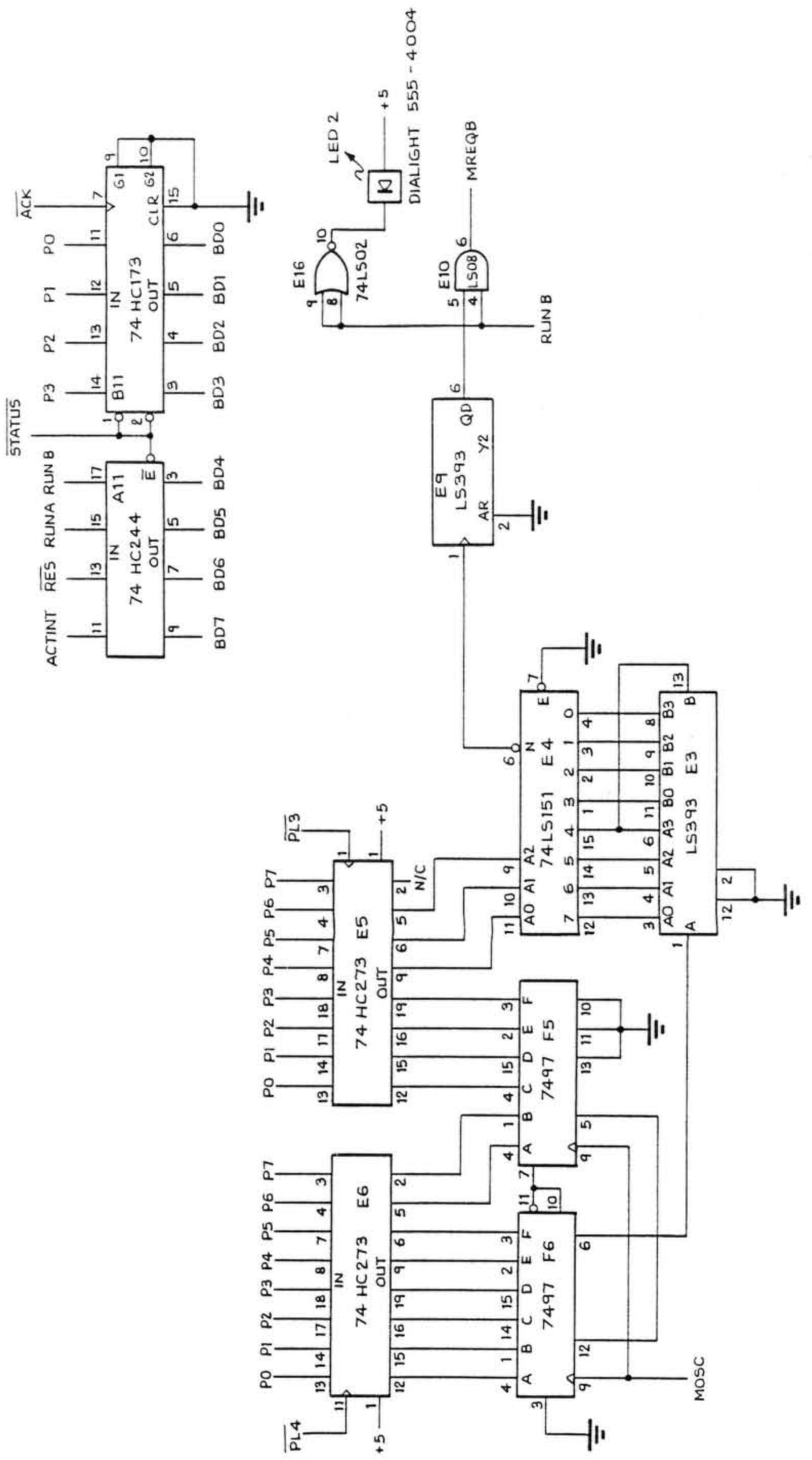
fairlight



Channel B Pitch Generation

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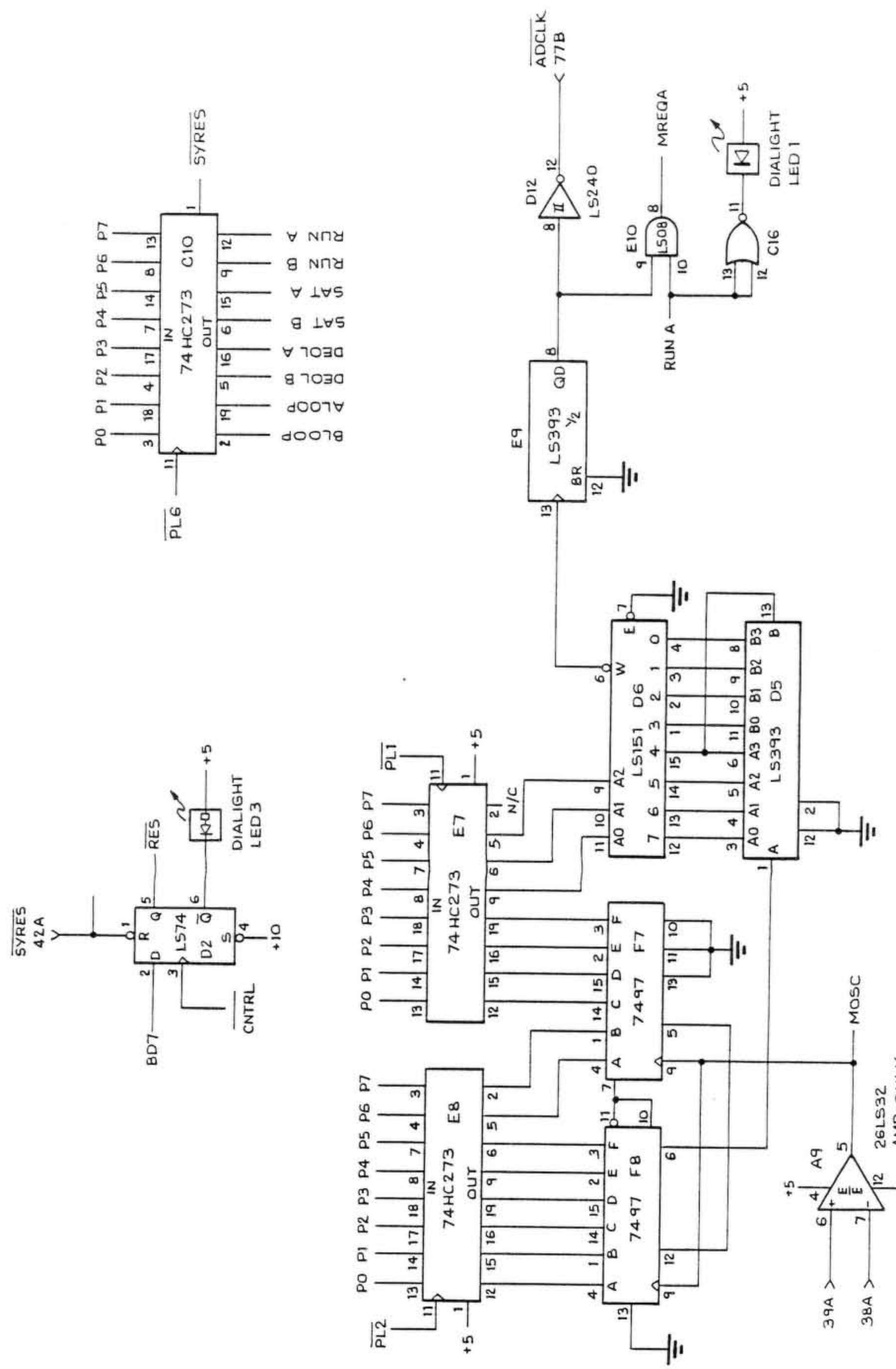

Channel A Pitch / Control Latch

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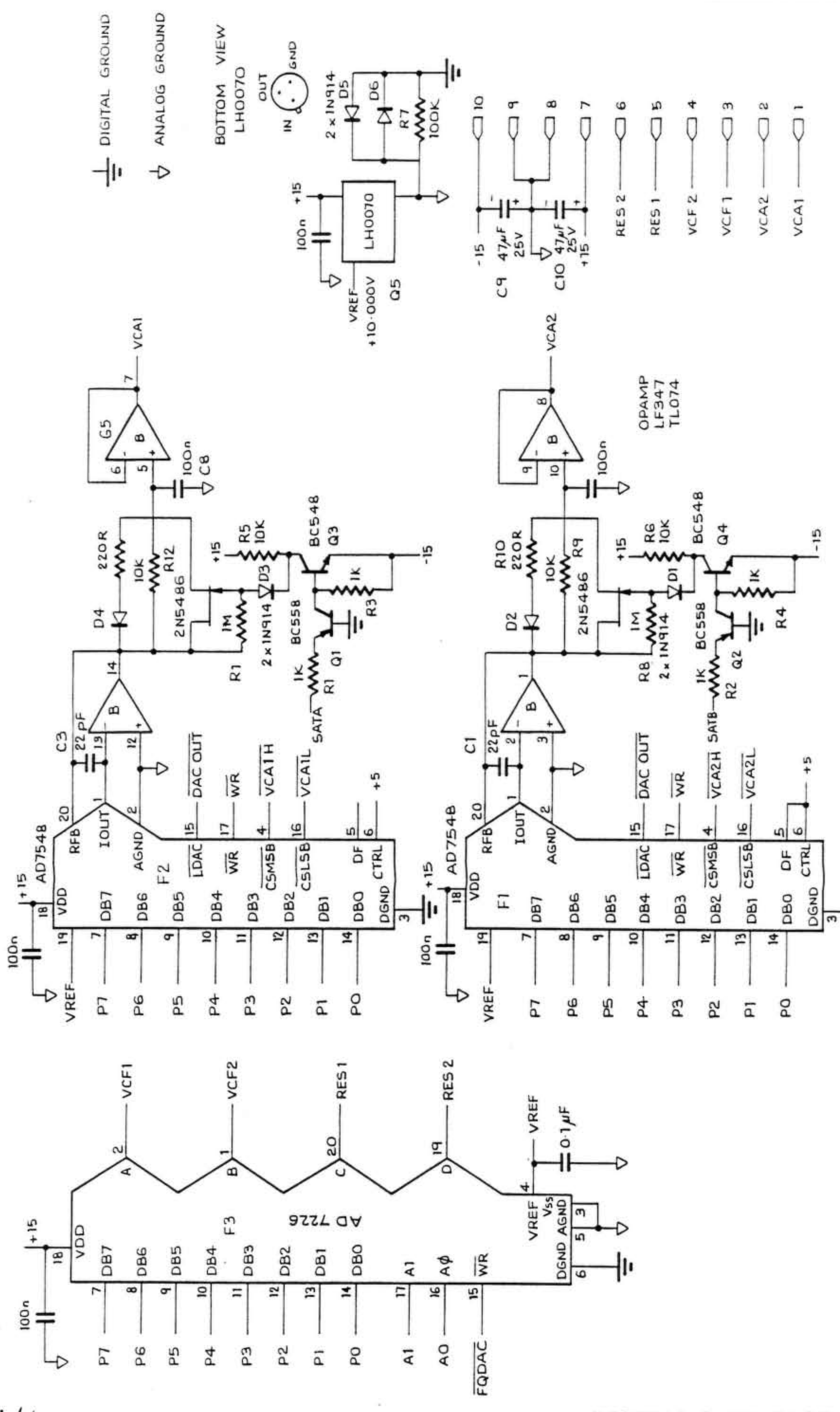

Control Voltage Generation

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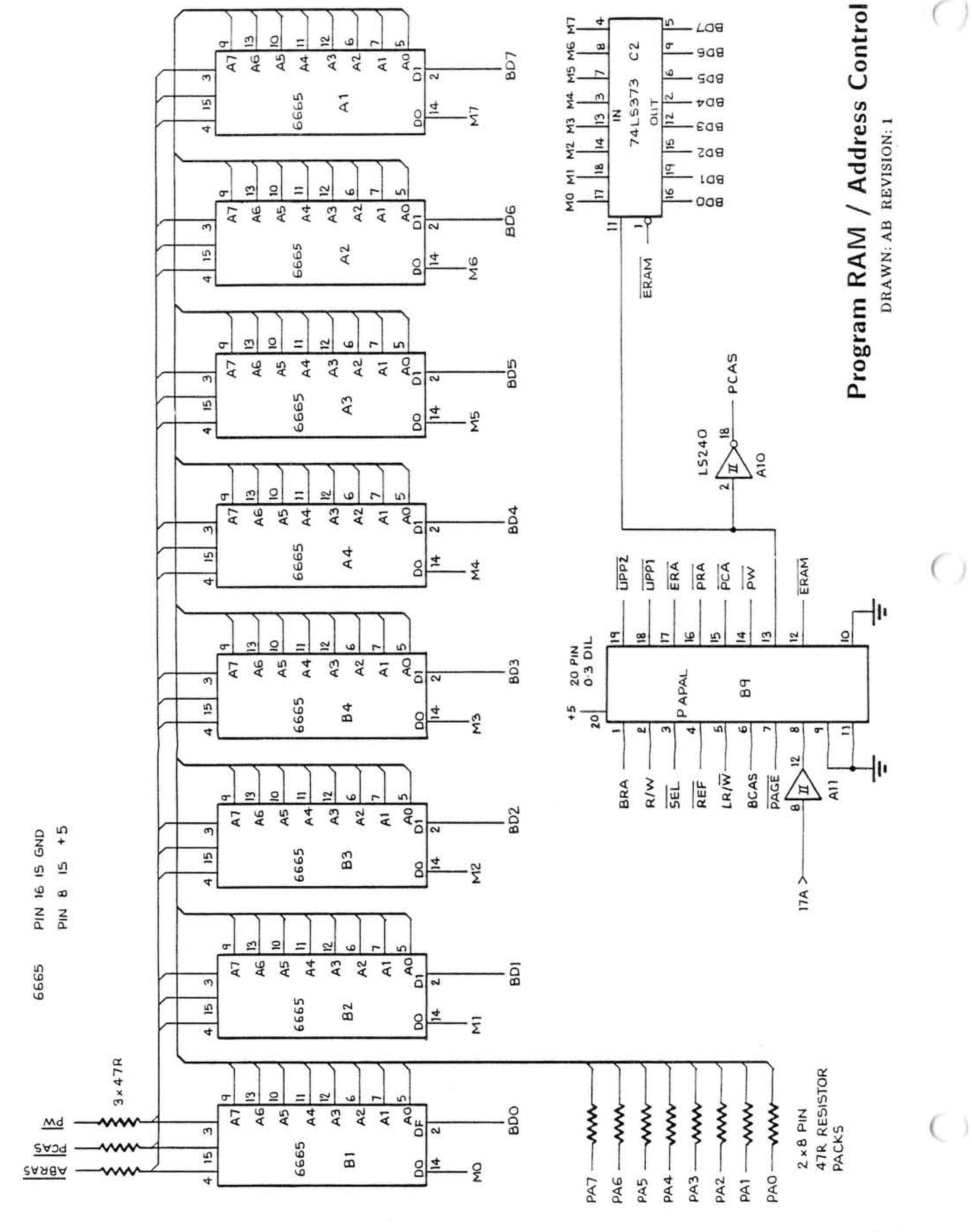
Program RAM / Address Control
DRAWN: AB REVISION: 1
6665 PIN 16 15 GND
PIN 8 15 +5
3×47R
2 × 8 PIN 47R RESISTOR PACKS
74LS373 C2
P APAL B9
20 PIN 0·3 DIL
LS240
PCAS
ERAM
BRA
R/W
SEL
REF
LR/W
BCAS
PAGE
17A
UPP2
UPP1
ERA
PRA
PCA
PW
PW
PCAS
ABRAS
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
M0
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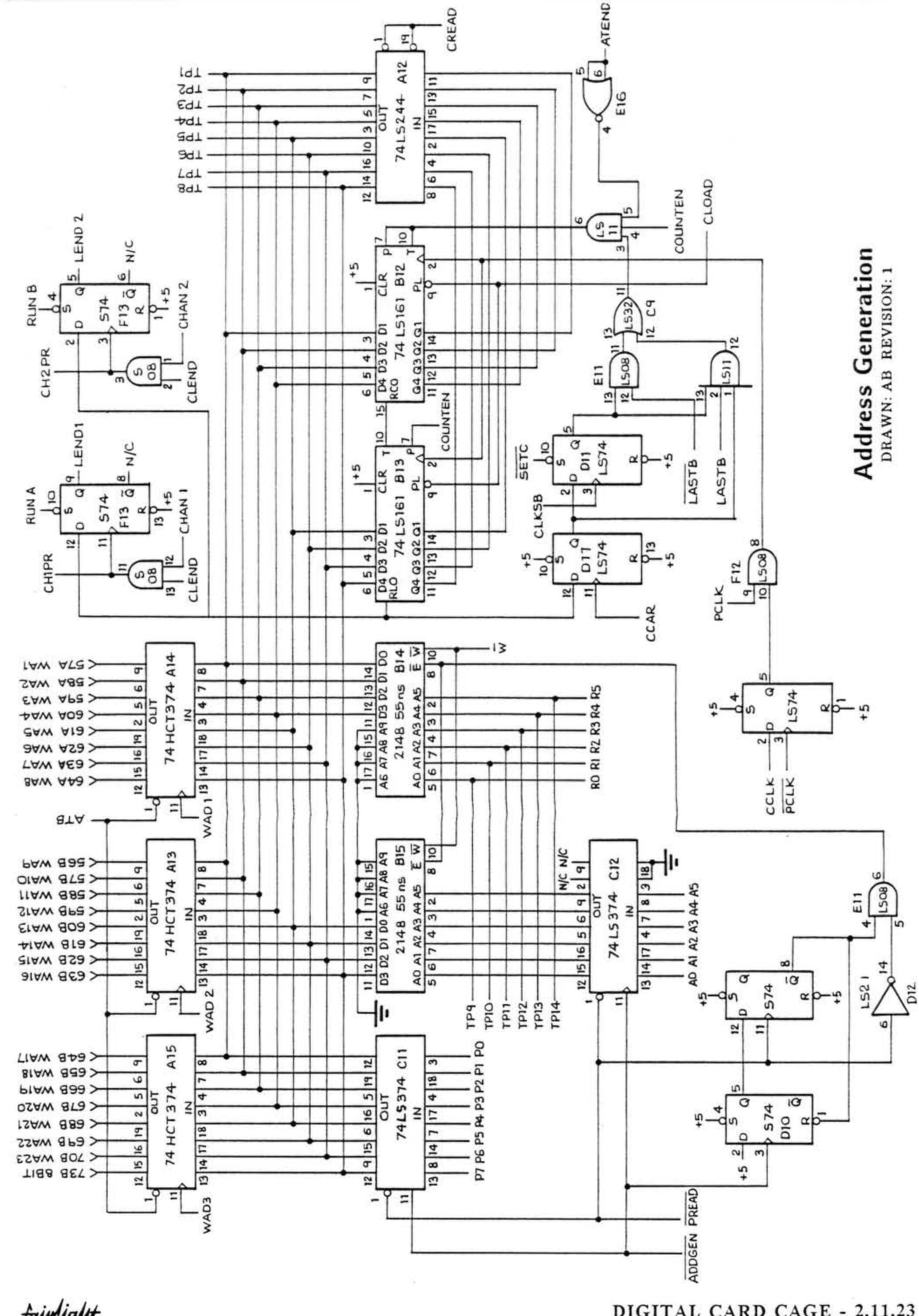
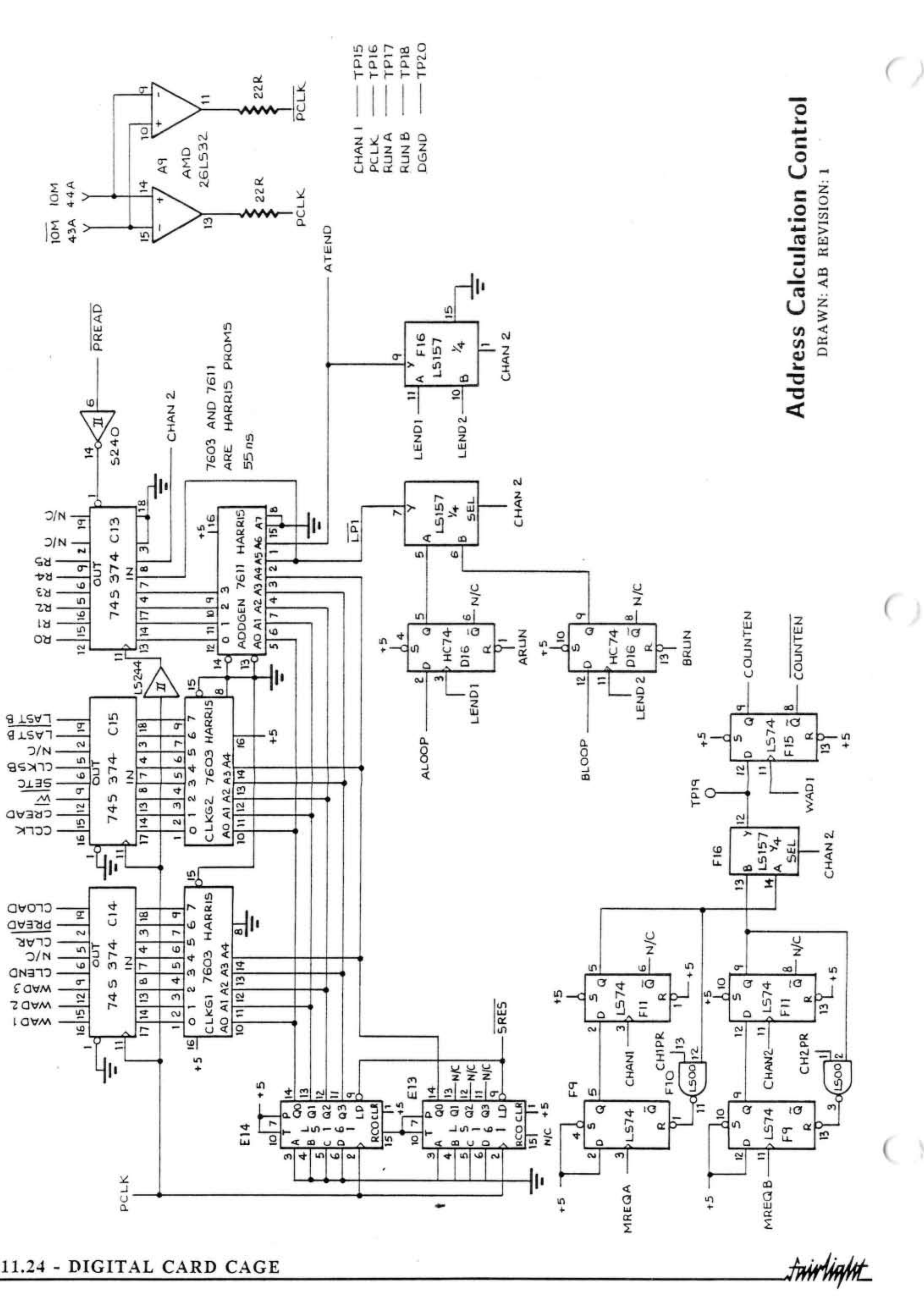
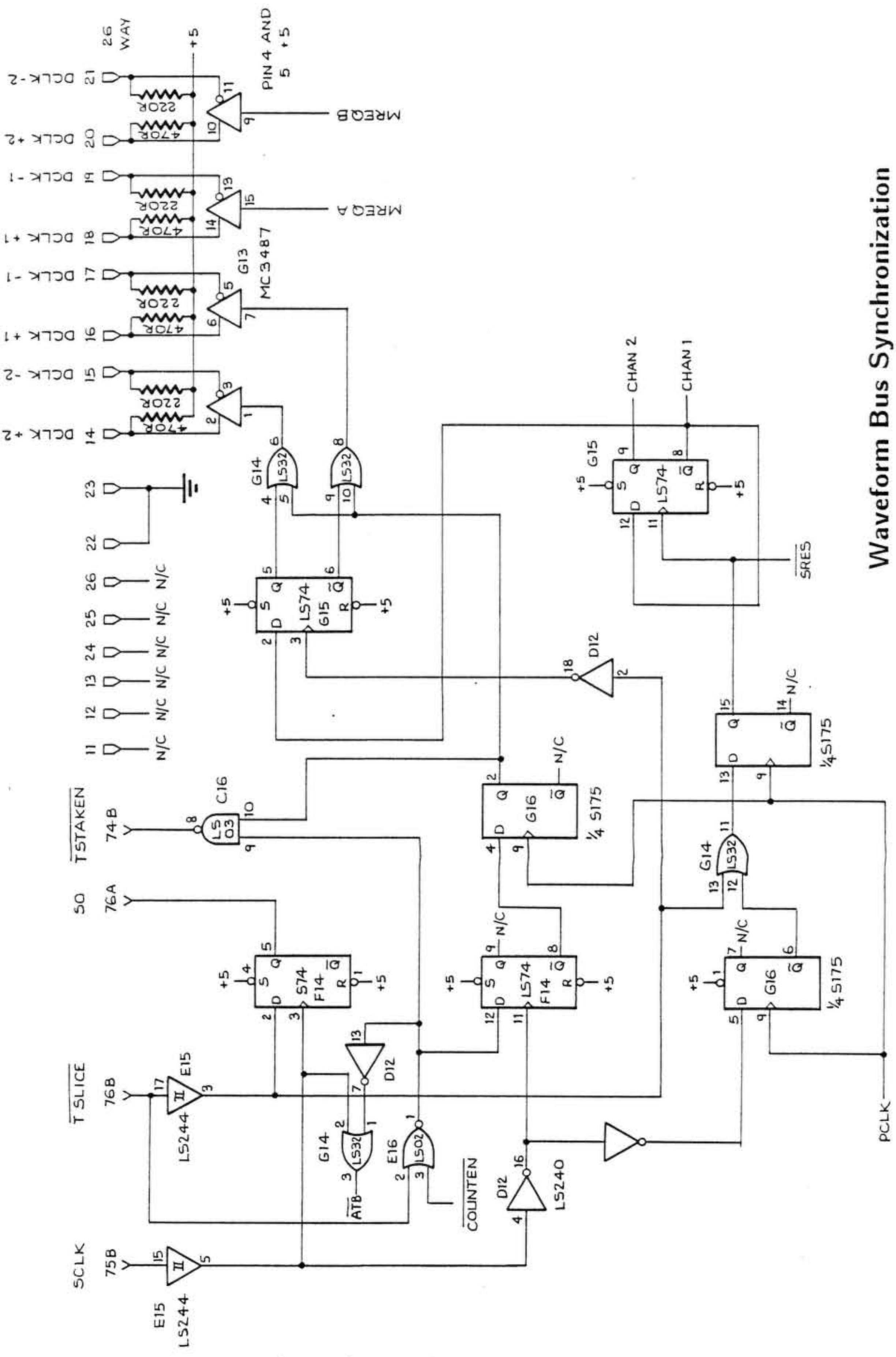
PA3
PA2
PA1
PA0


Address Generation
DRAWN: AB REVISION: 1


Address Calculation Control
DRAWN: AB REVISION: 1
7603 AND 7611 ARE HARRIS PROMS 55ns
CHAN 1 — TP15
PCLK — TP16
RUN A — TP17
RUN B — TP18
DGND — TP20
AMD 26LS32



Waveform Bus Synchronization

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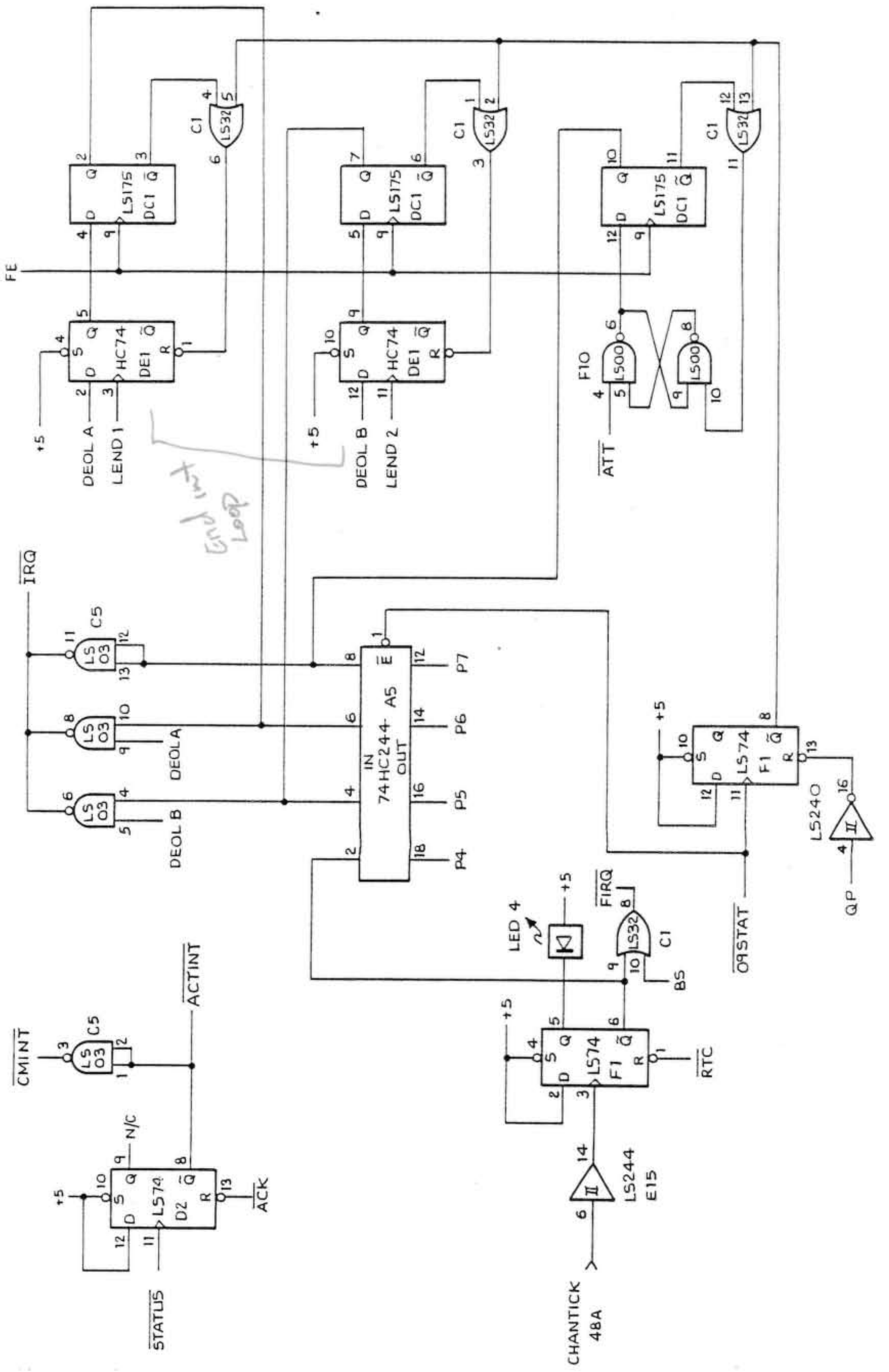
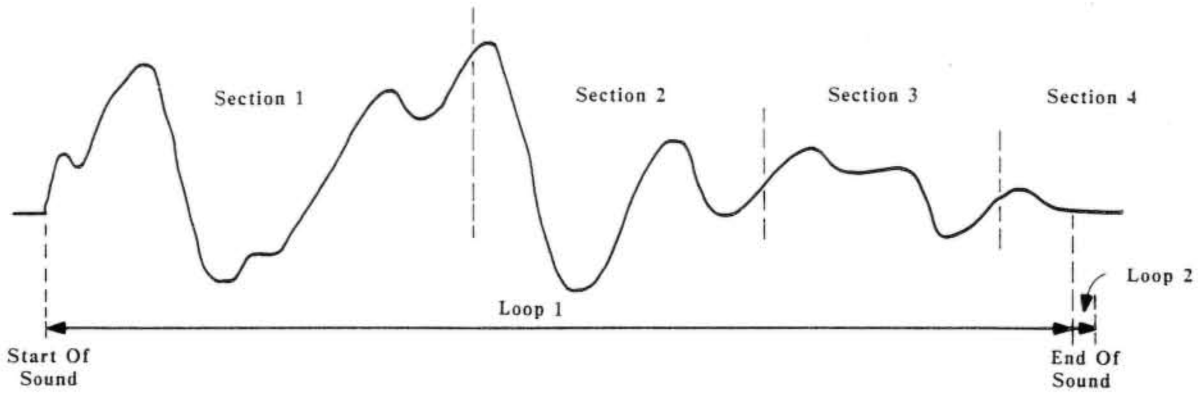
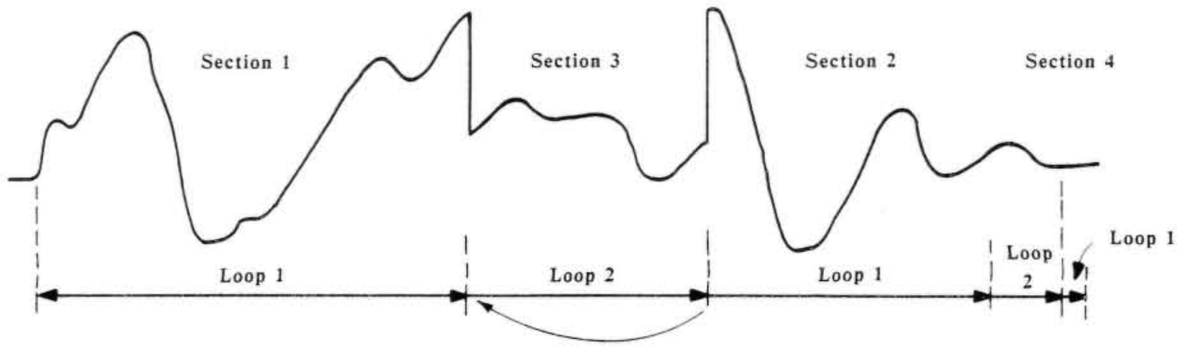


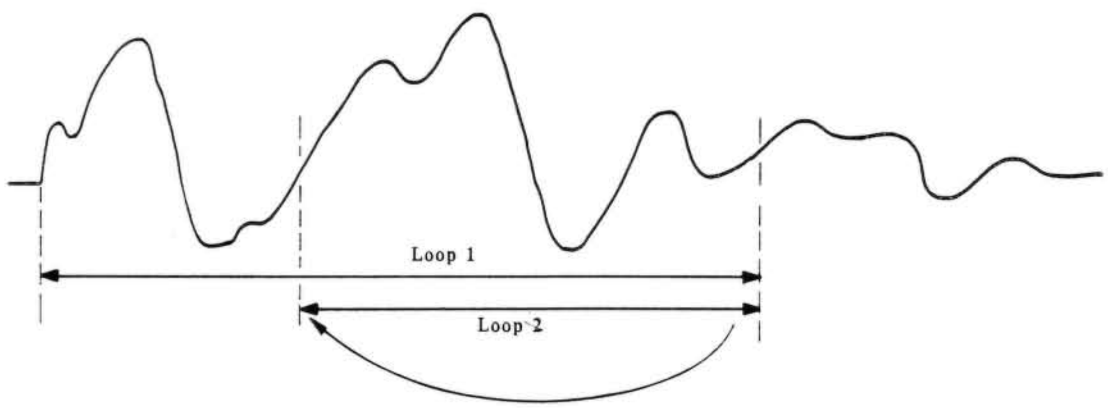
Interrupts

DRAWN: AB REVISION: 1

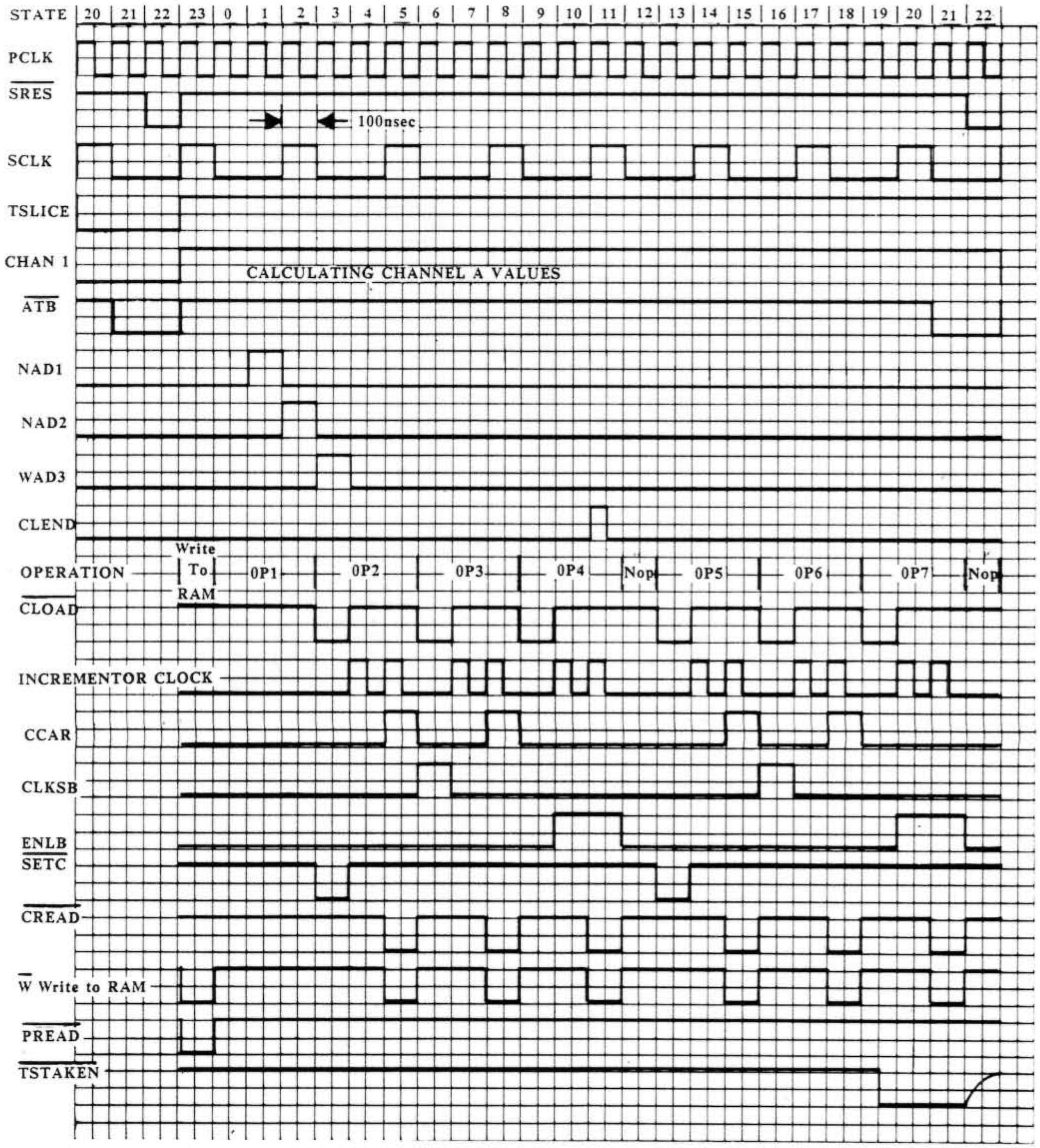
Address Generator Loops



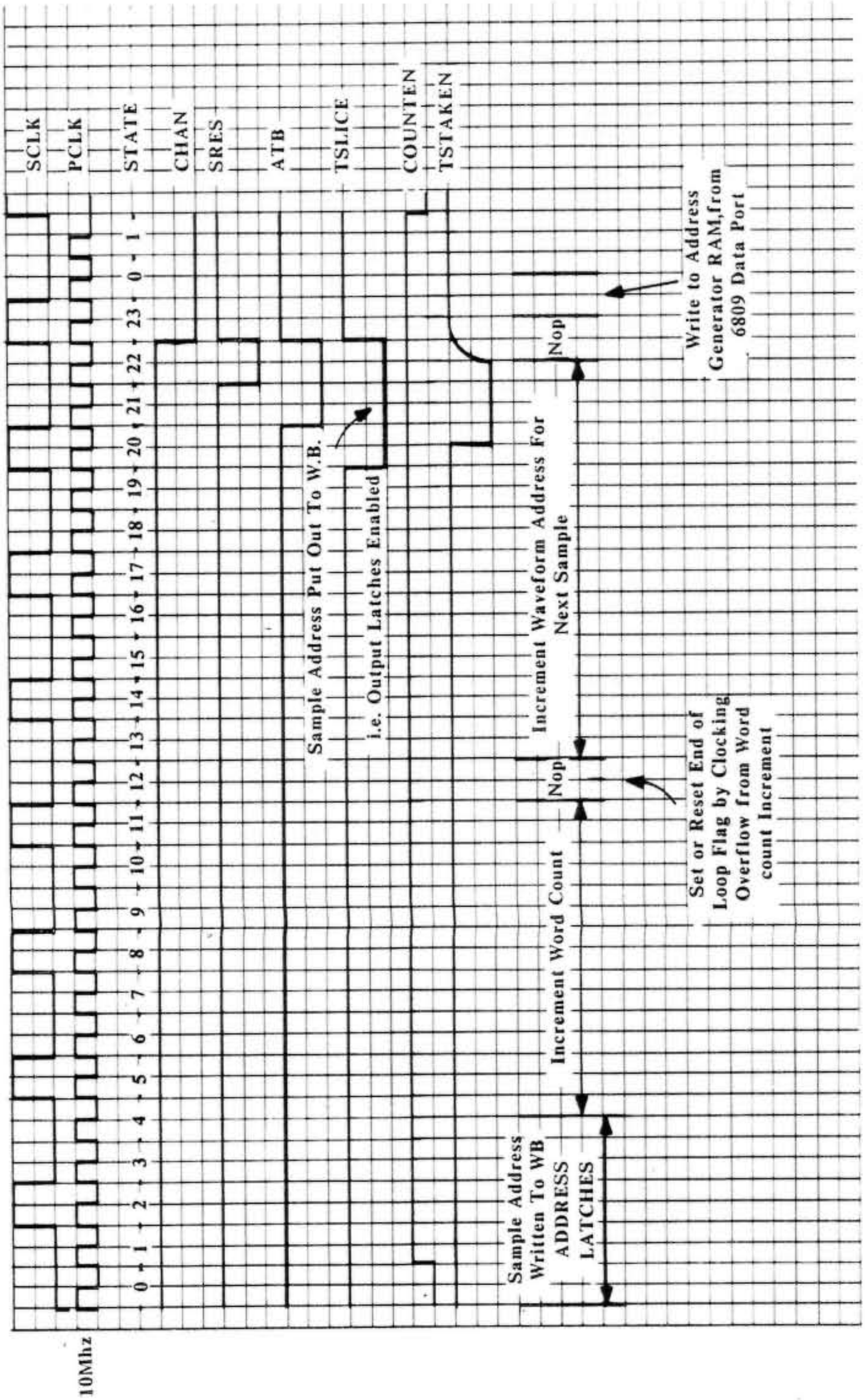




Address Generator Control Signals



An active address generator cycle



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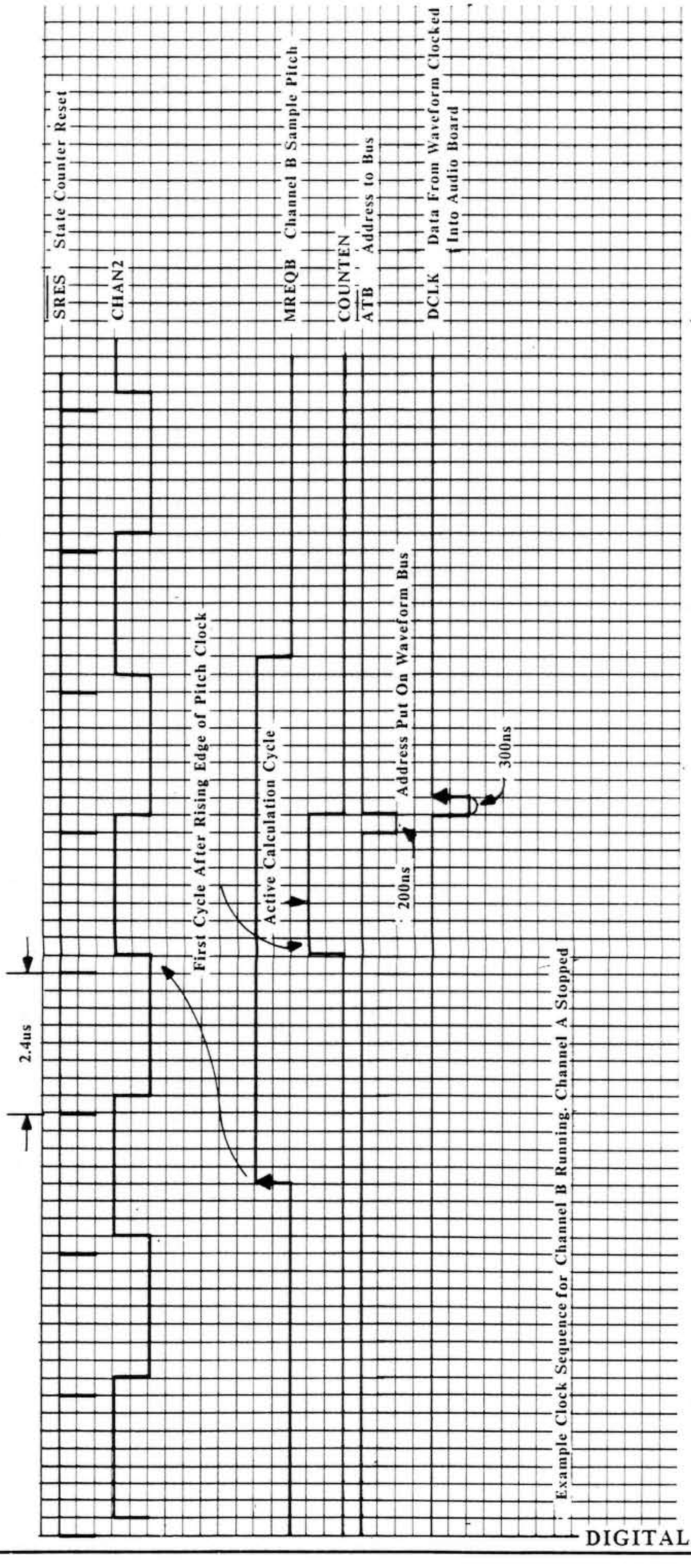
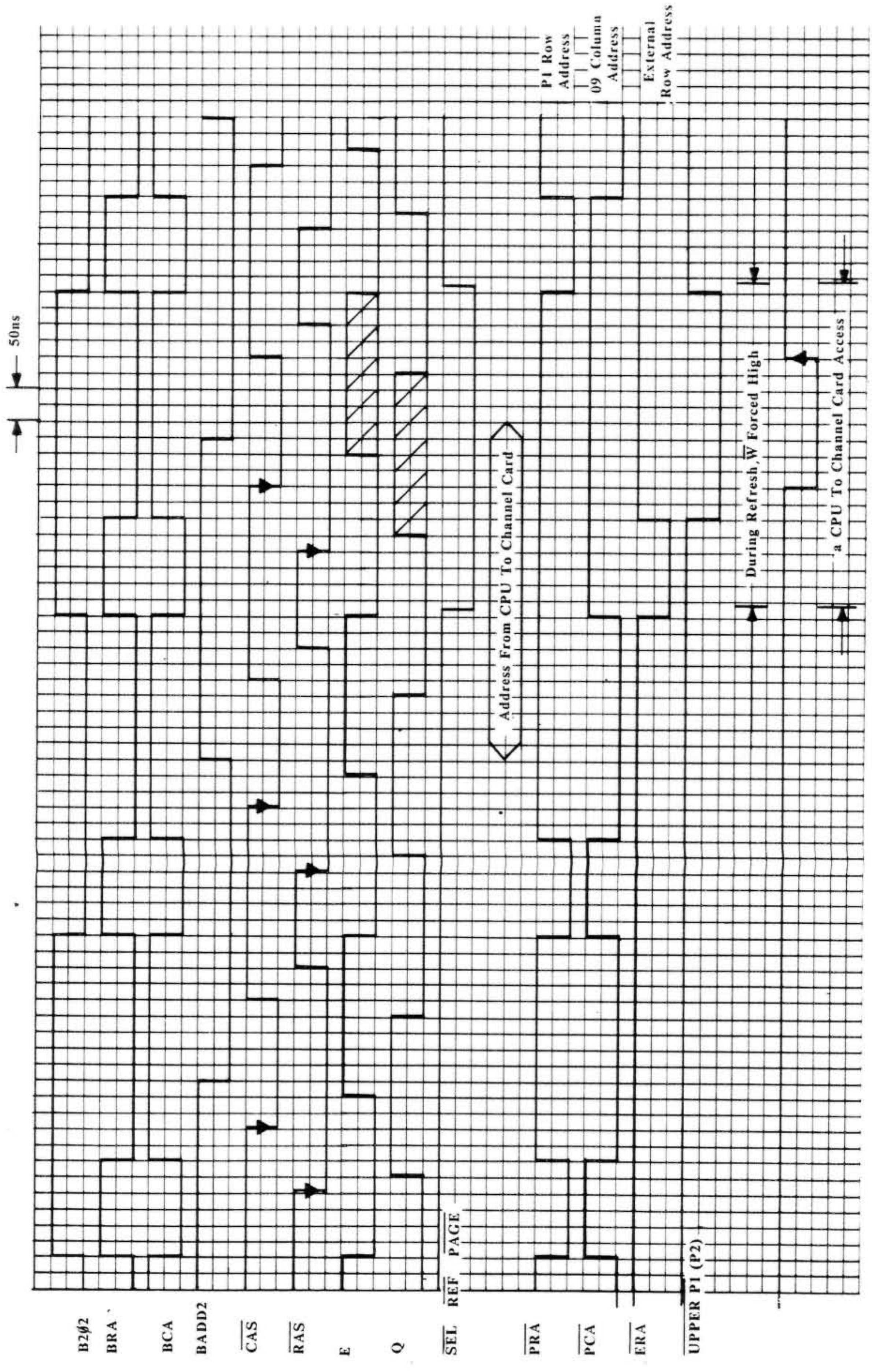


The operation of count enable



CMI Bus Interface