#1 OF 3

ORIGINAL

I N D E X

CG-3

COLOUR GRAPHICS CARD

fairlight

FIELD CHANGE NOTICE

DATE 3/ 5 / 93
NUMBER 127

ORIGINATOR John Gavin **PRODUCT: CMI / MFX**

ASSEMBLY No. CG-3 **DESCRIPTION** COLOUR GRAPHICS CARD

This FCN applies to REV No: REV 1.0 **New REV No is:** REV 1.1

REASON FOR CHANGE:
To correctly document changes made to production boards. All REV 1.0 boards have the following modifications done at the time of manufacture.

DETAILS OF CHANGE:

1. Wire link pin 6 to pin 13 of U 30 on the solder side of board.

2. Label board REV 1.1.

ORIGINATOR: JGavin	**DATE:** 3/5/93	**TEST:** Mario Paolucci 4/5/93 **PROD:** JGavin	**DATE:** **DATE:** 3/5/93
SERVICE:	**DATE:**	**KIT LIST CHANGE:** YES (NO)	

ESP-CG3 High Resolution Graphics Card Rev 1.0

HARDWARE DESCRIPTION

Document Revision: 1.0 2.9.1992 CEA

Fairlight ESP Pty. Ltd.
30 Bay Street,
Broadway,
Sydney Australia 2007.

ESP-CG3 Rev 1.0 Hardware Description
Fairlight ESP

Introduction

The CGD03 graphics card is capable of operating in three modes:

(1)	Low resolution	512(h) x 256(v),
(2)	Double	512(h) x 256(v) double scan,
(3)	High resolution	512(h) x 512(v).

The low resolution mode is only provided for compatability with the Q219 monochrome graphics card and is no longer used by the CMI software. As modern colour screens have high resolution raster lines, low resolution mode leaves gaps between horizontal lines.

Double mode provides the same resolution as low resolution mode (for compatability with CMI music software), with each vertical line displayed twice to fill the gaps in the high resolution raster lines. This mode is used for music software and Revision 9 disk recorder.

High resolution mode provides a 512 x 512 resolution picture used in Revision 10 and higher disk recorder software.

Video memory is located in the range 8000-BFFF with 8000 appearing in the top left corner of the screen (when the horizontal scroll register is zero). Each byte is displayed horizontally with the most significant bit displayed left-most. As there are 512 horizontal pixels, each 64 bytes represent one horizontal line.

The CGD03 card maintains compatability with the Q219 monochrome cards by generating colour using 8 planes of video memory with each plane identical to the Q219 memory. Each pixel on the screen receives the 8 plane bits which are fed through pallete RAMs (with other signals used for video effects) to produce the 6 bit TTL video output.

For faster graphics, locations are provided to automatically increment video memory address for write in the X and/or Y direction. Writing a byte to thse locations store the byte or bit and move the next update position. The initial update position is set via a dummy access to an absolute video RAM location.
determine the resultant 6 bit TTL video output.

Vertical scrolling is provided for faster text mode printing. Horizontal scrolling is provided on two planes for waveform scrolling on the disk recorder (only used in Revision 10 and above).

There are three software updatable palletes. MDR PALLETE is used for the disk recorder. CMI PALLETE is used for the CMI music software. OSK PALLETE is used for the operating system shell.

The CGD03 only produces TTL 6 bit video output. A buffer board is used to convert the data for TTL monitors or RGB anolog monitors.

2.1 P1/P2 Buss Interface
(see CGDCPU.SCH)

Accesses to the Video RAM (locations 8000-BFFF) are decoded by U19a (74LS20). This signal is qualified with *CGDEN by U54a (74LS32) to produce an active low card selection at U54a/3. *CGDEN is used as a card enable in a multiple graphics card system. The card selection is latched on the rising edge of RA by U23 (74LS374) to produce the video RAM enable signal *VRAM. As there is 32k of video memory for each plane, the video RAM must be accessed as two separate pages in the 16k 8000-BFFF memory range.

U21 (74LS138) decodes I/O addresses as 32 byte blocks in the range FC00-FCFF. Jumper JP1 is used to select the I/O address for this card. For a single graphics card system, I/O devices must be loscated at FCC0-FCDF. The selected enable from JP1 is latched on the rising edge of RA by U23 (74LS374) to produce *IOSEL.

I/O block locations (card at FCC0-FCDF)

FCC4,5	vertical scroll register
FCC6	control latch
FCC8,9	horizontal scroll register
FCCA	colour plane write selection latch
FCCB	colour plane read override latch
FCD0	store bit at current location
FCD1	store bit and increment X
FCD2	store bit and decrement X
FCD3	store byte at current location
FCD4	store bit and increment Y
FCD5	store bit and increment X, increment Y
FCD6	store bit and decrement X, increment Y
FCD7	store byte and increment Y
FCD8	store bit and ~~increment Y~~ decrement Y
FCD9	store bit and increment X, decrement Y
FCDA	store bit and decrement X, decrement Y
FCDB	store byte and decrement Y

When a byte is accessed the complete byte is read/written to the VRAM. When a bit is accessed, the current pixel location X,Y enables only the bit corresponding to the pixel bit in video memory.

IOPAL with U67 (74LS138) decode the latched address lines to provide the control signals for the above I/O functions. Auto-update operations assert the appropraite active low YUP,YDN,XUP,XDN strobes and the *BITMODE signal. Direct accesses to video memory assert the *RAMEN and *DIRECT signals.

The horizontal and vertical scroll position latch is implemented in a PIA enabled by the *PIA signal.

The CPUADD signal is used to share Video RAM accesses between the CGD03 and P1 or P2. While CPUADD is high, the CGD03 is using the Video RAM for display refresh; while CPUADD is low, the Video RAM is free for CPU update.

2.2 Latches
(see CGDLAT.SCH)

To allow vertical and horizontal scrolling, U8 (68B21 PIA) is used as a read-back latch to hold the horizontal (HS0..8) and vertical (VS0..7) starting position to set as the top left pixel. U8 also provides the *CGDEN signal used to software control the enable for the graphics card.

The control latch (U39 74LS374) holds the current control mode bits for the CGD03 card.

Bit 7	DP	displayed page select in low-res and double mode or page to appear at top of screen in high-res mode.
Bit 6	UP	CPU update page select
Bit 5	CMIPAL	CMI pallete selection bit
Bit 4	*P1SEL	enable P1 access (else P2)
Bit 3	PALSEL	select MDR/OSK pallete
Bit 2	D512	enable 512 vertical lines (hi-res and double modes)
Bit 1	*PALEN	enable access to pallete RAM
Bit 0	DOUBLE	enable double mode

If there are 512 vetical pixels, U54c (74LS32) asserts the L512 signal.

The Colour Latch (U40 74LS374) is used to select which of the 8 colour planes are to be enable for read/write by P1/P2. During accesses to the pallete RAM, the colour latch is tri-stated to allow all planes to be disabled and the pallete RAM to be accessed instead of Video RAM in the 8000-BFFF range.

When multiple planes are enabled, and a location in Video RAM is read, the value returned is the logical OR of colour planes for each bit. The Override latch (U85 74LS374) is used to determine which planes are to be included in the ORing of the planes.

2.3 Video Synchronisation Timing
(see CGDSYNC.SCH)

The video dot clock signal (DOTCLK) is a continuous clock at the rate the pixels are to be displayed on the screen. For 256 vertical lines (low-res mode) DOTCLK runs at 10MHz; for 512 vertical lines DOTCLK runs at 20MHz. The CGD03 simply works at half speed in low-res mode.

U47 (74LS161) divides DOTCLK by 8 to clock U46 (74LS161) and U45 (74LS161) at the screen byte rate. U45,46 count the current byte position displayed on the screen. Bytes 0..63 are the displayed byte times - the rest of the byte counts until LRST (line reset) is asserted by SYNCPAL are the horizontal blanking period. HBLANK is asserted for this purpose by detecting bytes 64 and greater.

U44,43,42 (74LS161) are the current vertical line counters. These counters are incremented at the end of each horizontal line

by the LINC (line increment) signal generated by SYNCPAL. Th eline counts 0..511 are the displayed lines - the rest are the vertical blanking period. When *LASTL (last line) is asserted by SYNCPAL, the line counters are reset to start the next screen refresh.

The *VSCRST signal resets the vertical scroll counter at the beginning of each screen refresh. The BLANK signa lis the logical OR of the horizontal blanking period and the vertical blanking period used to turn off the display during horizontal and vertical retrace.

2.4 CPU Access VRAM Addressing
(see CGDCADD.SCH).

When P1/P2 directly access VRAM (*DIRECT = 0), U24 (74LS244) and U25 (74LS244) assert the CPU address lines to the VRAM address lines RA0..13. RA14 is provided by the UP (update page) signa lto select which bank of 16k appears from the 32k plane VRAM at 8000-BFFF. Every direct access to VRAM loads the current screen update location into the auto-increment/decrement counters U53,37,14,18,17,52 (74LS193 up/down counters).

An access to VRAM bits via the auto-increment/decrement location assert the YUP,YDN,XUP,XDN signals to control these counters at the end of the access ready for the next access. The output of these counters hold the next pixel bit number (BS0..2), and the screen byte position (CA0..14) and the current update page (CUP). The UP signal is included in the count to allow auto-increment/decrement for all the 32k of VRAM.

2.5 Screen Refresh Access VRAM Addressing
(see CGDVADD.SCH)

U35a and U35B (74LS393) generate the current byte-in-line address to be accessed from the VRAM for refreshing the screen display. After every load of data from the VRAM (end of PLOAD assertion), U35 is incremented to the next byte address. U35 is reset during vertical sync (*VSYNC = 0). At the end of every line, U35 folds back to zero ready for the next line.

2.6 VRAM Address Multiplexing
(see CGDMUX.SCH)

While the CPUADD signal is low, U15,16,36,51 (74LS257) select the video refresh address lines (VA0..14) to be routed to the VRAM address lines (RA0..14). When CPUADD is high, the VRAM is free for CPU auto-increment/decrement accessesand the current VRAM access address (CA0..14) is routed to RA0..14). During a direct access to VRAM (*DIRECT=0), the multiplexors are tri-stated to allow U24,25 (74LS244) to drive RA0..14 directly.

2.7 Horizontal Scrolling
(see CGDHSC.SCH)

To provide horizontal scrolling, the horizontal scroll latch bits HS3..8 are added to VRAM address lines RA0..5 to generate the scrolling address lines SA0..5. The serial data from the scrolling planes (SD5 and SD6 - planes 5 and 6 are the only scrolling planes), is clocked into U49 and U48 (74LS164) to delay the bit data. Horizontal scroll register bits HS0..2 select which of the delayed signals to display via U33 and U32 (74LS151) de-multiplexors.

2.8 VRAM Data Latches.
(see CGDDATA.SCH)

The Q219 monochrome graphics card VRAM appears as a 16k memory image of the current screen display. To maintain software compatability, colour has been added to the CGD03 card by implementing 8 parallel images of the screen to generate 8 bits of data per pixel to describe colour - each plane is identical to a Q219 screen image.

To read a particular bit on the screen, thee logical OR of the planes enabled by the Colour Latch (COL0..7), excluding bits set in the Override latch (OVR0..7), produce the one bit value read. On write, the data buss bit is written to planes enabled by the Colour Latch. Planes written with their override bit set, will have their pixel cleared. The data conversion is performed by a DATAPAL for each bit in the data buss (BD0..7).

During byte mode accesses, the DATAPALs provide the conversion for all bits in the data buss. During bit accesses, BSELPAL asserts only the BIT0..7 signal appropriate for the current bit position described by BS0..2, enabling only one of the DATAPALs to generate an output.

2.9 VRAM and Video Serialisation
(see CGDRAMA.SCH,CGDRAMB.SCH)

Each of the 62256 32kx8 static RAMs hold the data for one bit plane for the screen. U58 is plane 0 and U65 is plane 7. Note that plane 5 (U63) and plane 6 (U64) have scrolling addresses connected to A0..5. By convention, plane 7 is called the 'cursor' plane and is programmed in the pallete to always be visible (this is used for the mouse cursor, the command line and text at the shell).

During a video refresh memory cycle (CPUADD=0), *PLOAD is asserted to load VRAM data into the shift registers. The *SHIFT signal is then used to clock out the 74LS165 shift register data as serial streams VD0..5 and SD5,6. After the horizontal scrolling hardware for planes 5 and 6, VD0..7 represents the serial video data to be displayed. The 74LS08 AND gates guarantee that all the VRAMs will be enabled during refresh irrespective of the current Colour Latch setting.

The data held in the VRAM is inverted to allow disabled VRAMs

to be read as pixels-off using pull-up resistors to hold undriven lines high. The sense of the data is inverted back to normal by the DATAPALs for CPU reads, and inverted by the 74LS165s during video refresh.

2.10 Video FIFO
(see CGDVID.SCH)

To allow P1/P2 to access video memory, the video refresh data reads from the VRAM have been synchronised to the CMI buss. The output of bits for display is asynchronous to the CMI buss and so a FIFO (U2 CY7C421) is used to buffer the data.

The timing for loading the FIFO and loading the shift registers is provided by LINEPAL.

2.11 Pallete Colour Generation and Video Output
(see CGDVID.SCH)

During the non-blanking periods, LINEPAL generates the read signal for the FIFO synchronous to the output bit clock DOTCLK. The data read from the FIFO appears as pallete RAM address lines PA0..7. The rest of the pallete RAM address lines are used to add attributes decoded by the ATTRIB PAL.

PA8	odd dots
PA9	bottom 384 lines
PA10	odd line
PA11	flashing (from U30 counter)
PA12	half tone
PA13	<spare>

The pallete RAM consists of three 7C185-20 fast static RAMs. The current pallete displayed is selected by U31 (74LS139) using CMIPAL and PALSEL from the Control Latch. Each of the pallete RAM locations are programmed with a value to be sent to the OUTPUT PAL as selected by the 13 bit pallete address. OUTPUT PAL converts the pallete data to TTL video gun signals PRED,PGRN,PBLU (primary red,green,blue) and SRED,SGRN,SBLU (secondary RED,GREEN,BLUE).

The TTL video signals appear at CN2 along with HS (horizontal sync), VS (vertical sync) and GND. A fused +5V supply is also available for the buffer board.

2.12 Software Access to the Pallete
(see CGDVID.SCH)

To access the pallete RAM instead of the VRAM at 8000-BFFF, the *PALEN bit is set low in the Control Latch. This enables P1/P2 address buss lines to the pallete RAM via U28 and U29 (74LS244); and the data buss via U1 (74LS245). The pallete RAM accessed is determined by PALSEL and CMIPAL control bits.

2.13 Video Mode Switching
(see CGDSWICH.SCH)

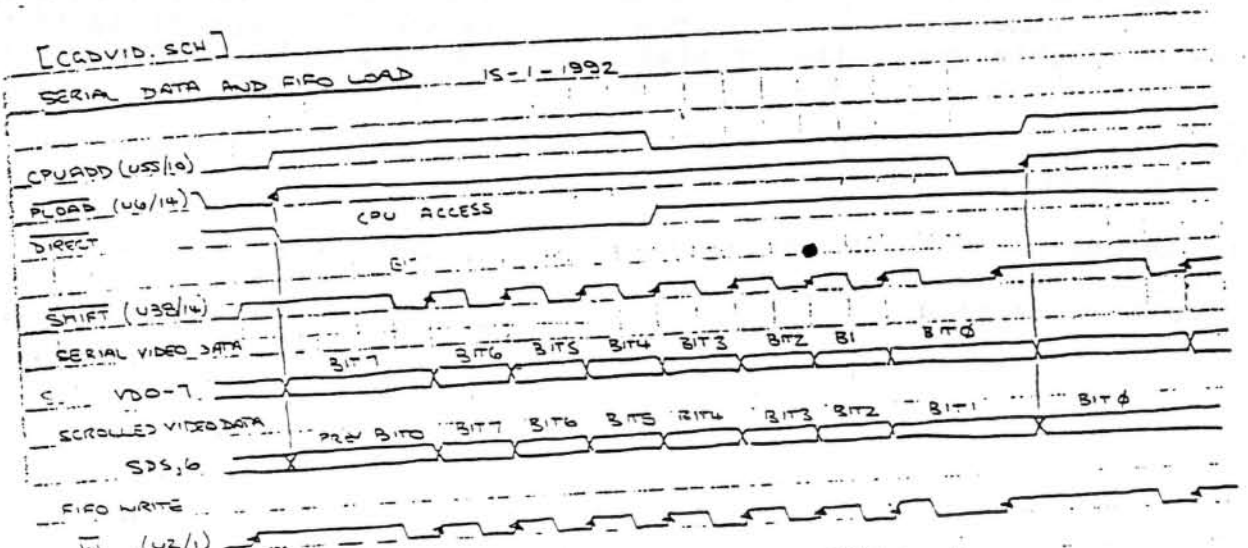
SWITCH PAL is clocked by a 20MHz crystal module to generate DOTCLK and DDCLK (delayed dot clock). If the CGD03 is operating in hi-res or double mode, the crystal is fed straight to DOTCLK. In low-res mode, the crystal is divided by 2 to produce DOTCLK.

CA14 is generated by SWITCH PAL for the different modes by decoding UP,CUP,DP,CDP.

To increment the vertical line counter, SWITCH generates the VINC signal. During double mode, VINC is asserted on every second line to display each line twice.

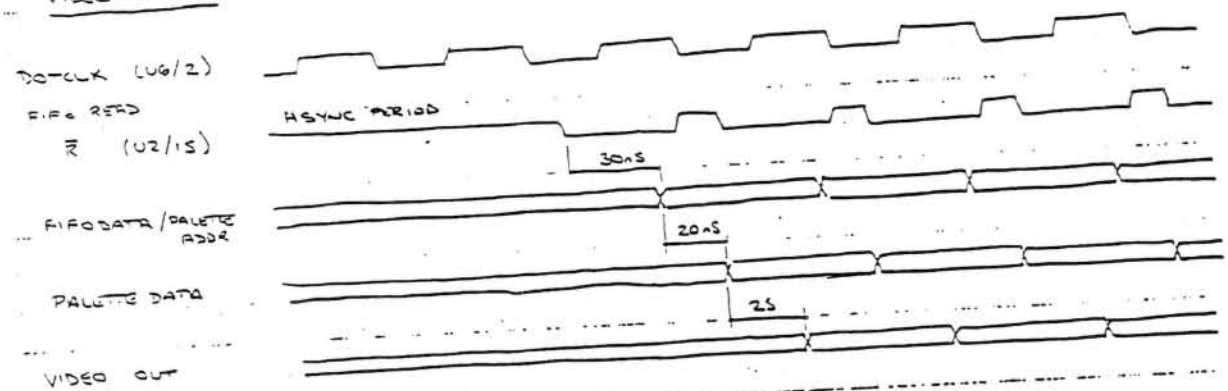
[CGDVID.SCH]

SERIAL DATA AND FIFO LOAD 15-1-1992



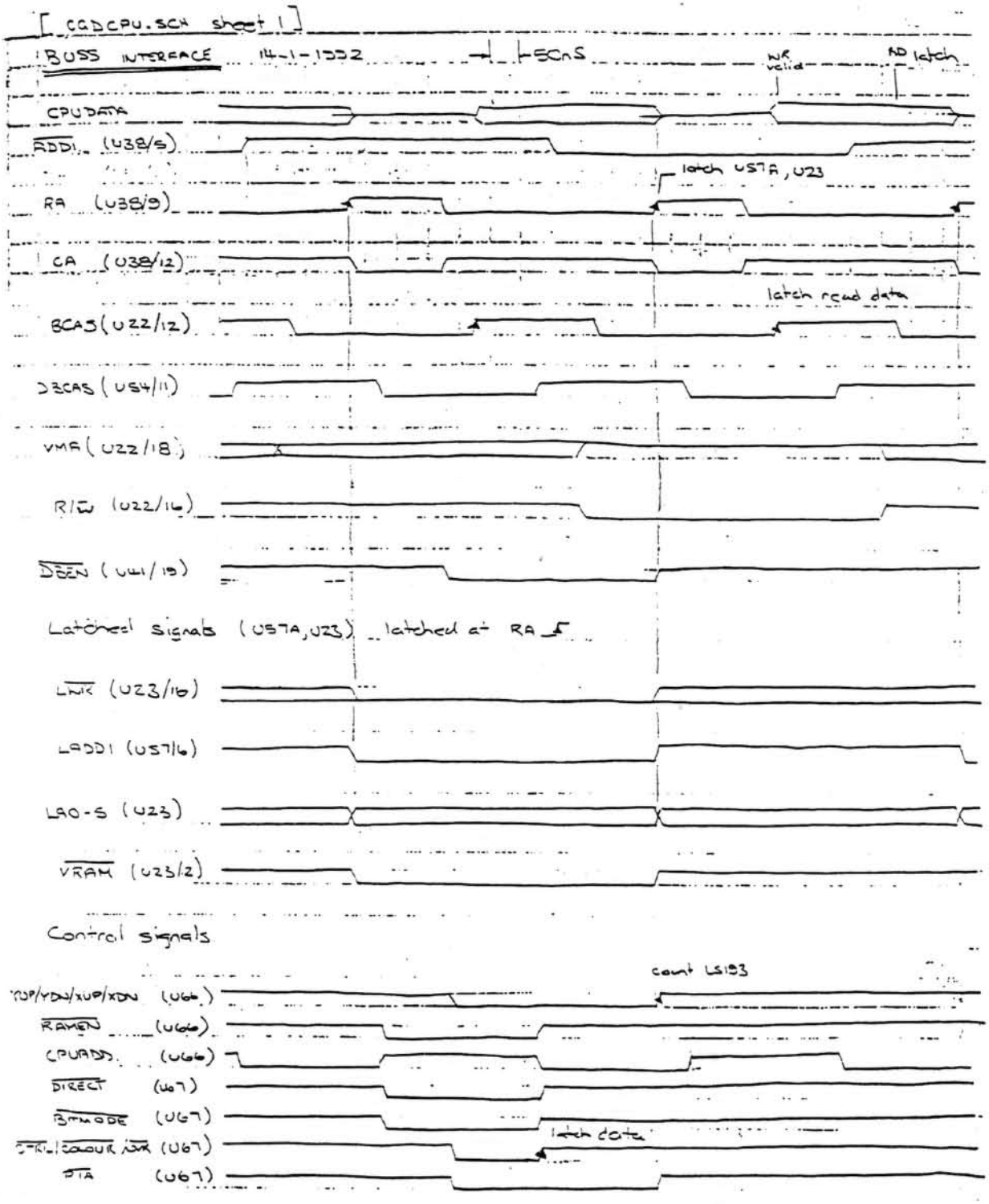
[CGDVID.SCH]

VIDEO OUTPUT 15-1-1992 ← 12.5nS →



[CGDCPU.SCH sheet 1]

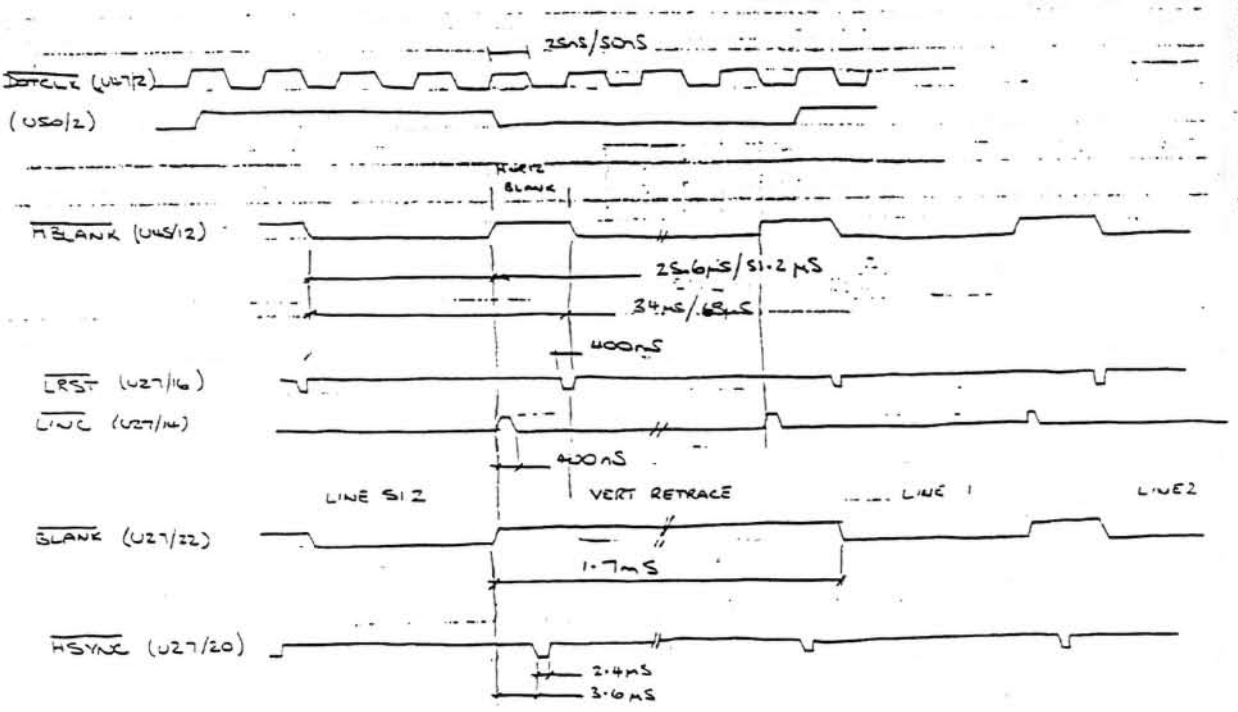
BUSS INTERFACE 14-1-1992 ← 50nS → NR valid ND latch

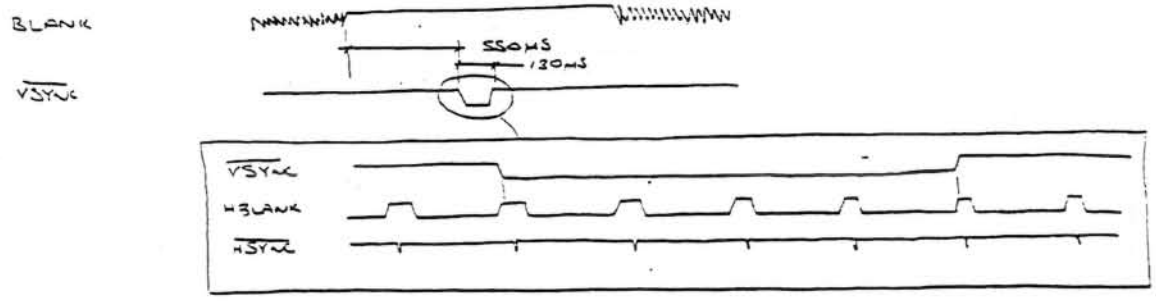


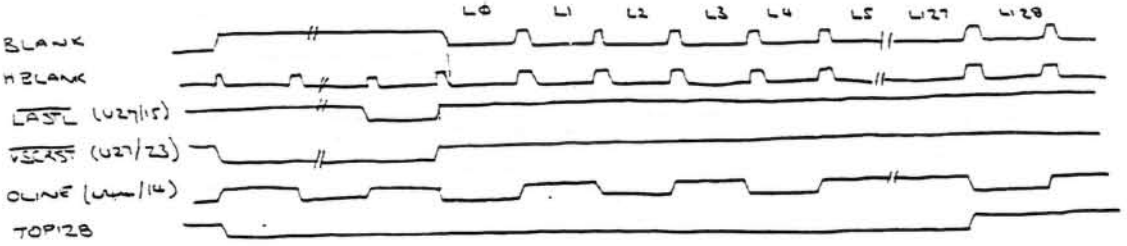
[CRDSYNC.SCH SHEET 3]

VIDEO SYNCHRONISATION TIMING 5-1-1992

TIMINGS SHOWN AS : (LS12)/(LS12')

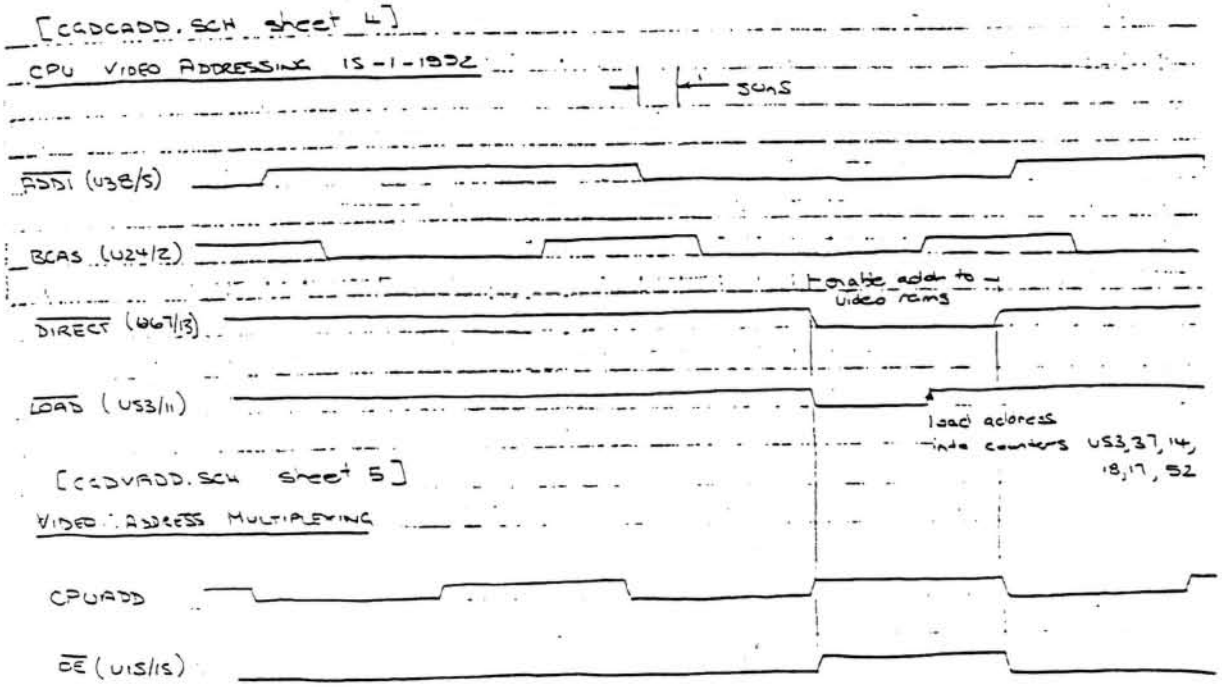






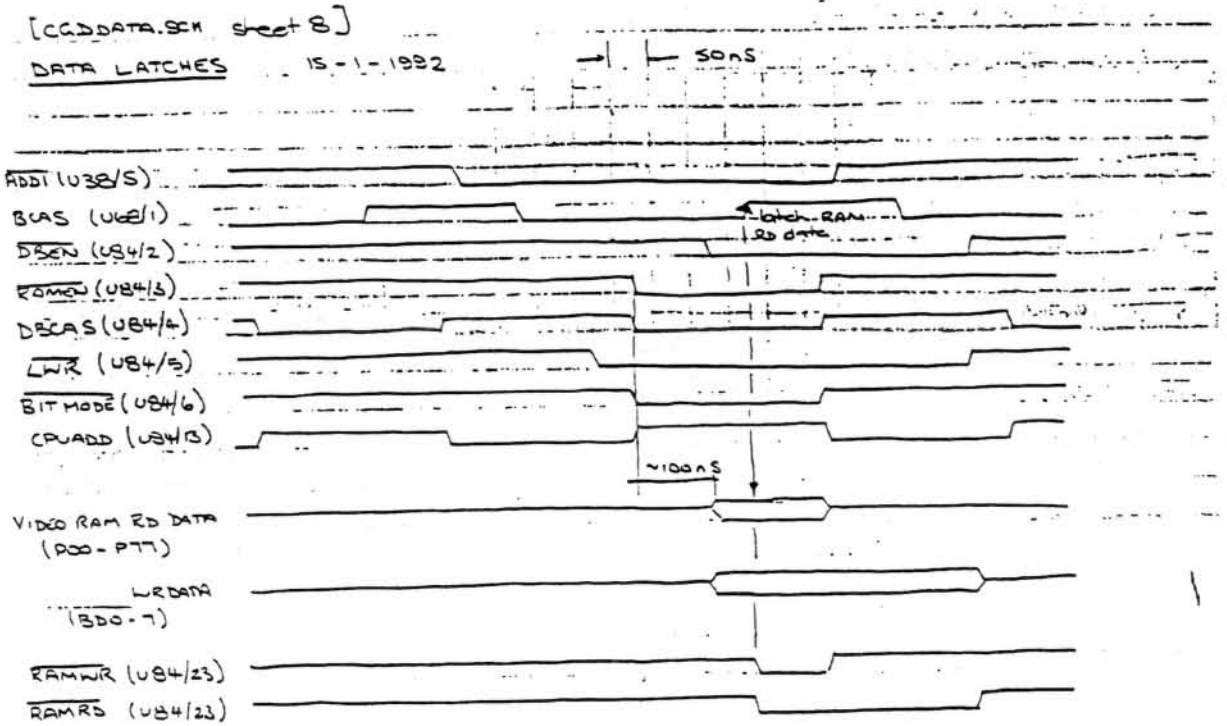
[CGDCADD.SCH sheet 4]

CPU VIDEO ADDRESSING 15-1-1992



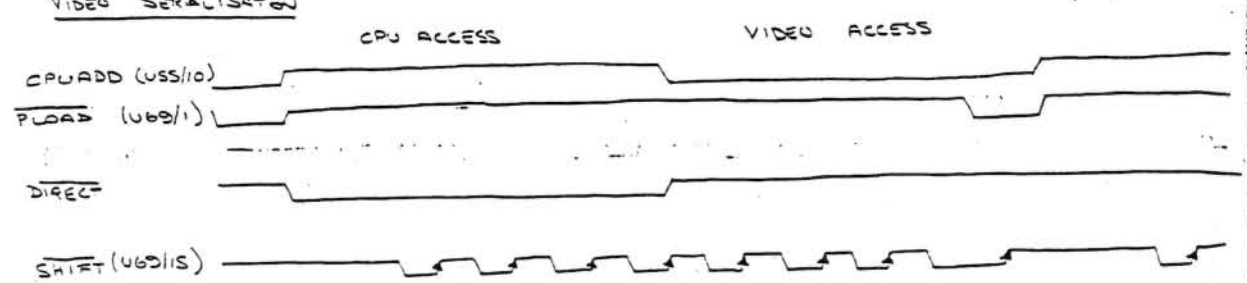
[CGDDATA.SCH sheet 8]

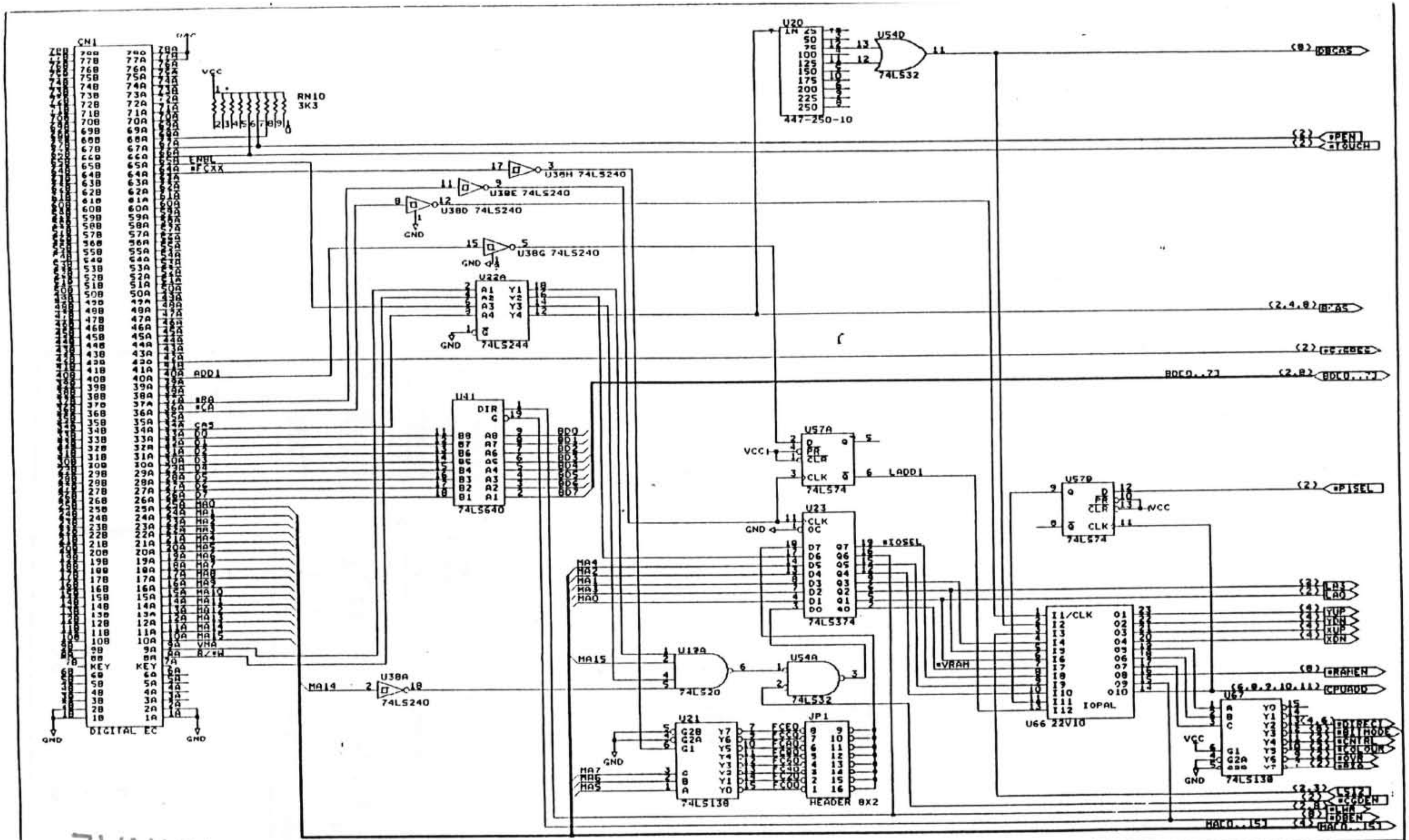
DATA LATCHES 15-1-1992



[CGDRAMA.SCH sheet 9 / CGDRAMB.SCH sheet 10]

VIDEO SERIALISATION





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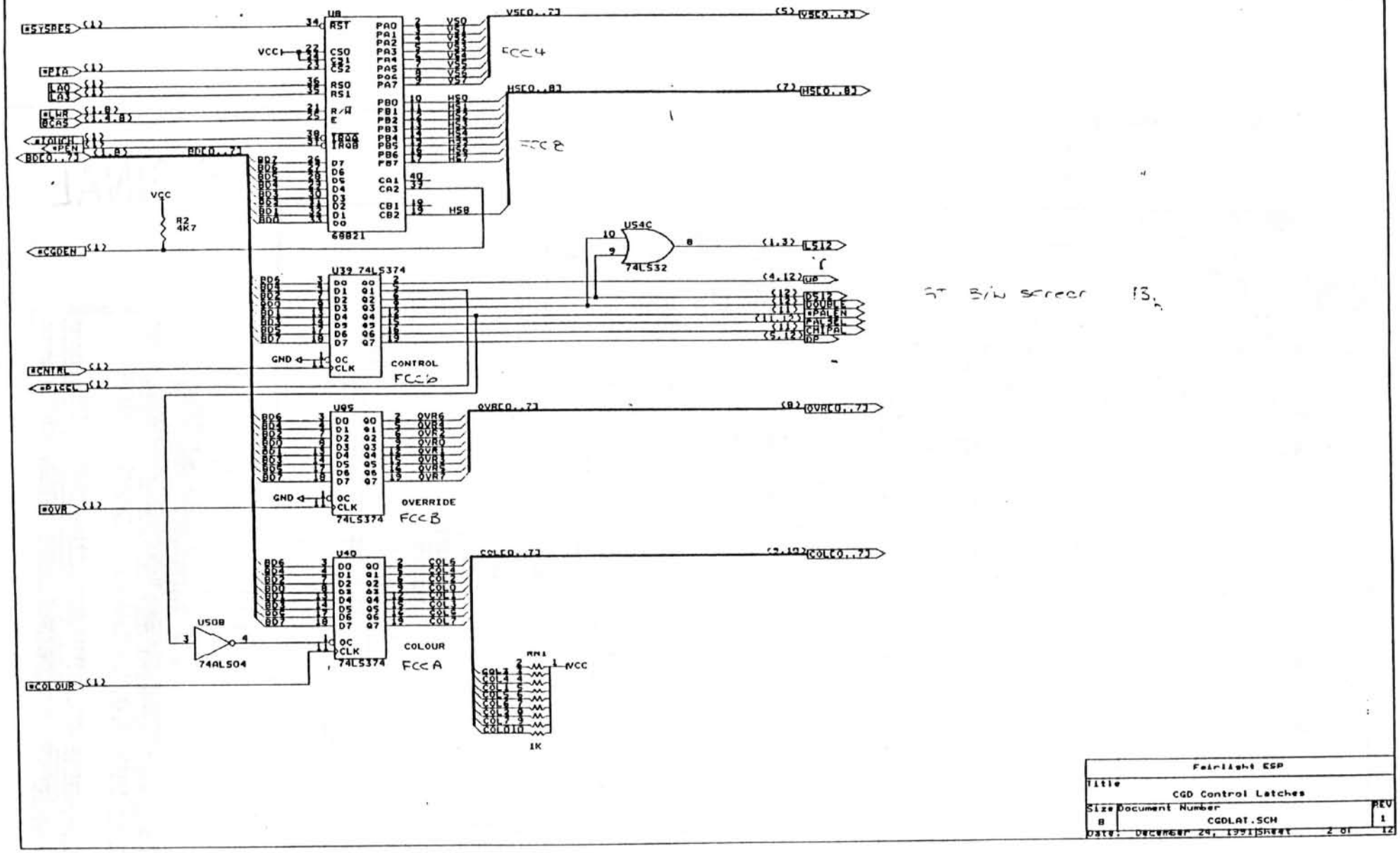
Date: February 17, 1992	Sheet 1 of 12	



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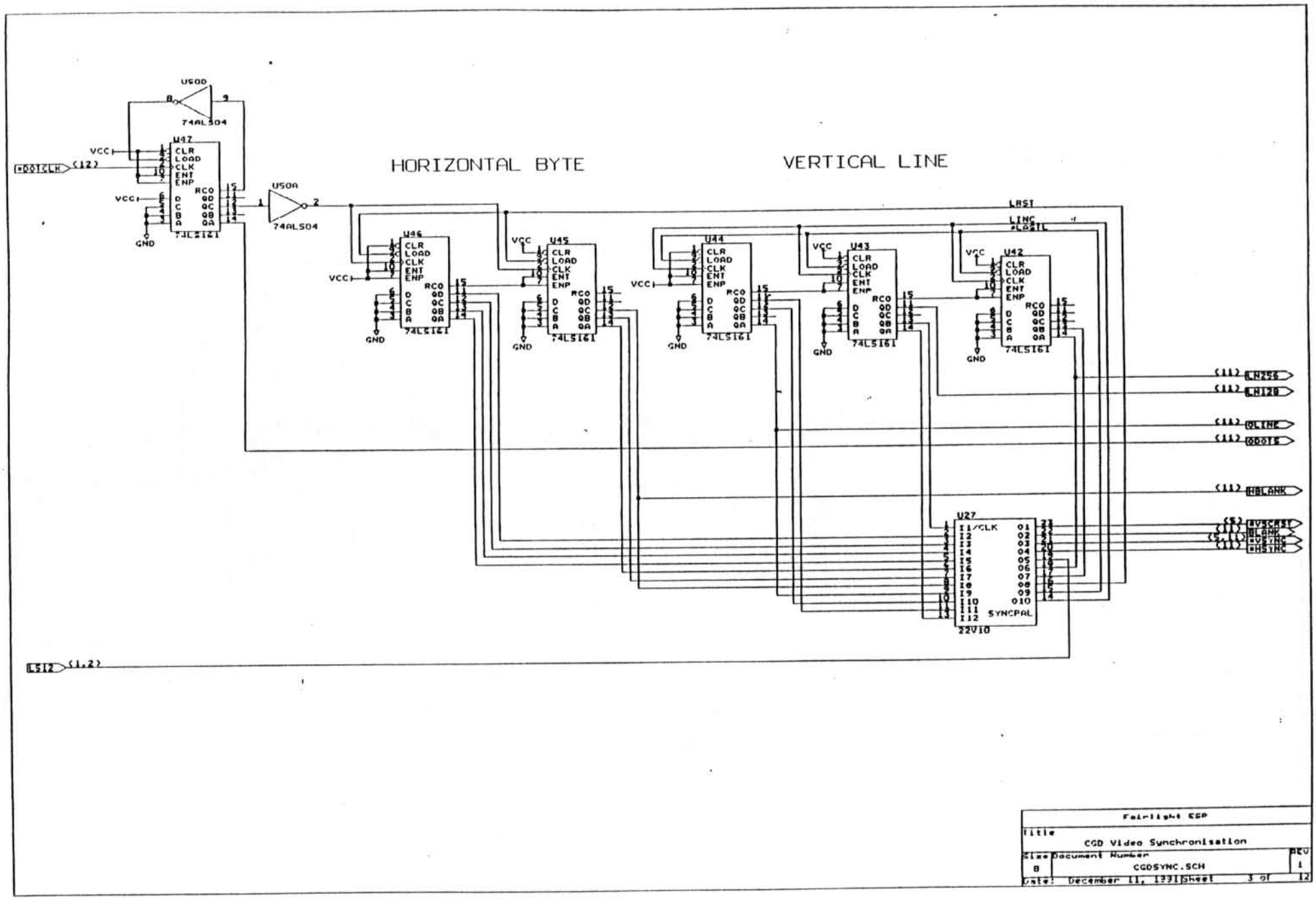

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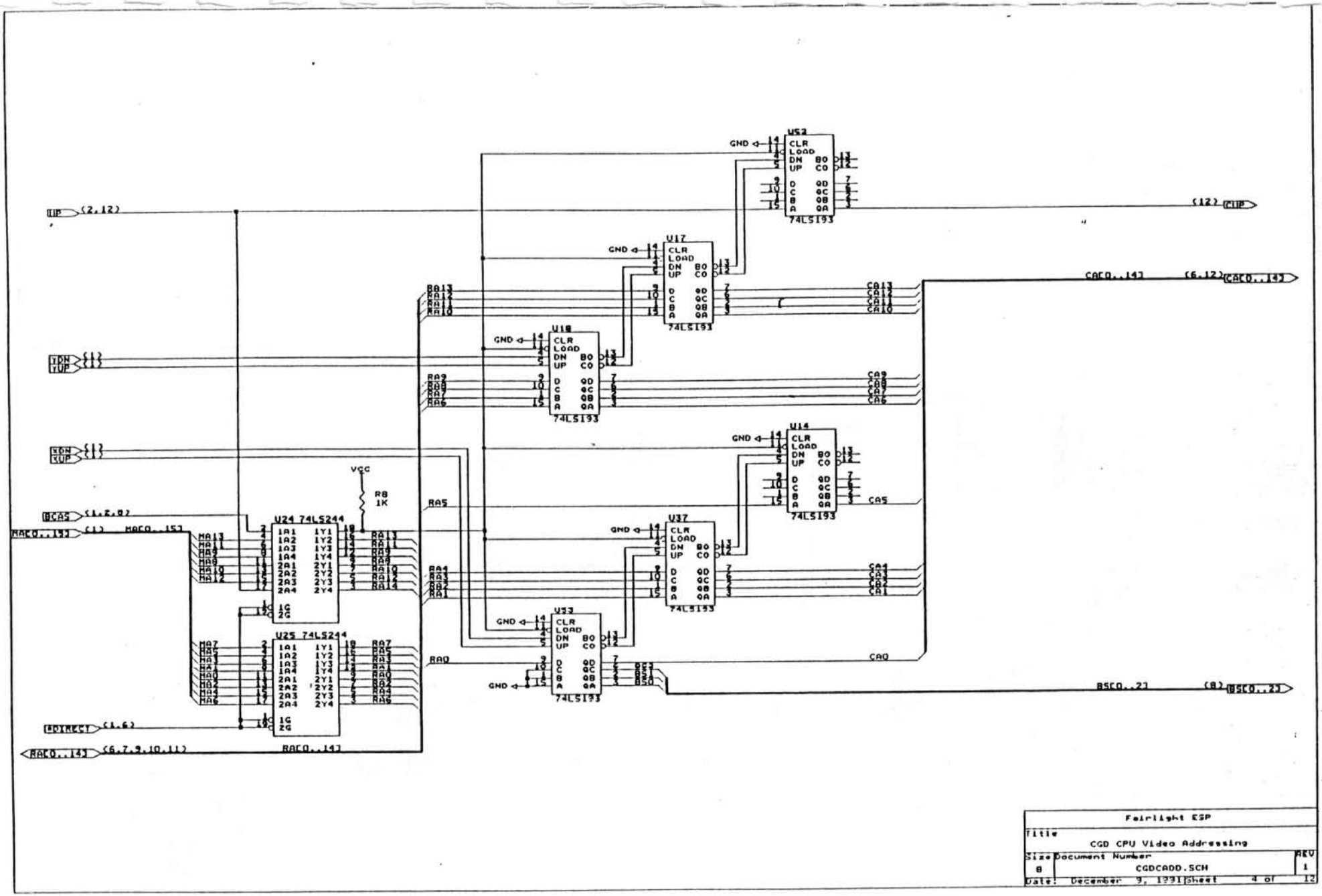
Date: December 11, 1331	Sheet 3 of 12	



Fairlight ESP		
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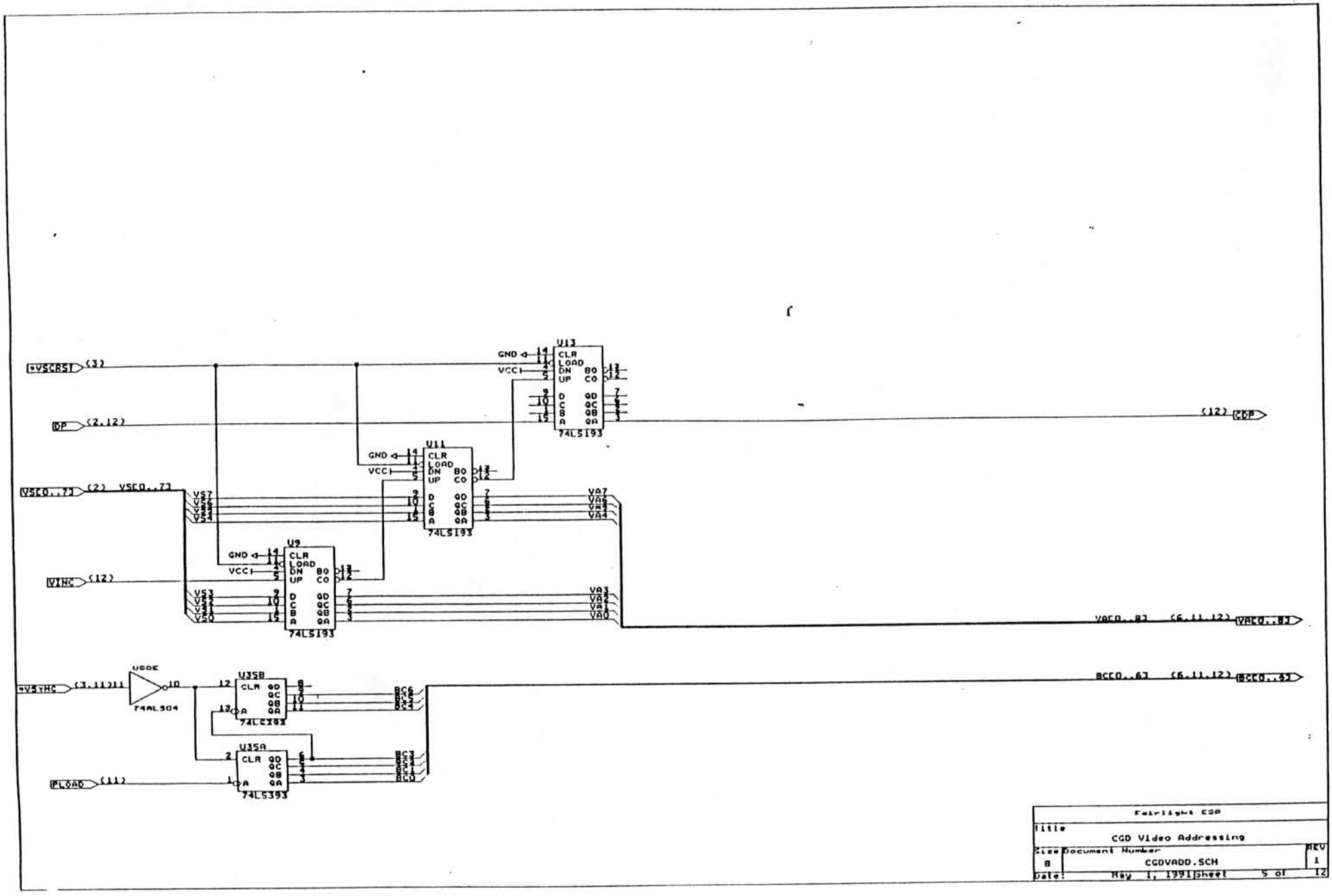
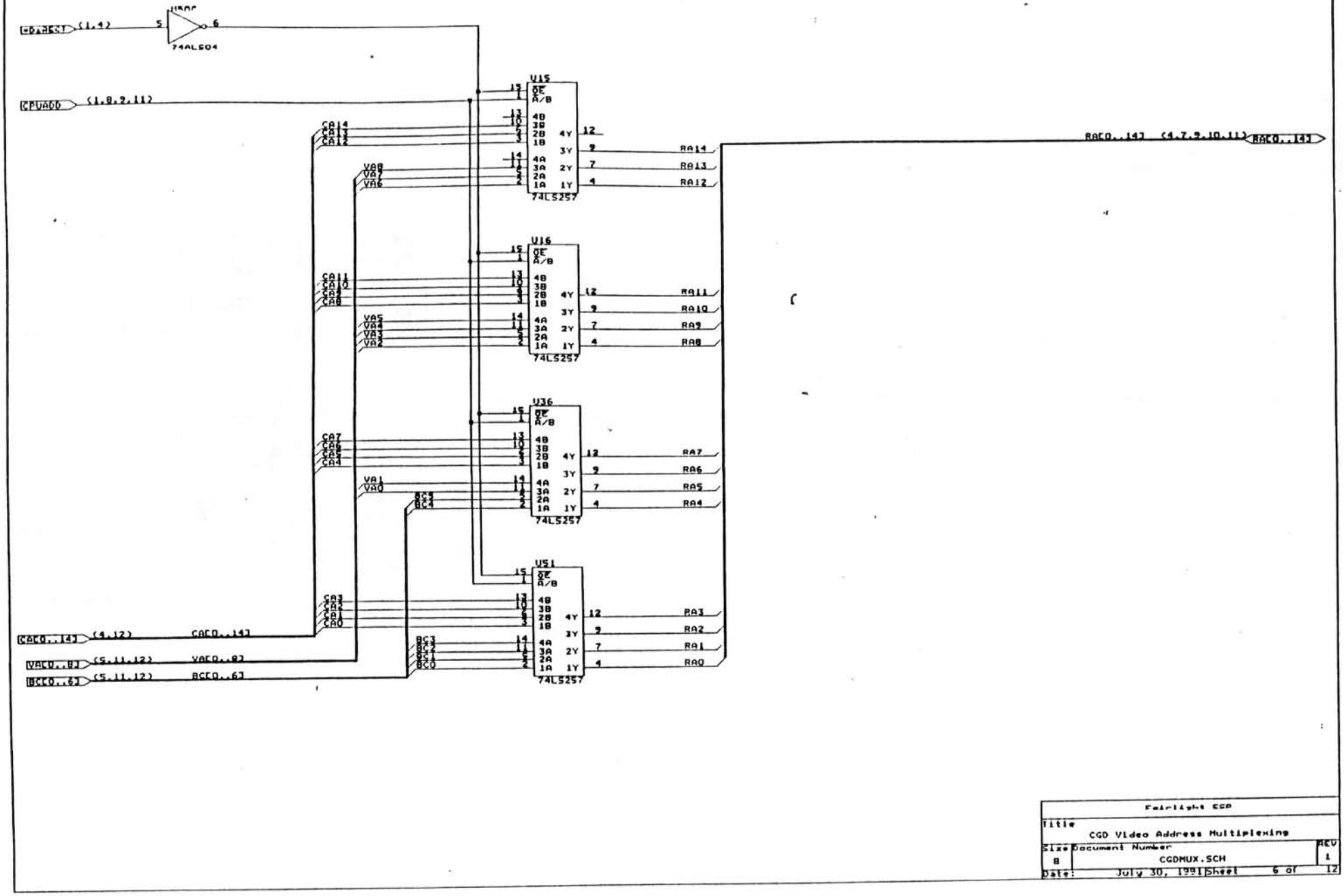
Date: December 9, 1991	Sheet 4 of 12	


U13
74LS193
U11
74LS193
U9
74LS193
U50E
74ALS04
U35B
74LS393
U35A
74LS393
GND
VCC
CLR
LOAD
DN
UP
BO
CO
D
C
B
A
QD
QC
QB
QA
•VSCRSI (3)
DP (2,12)
VSC0..7] (2) VSC0..7]
VINC (12)
•VSYNC (3,11)11
PLOAD (11)
(12) CDP
VAC0..8] (6,11,12) VAC0..8]
BCC0..6] (6,11,12) BCC0..6]
Fairlight CGP
Title
CGD Video Addressing
Size B
Document Number
CGDVADD.SCH
REV 1
Date: May 1, 1991 Sheet 5 of 12


U15C
74ALS04
U15
U16
U36
U51
74LS257
CPUADD (1,8,9,11)
CACO..14] (4,12)
VACO..8] (5,11,12)
BCCO..6] (5,11,12)
RACO..14] (4,7,9,10,11)
RA14
RA13
RA12
RA11
RA10
RA9
RA8
RA7
RA6
RA5
RA4
RA3
RA2
RA1
RA0
Fairlight CGP
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CGD Video Address Multiplexing
Size B
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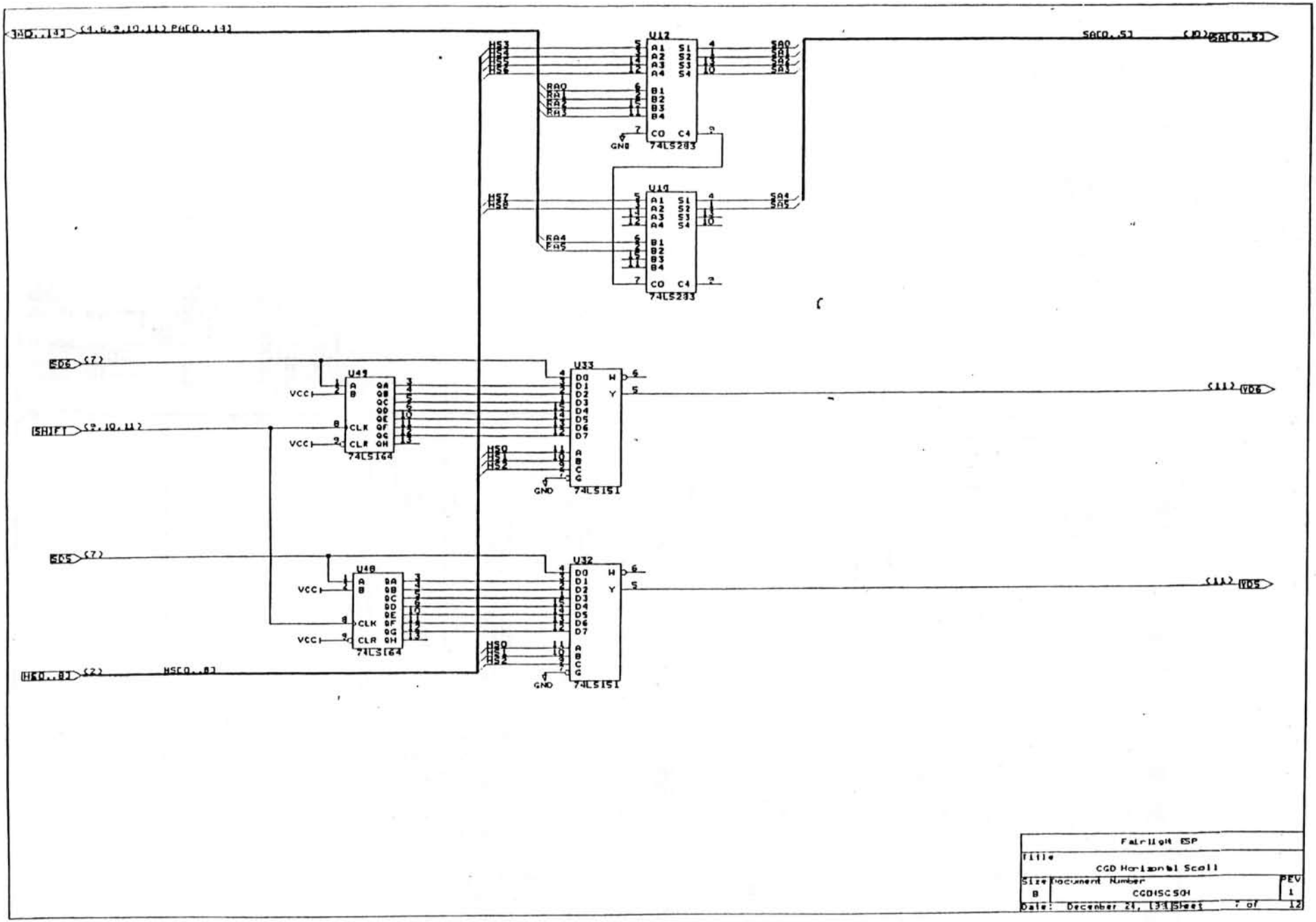
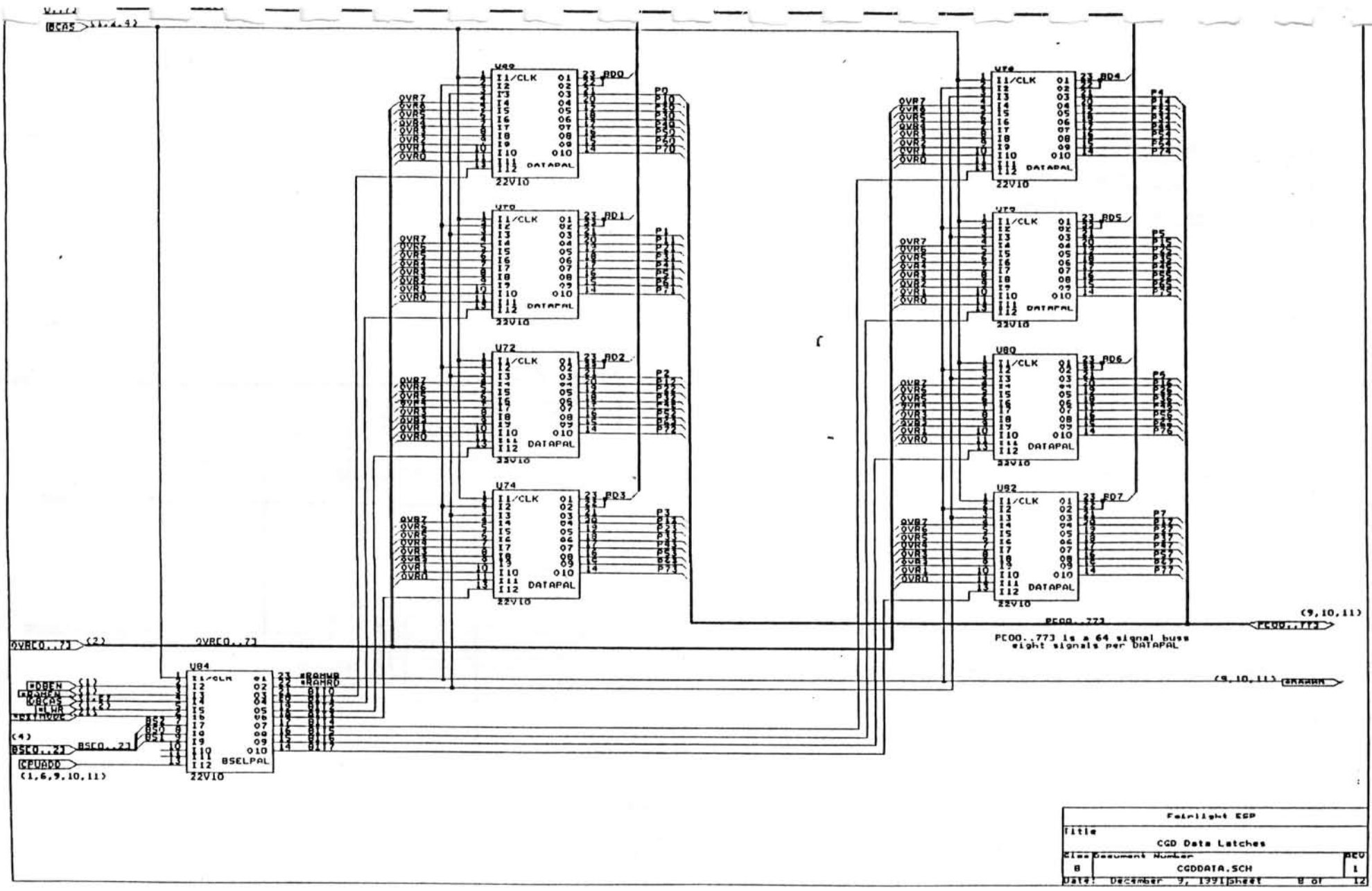
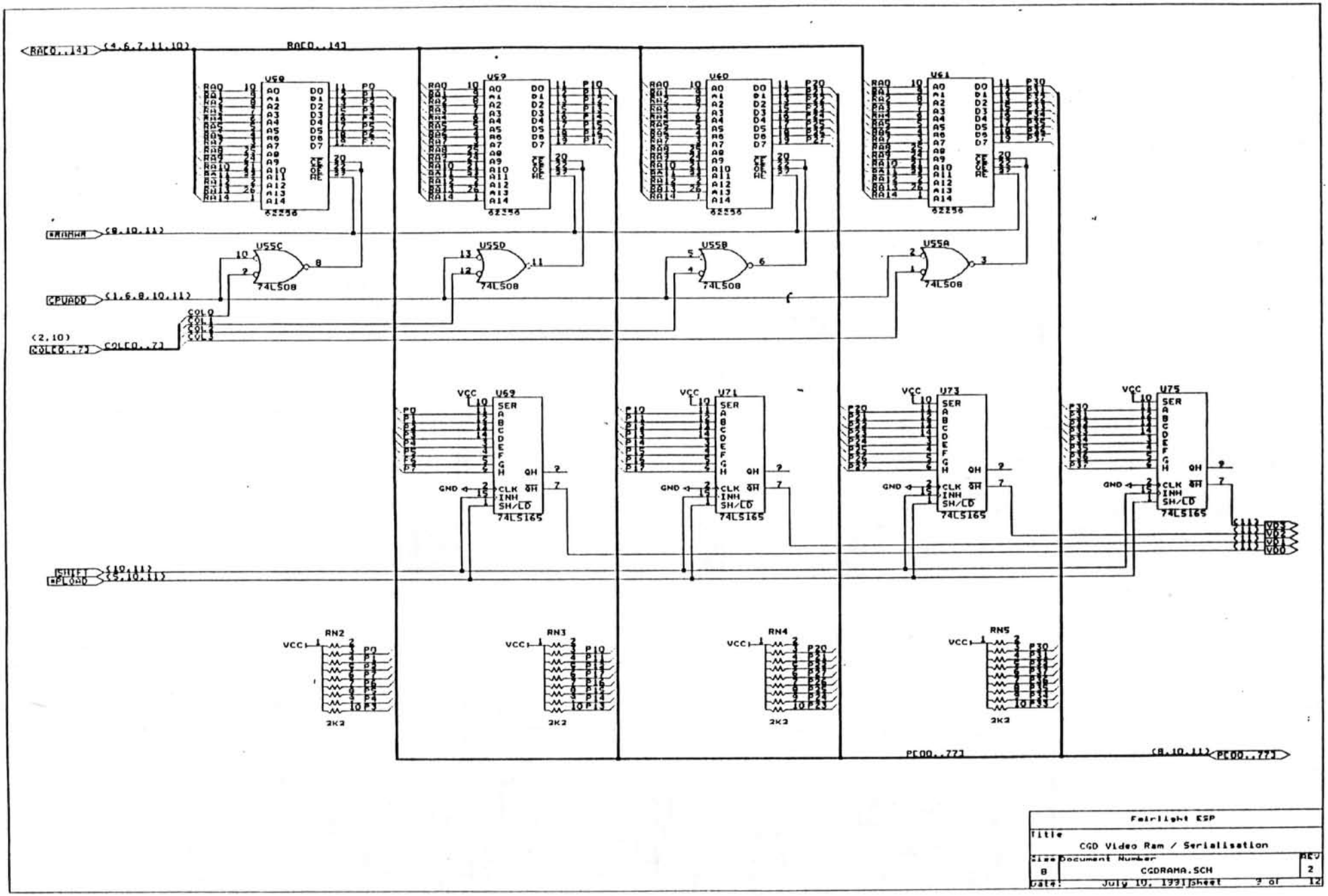
REV 1
Date: July 30, 1991 Sheet 6 of 12


PAD..19]
(4,6,9,10,11) PACO..19]
U12
74LS283
U10
74LS283
SACO..5]
(2) SACO..5]
SD6 (7)
U49
74LS164
U33
74LS151
(11) VD6
SHIFT (9,10,11)
SD5 (7)
U48
74LS164
U32
74LS151
(11) VD5
HSO..8] (2)
HSCO..8]
VCC
GND
Fairlight ESP
CGD Horizontal Scroll
CGDISCSOH
December 21, 19
Sheet 7 of 12


BCAS (1,4,9)
U69
U78
U72
U74
U76
U80
U82
U84
22V10
DATAPAL
BSELPAL
OVR7
OVR6
OVR5
OVR4
OVR3
OVR2
OVR1
OVR0
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
P0
P1
P2
P3
P4
P5
P6
P7
OVRC0..7] (2)
OVRC0..7]
BSC0..2]
CPUADD
(1,6,9,10,11)
(4)
(9,10,11)
PC00..77]
PC00..77] is a 64 signal buss
eight signals per DATAPAL
Fairlight ESP
title
CGD Data Latches
Size
B
Document Number
CGDDATA.SCH
REV
1
Date: December 9, 1991
Sheet 8 of 12



Fairlight ESP		
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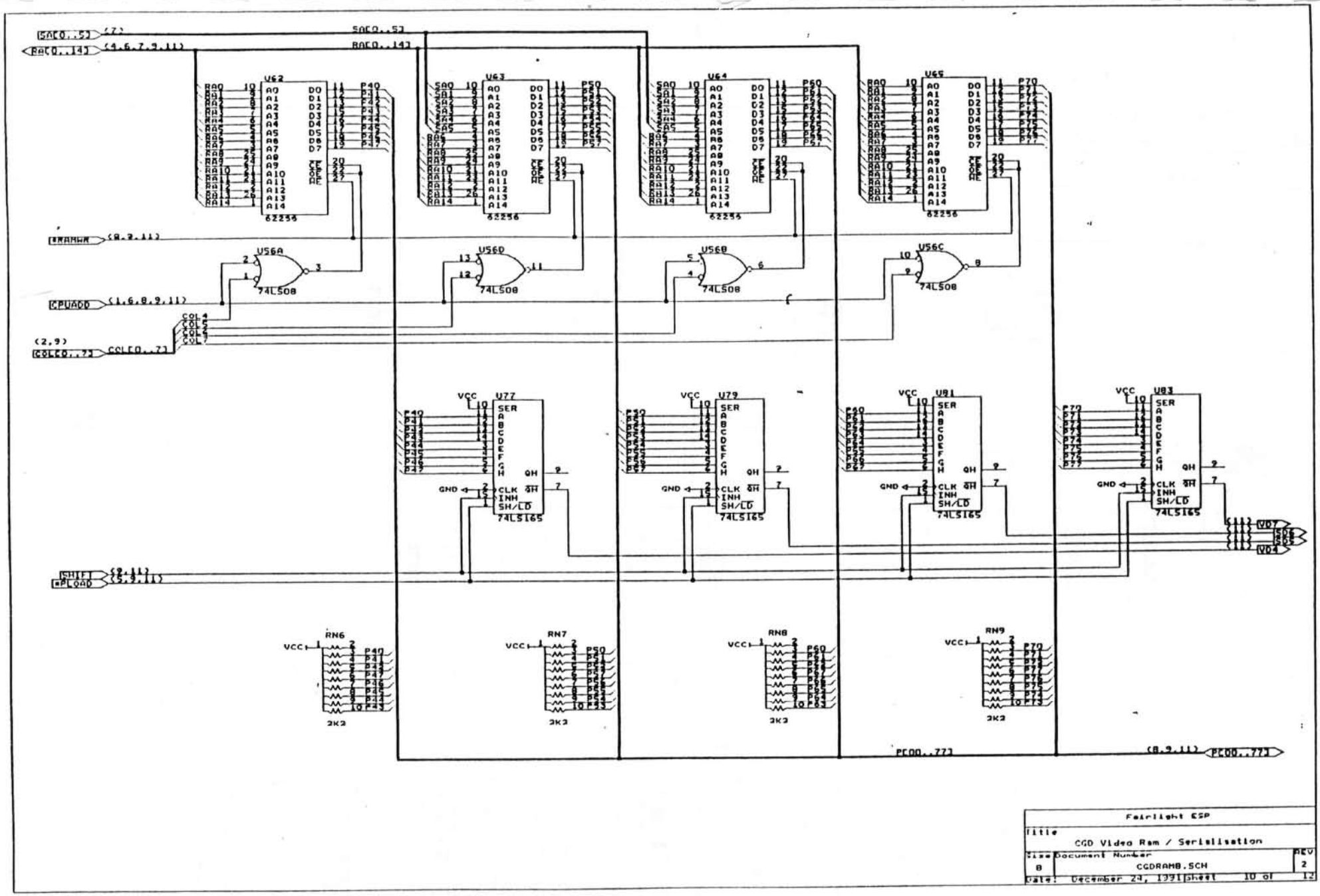
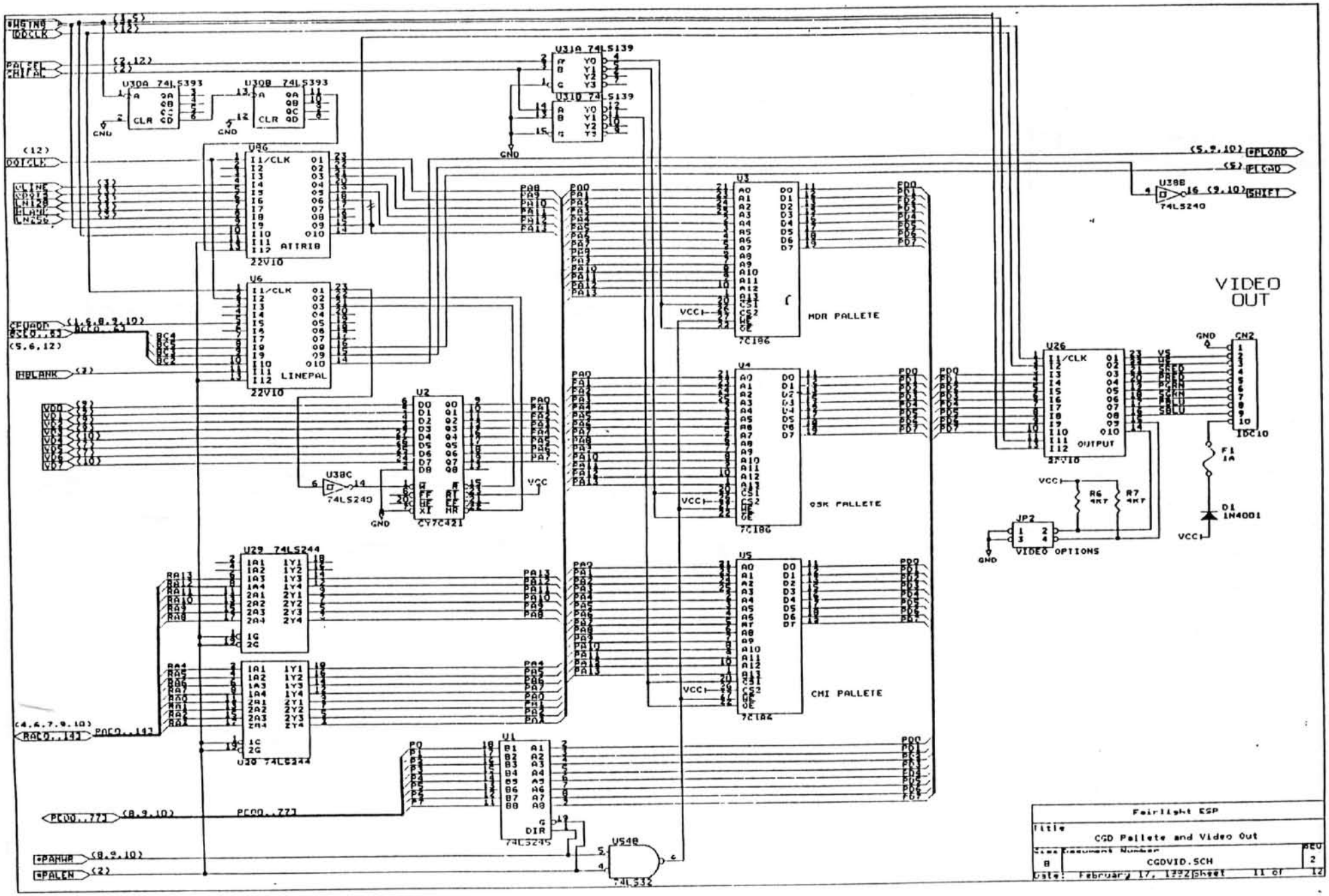
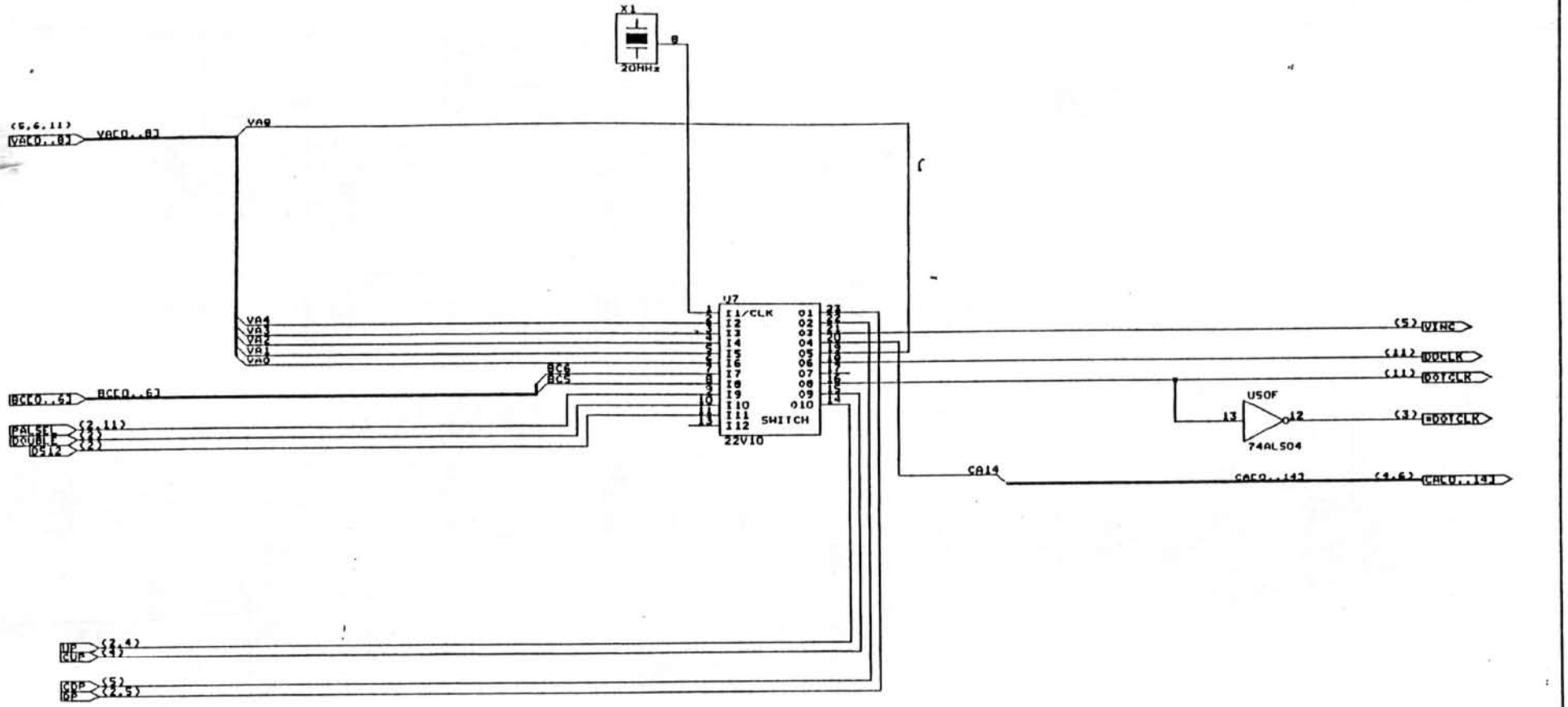
Size: B	Document Number: CGDRAMA.SCH	REV: 2
Date: July 10, 1991	Sheet 3 of 12	


SAC0..5
RAC0..14
U62
U63
U64
U65
62256
*RAMWR
U56A
U56D
U56B
U56C
74LS08
CPUADD
COL4
COL5
COL6
COL7
COLC0..7
U77
U79
U81
U83
74LS165
SER
QH
CLK
INH
SH/LD
GND
VCC
VD7
VD6
VD5
VD4
SHIFT
*PLOAD
RN6
RN7
RN8
RN9
2K2
PC00..7
Fairlight ESP
CGD Video Ram / Serialisation
CGDRAMB.SCH
December 24, 1991
Sheet 10 of 12



* ATTRIB/1B ↔ ATTRIB/5


X1
20MHz
U7
SWITCH
22V10
USOF
74ALS04
Fairlight ESP
CGD Video Mode Switching
CGDSWITCH.SCH
July 10, 1991
Sheet 12 of 12

JP1

Pin 1 GND

2 Vert. Sync

3 Horz Sync

4 Secondary Red

5 Primary Red

6 Primary Green

7 Secondary Green

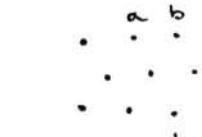
8 Primary Blue

9 Secondary Blue

10 +5V

VGA DB-15

View from ~~top~~ track side



a Vertical

b Horizontal

c 5V

d analog o/ps

e " "

f " "