QFC-9

FLOPPY DISK CONTROL CARD

Fairlight

FIELD CHANGE NOTICE

DATE 8/ 7 /92
NUMBER 94

ORIGINATOR Chris Alfred

PRODUCT: CMI / MFX

ASSEMBLY No. QFC-9 **DESCRIPTION** Floppy disk control card

This FCN applies to REV No: REV 6A.0 **The New REV No is:** REV 6A.2

REASON FOR CHANGE:

To correctly modify card for 8" or 3.5" floppy drives.

DETAILS OF CHANGE:

1. Check that the information described in FCN -1 and FCN -5 is done. See attached sheets.

2. Remove pin 8 from RN-1 (150 ohm), and install EPROM rev DQFC911.

Mark board for use only with 3.5" drive.

In the case where the card is used with an 8" drive check FCN -1 and FCN -5 have been done and that EPROM rev. DFQC910 is in place.

ORIGINATOR: DATE:

SERVICE MANAGER: DATE:

Address Map
(refer schematic QFC9-01)

The controller is accessed through two locations, in a memory map which enables access to peripherals. An address register is set up to point to the required controller register. All data is read or written through a single data register.

ADDRESS (HEX)	READ	WRITE
FCE0	data	data
FCE1	status register	address register

The 7 controller registers are:

00	control register
02	DMA address (low byte)
04	DMA address (high byte)
06	byte count to read/write (low byte, inverted)
08	byte count to read/write (high byte, inverted)
0A	command location to load device driver ROM into RAM
	WD1791 L.S.I
0C	cmd (write) status (read)
0D	track
0E	sector
0F	data

The definitions of the control register bits are:

0	DS0 drive select address bit 0
1	DS1 drive select address bit 1
2	enable interrupt (active high)
3	enable DMA address incrementing (active low)
4	DMA transfer direction (1= to disk)
5	side select
6	retrig head load timer
7	DENS density selection

The definitions of the control status bits are:

0	0
1	n/c
2	n/c
3	ready
4	two sided
5	disk change
6	interrupt
7	device driver loading (active low)

Commands

The extensive instruction set of the 1791 LSI can be obtained from the manufacturers data sheets for the 1791. This device handles all data conversions between the disk drive and the CMI buss.

DMA address Counters

(refer schematic QFC9-02)

Sixteen bit counter chain C1 to C4 is used to provide the address for DMA transfers. The starting address for each disk transfer is established by writing the appropriate byte address to the address register then writing the address byte to the data register and then repeating for the other address byte. This causes the address to be preset into the DMA address counters by means of parallel-load strobe pulses STAL (low byte) and STAH (high byte). The incrementing of the DMA counters may be inhibited under software control, so that disk data may be dumped directly into the data portholes on channel cards.

DMA Byte Transfer Counters

(refer schematic QFC9-04)

Sixteen bit counter chain C5 to C8 is used to transfer the required number of bytes to or from disk. It must be initialized with the inverse of the number of bytes to be transfered. Any number may be specified up to a maximum of 65,535 bytes. Only those bytes specified will be tranferred to memory on a disk read. This allows less than a sector to be read from disk, and saves the software overhead required to handle partial sector reads. The read takes place but the buss VMA signal goes inactive after the required number of bytes have been transferred, so disabling memory writes. The VMA disable signal is generated from the ripple carry out on this counter chain, by buffering /FINPS, (Finished Partial Sector).

When a transfer occurs, the DMAC (Direct Memory Access Claim) line is generated so that the memory card swaps maps, allowing data to be dumped into memory currently not mapped into the processor's address space. This signal is generated by the components around flip-flop A11.

Data Buffers

(refer schematic QFC9-02)

Data is propagated from the system data bus via latch B6 which hold the data across the processor 1 phase. This latched data also becomes the DATA FROM BUS via buffer B5, to the floppy-controller LSI.

Data written to the system control register at 00 is latched by B7. This controls such functions as drive select and DMA direction.

Address Decoding

Address range $FCE0-$FCE1 is decoded by gates B1, E1, B2, E1 and latched by D2.

Address $FCE0 is used to enable the internal data buss to read and write to controller functions.

Address $FCE1 data is latched by B8 and with the access to FCE0 generates the internal chip selects and read/write strobes through C9.

Inverting buffer E5 and open collector drivers E6, E7 are used to interface the 1791 LSI controller to the disk drive cable. Incoming disk status signals are pulled up by 150 ohm terminating resistors.

Controller LSI

The Interupt Request from the LSI is gated with the Interupt Enable to provide an open-collector interupt signal for the system I.R.Q. on buss pin 63A.

DMA Logic

(refer schematic QFC9-03)

Data requests from the 1791 or Device Driver rom loading are synchronised with Processor 2 Phase 2 using flip-flops C1 and A10. This sets up a DMA request to the processor (RDMA).

DMA cycles are granted by ACK acknowledge signal.

Flip-flop A11 only allows a DMA cycle to occur every second Processor cycle (the floppy drive can not transfer at that rate but this is a system constraint on other DMA devices in the DMA daisy chain).

The DMA daisy chain is controled by /ENL and /EDL. Respectively these stand for, Enable Next Level and Enable Dma Level. When /EDL is active, a DMA request may be requested by the highest priority device. The /ENL signal informs the next device in the daisy chain that it may make a request if higher priority devices have not.

Depending on which function has been requested (Reset, Read, write) the required DTB (Data to Bus), and ATB (Address to Bus) signals are issued.

Control Register

The control register contains the drive number select bits, density selection, interupt enable, increment DMA address enable, data transfer direction, side select and retrigger head load delay.

This register is the latch at B7.

The "retrig head" signal is used to reactivate the head load delay when the drive number has been changed, to allow for head bounce.

Master Oscillator

(refer schematic QFC9-05)

The LSIs used on the card require a master 16MHz clock. This is generated with the components around the 74S04 at F5. The FDC9229 generates the 2 MHz clock for the 1791, by dividing this internally.

Write Precompensation

In double density operation there may be a time shift applied to the data when it is being written to the inner disk tracks (>45). The amount of shift is determined by the LSI and the floppy disk suport device 9229. They produce a programmable delay of 1 to 3 clock cycles.

The amount, if any, is specified by the drive manufacturer. Links W4, W5, W6, W7 select the amount. The amount on inner and outer tracks can be independently set.

W5	W6	W7	Precompensation Value (in,nS)
0	0	0	0
0	0	1	62.5
0	1	0	125
0	1	1	187.5
1	0	0	250
1	0	1	250
1	1	0	312.5
1	1	1	312.5

The precompensation value is normally set to 0 on inner and outer tracks. It is more important on inner tracks as the bit density on the disk is greater.

W4 selects minifloppy drives and also requires the board to be made with a 34 pin connector (or a special cable) and an 8MHz crystal.

Data Separator

The serial data stream that comes from the drive is in a synchronous form. It has embedded the required data as well as clock pulses and synchronization "marker bytes".

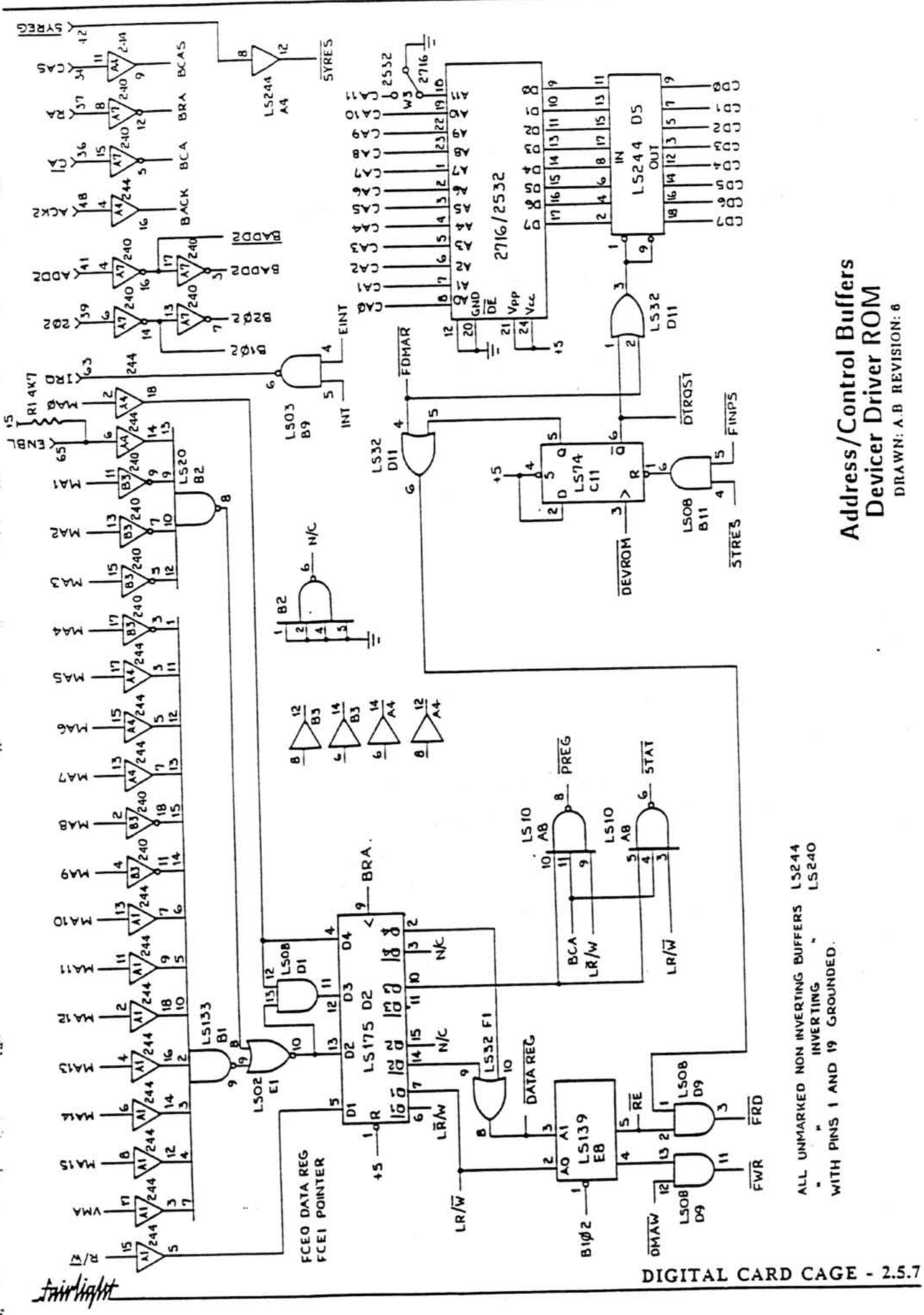
The data separator is used to generate the data window from the FM (single density) or MFM (double density) encoded READ DATA supplied by the disk drive. The separator tracks, so that incoming data is always in the center of the data window. This data window informs the controller chip which bits in the data stream it is receiving are data and which are clock bits just used in the data encoding scheme.

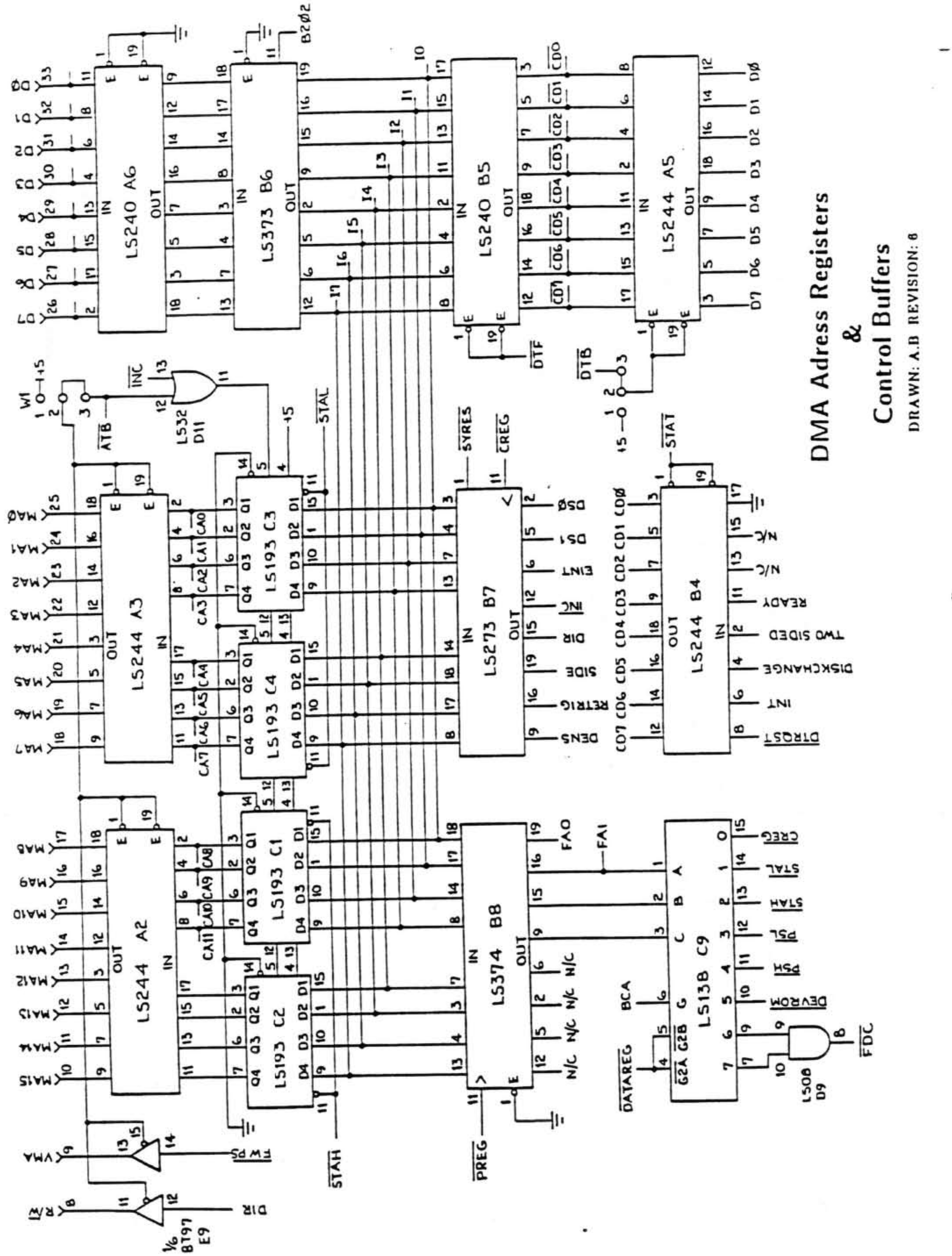
The separator is a digital phase locked loop in the FDC9229 chip at E10. This chip does all the work of data separation.

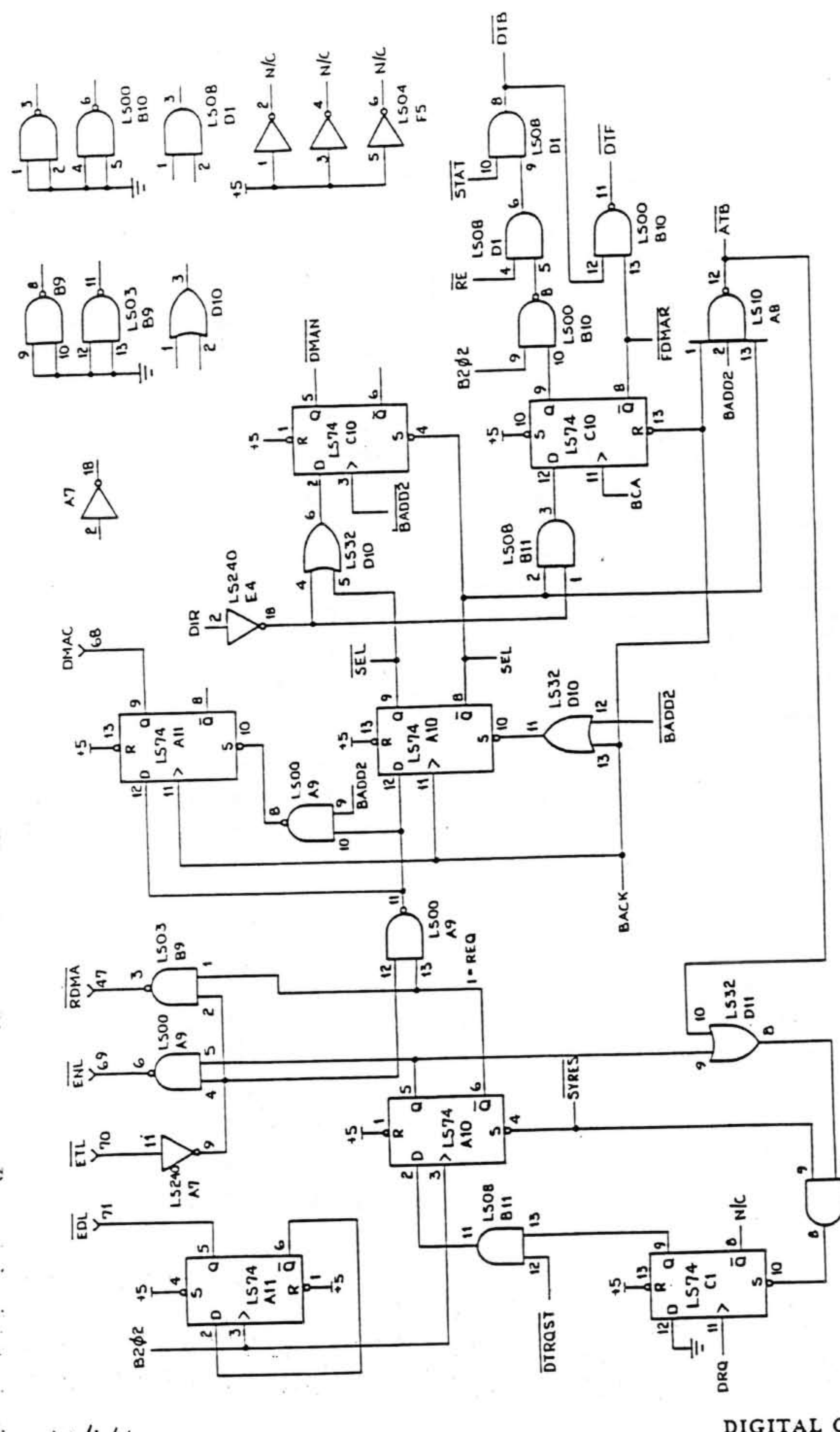
Device Driver ROM

The disk controller software may be placed in a 2K or 4K EPROM on the controller card. This EPROM is not in the processor's directly addressable memory. It is executed by reading the software into RAM. This is done by DMA. The EPROM is copied into RAM as if reading a disk, except much faster.

The least significant DMA counter lines are used as addresses on the EPROM, so the EPROM can only be loaded into memory on 2k or 4k boundaries. The flip-flop C11 and gates in D11 and B11 produce a DMA write to memory request that is terminated after the byte counter times out.

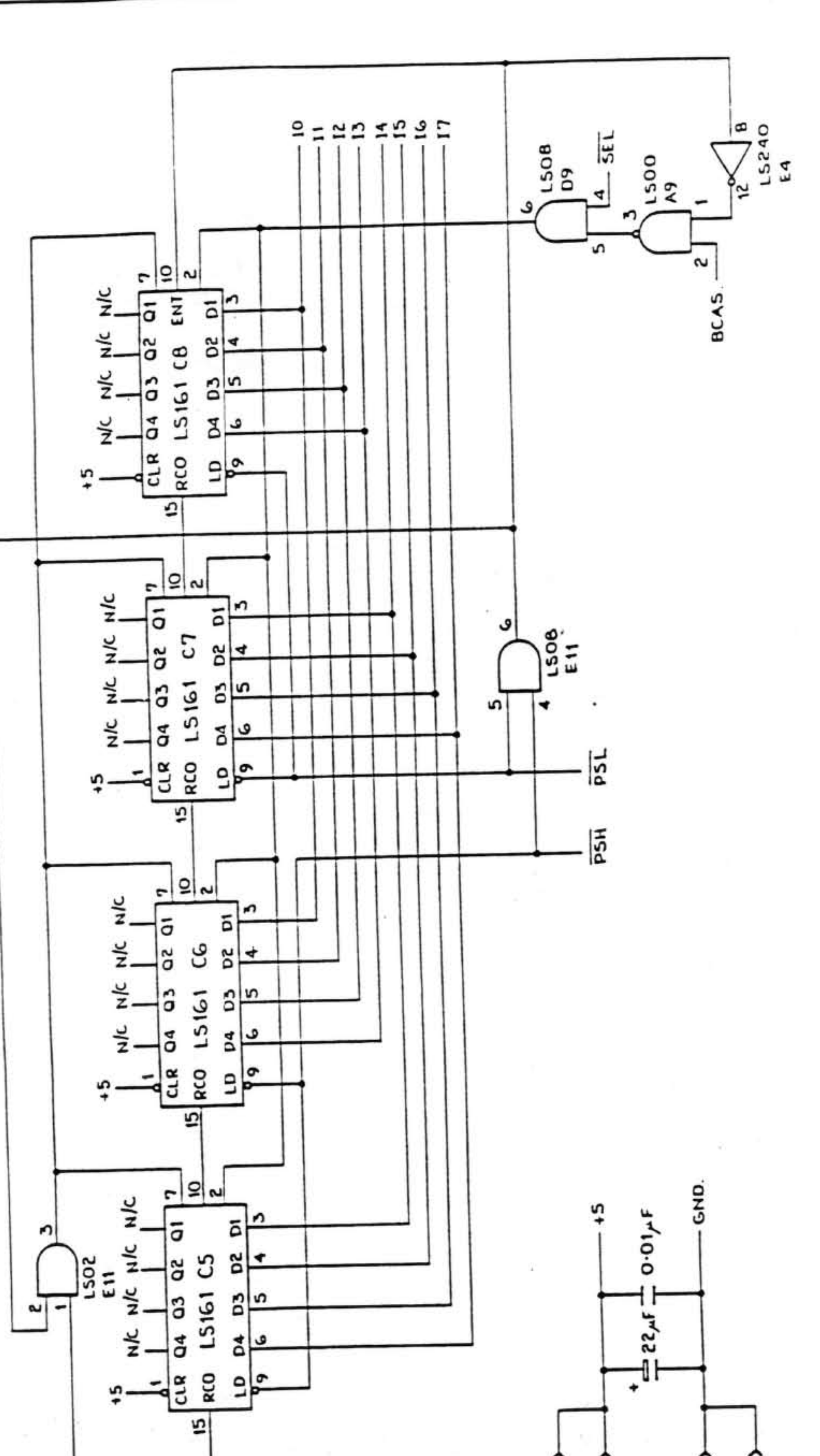

Address/Control Buffers
Devicer Driver ROM
DRAWN: A.B REVISION: 6
ALL UNMARKED NON INVERTING BUFFERS LS244
" INVERTING " LS240
WITH PINS 1 AND 19 GROUNDED.
FCEO DATA REG
FCE1 POINTER
2716/2532
LS244 D5
LS175 D2
LS139 E8
LS74 C11


DMA Adress Registers
&
Control Buffers
DRAWN: A.B REVISION: B



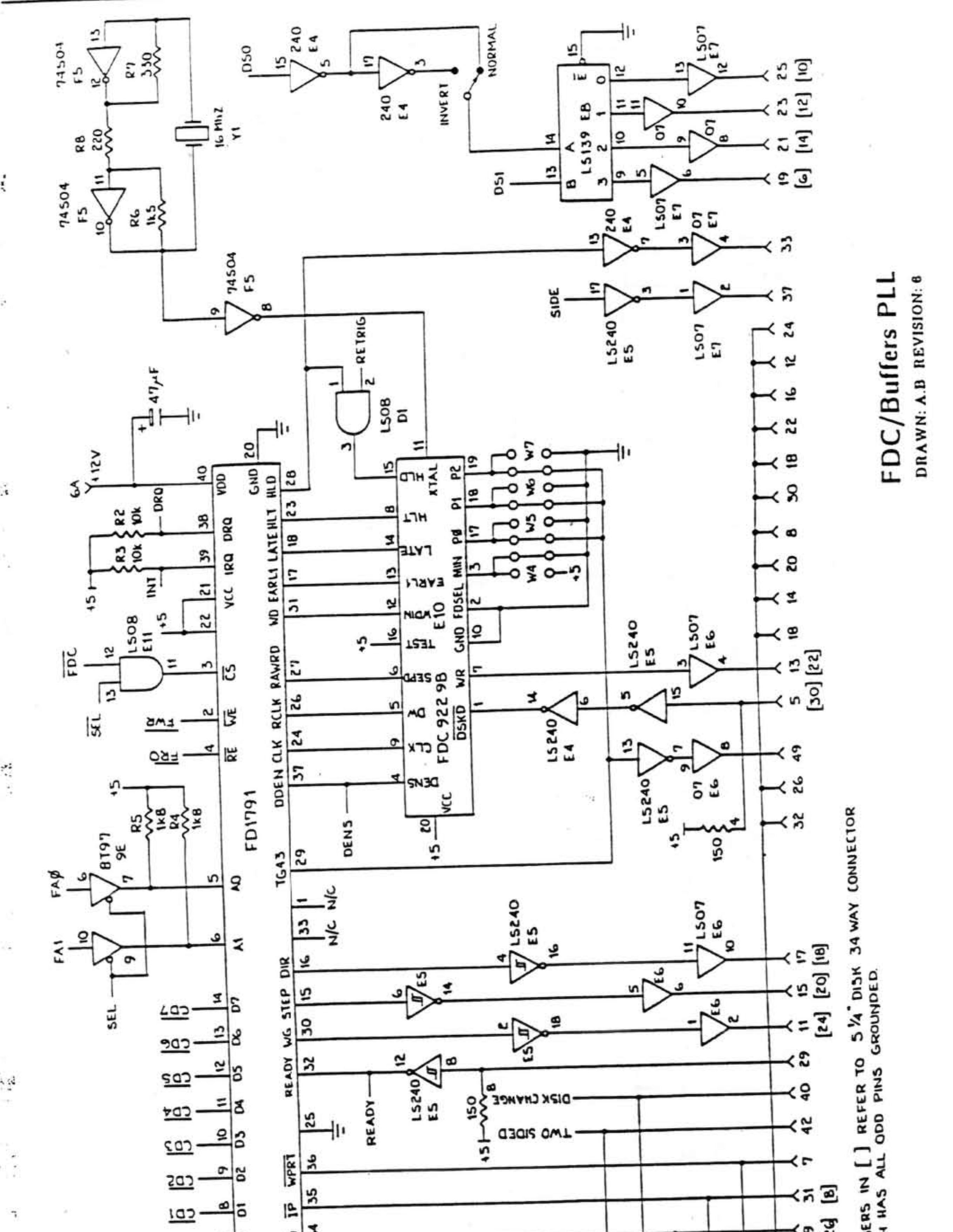
DMA Logic Daisy Chain

DRAWN: A.B REVISION: 6



Byte Transfer Counter

DRAWN: A.B REVISION: 6


FDC/Buffers PLL
DRAWN: A.B REVISION: 6
NUMBERS IN [ ] REFER TO 5 1/4" DISK 34 WAY CONNECTOR
WHICH HAS ALL ODD PINS GROUNDED.
FD1791
FDC 9229B

Cable Connector Signals

DRAWN: A.B REVISION: 6

1		2	GND
3		4	HDL3
5	READ DATA	6	HDL2
7	WRITE PROTECT	8	
9	TRACK Ø	10	
11	WRITE GATE	12	
13	WRITE DATA	14	
15	STEP	16	
17	DIRECTION	18	
19	DS4	20	
21	DS3	22	
23	DS2	24	
25	DS1	26	
27		28	HD.L1
29	READY	30	
31	INDEX	32	
33	HEAD LOAD	34	HDLØ
35	ALT	36	IN USE
37	SIDE SELECT	38	
39		40	DISK CHANGE
41		42	TWO SIDE
43		44	
45		46	
47		48	
49	LOW CURRENT	50	