Q133

DEBUG CARD

fairlight ORIGINAL

FIELD CHANGE NOTICE

DATE 16/ 08/ 93

NUMBER 134

ORIGINATOR Chris Alfred **PRODUCT: CMI / MFX**

ASSEMBLY No. Q133 **DESCRIPTION** DEBUG CARD

This FCN applies to REV No: 9 **New REV No is:** 9.1

REASON FOR CHANGE:

ENSURE CLOCK DOES NOT LOOSE TIME AT EACH SWITCH ON AND CALLIBRATION OF CLOCK.

DETAILS OF CHANGE:

(1) REMOVE THE BATTERY

(2) CUT COMPONENT SIDE TRACK BETWEEN RN1/10 (10K) AND U8/10 (68B21)

(3) CUT SOLDER SIDE TRACK TO R23 ON SIDE NEAREST BATTERY

(4) CONNECT 10K RESISTOR BETWEEN U7/18 (5832) AND U7/14

(5) CONNECT 10K RESISTOR BETWEEN U7/2 AND U7/14

(6) REPLACE BATTERY

(7) MARK THE PCB AS REV 9.1

NOTE: /## INDICATED THE PIN NUMBER OF THE DEVICE.
(##) INDICATED PART VALUE OR PART NUMBER.

ORIGINATOR:	DATE:	TEST:	DATE:
		PROD: J Gavin	DATE: 19/07/93
SERVICE:	DATE:	KIT LIST CHANGE:	YES NO

fairlight

FIELD CHANGE NOTICE

DATE 5/ 3 /93
NUMBER 121

ORIGINATOR Chris Alfred

PRODUCT: CMI / MFX

ASSEMBLY No. Q-133 **DESCRIPTION** D BUG CARD

This FCN applies to REV No: 7.2 and 8.0 **The New REV No is:** 7.3 and 8.1

REASON FOR CHANGE:
Lost time.

The system clock will loose time at each switch on. This is approximately 5 seconds each at power up. The system clock should also be adjusted for correct time calibration.

The changes to stop the switch on loss is optional, however it is recommended that the system clock be set per the instructions below.

DETAILS OF CHANGE:

1. Locate the MSM 5832 timer IC.

2. Cut track from pin 10 of resistor pack to pin 18 of the MSM 5832. Make sure the connection from pin 18 of MSM 5832 to pin 10 of the 6821 is still in place.

3a Lift R18 leg at the junction with R 19 (PUP line). For REV 7 PCB
3b Lift R23 leg at the junction with R 24 (PUP line). For REV 8 PCB

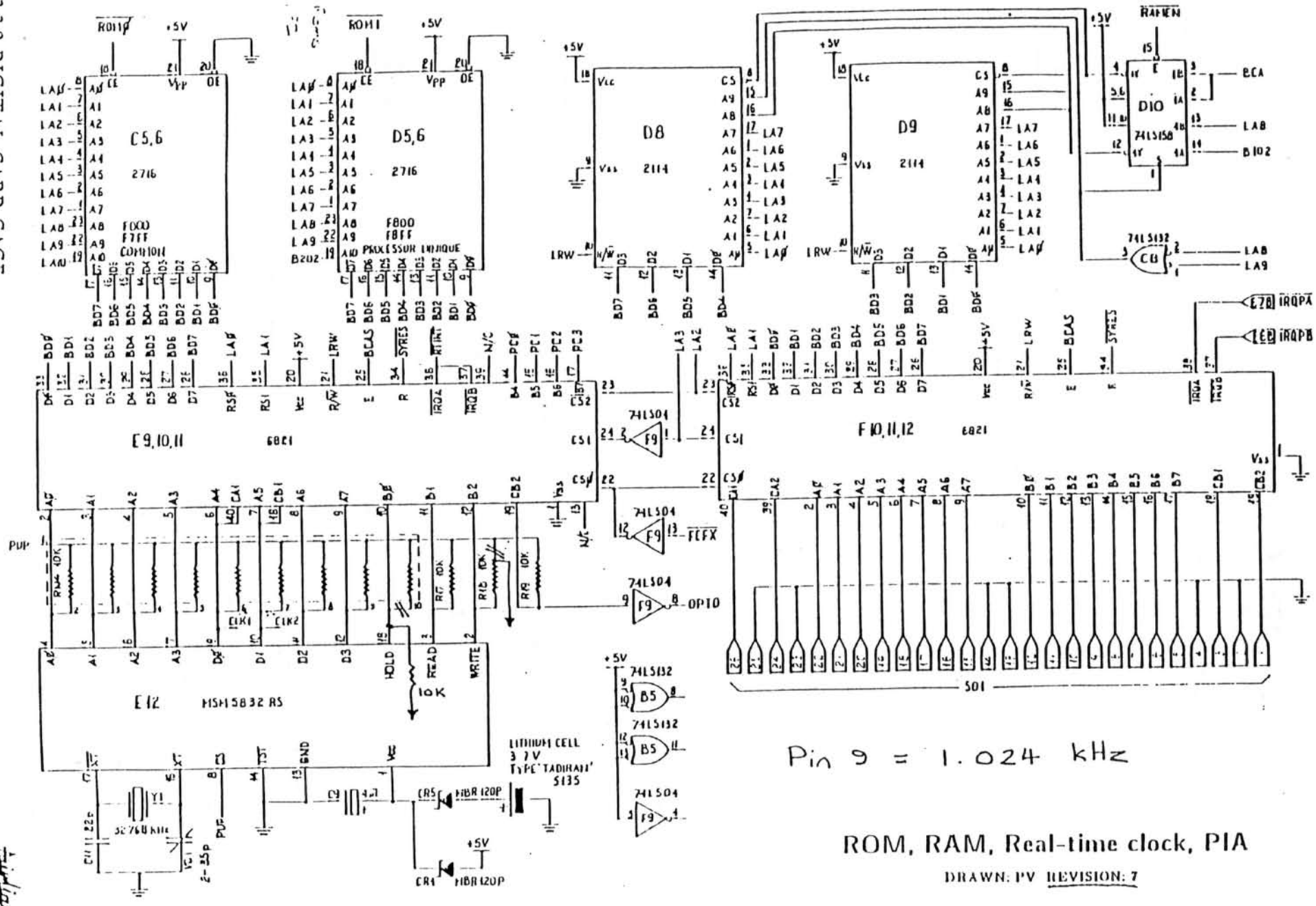
4. Add 10K resistor from pin 18 of MSM 5832 to 0V. For REV 7 & 8 PCB

5a Connect lifted leg of R18 to 0V. For REV 7 PCB
5b Connect lifted leg of R23 to 0V. For REV 8 PCB

6. Label new PCB revision number.

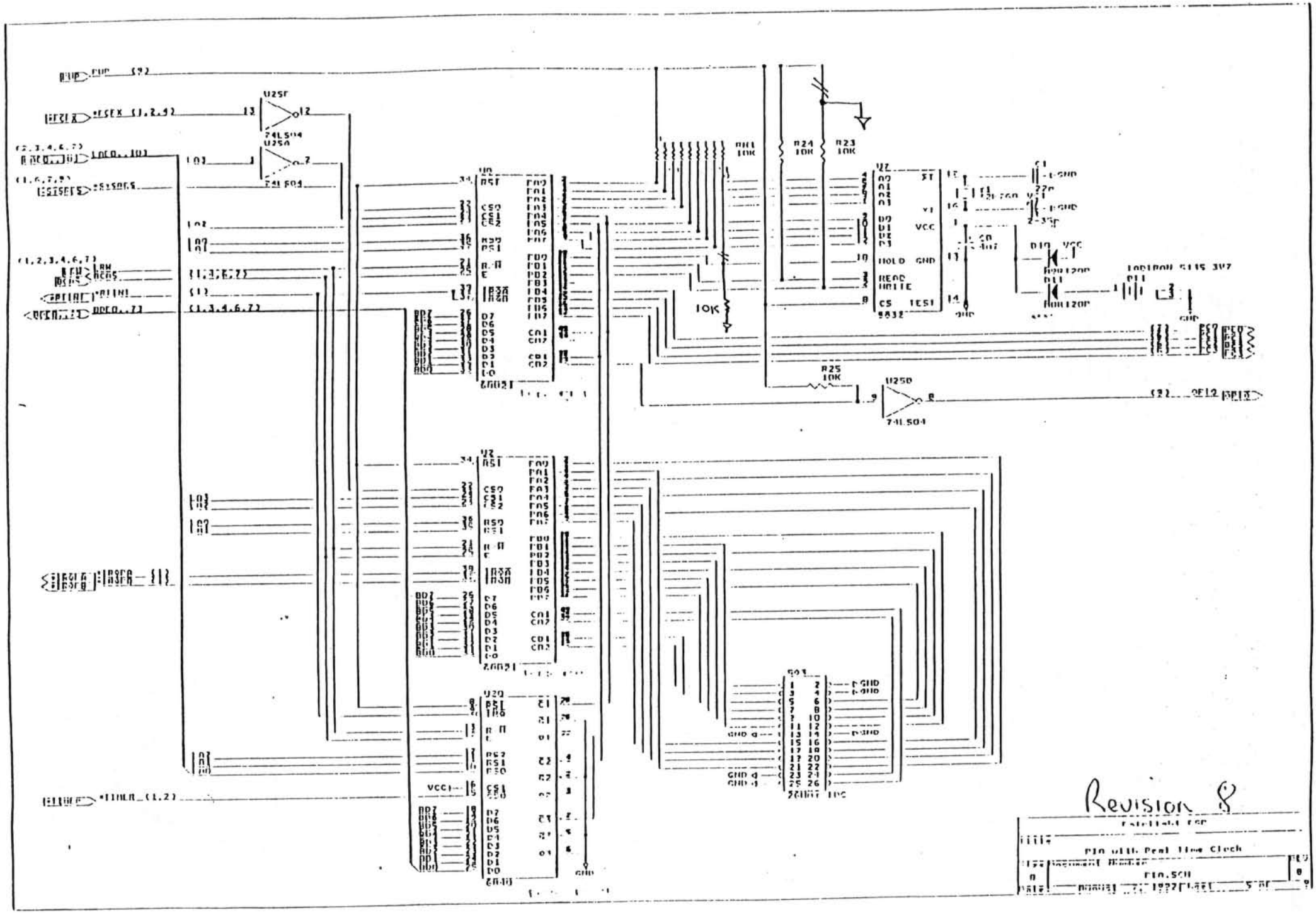
To adjust the clock. Set VC 1 so that the signal on pin 9 of the MSM 5832 is 1.024 KHz.
To set the time and date on the system. Go to the shell and type "SETIME"<ret>
Enter time and date then <ret>.

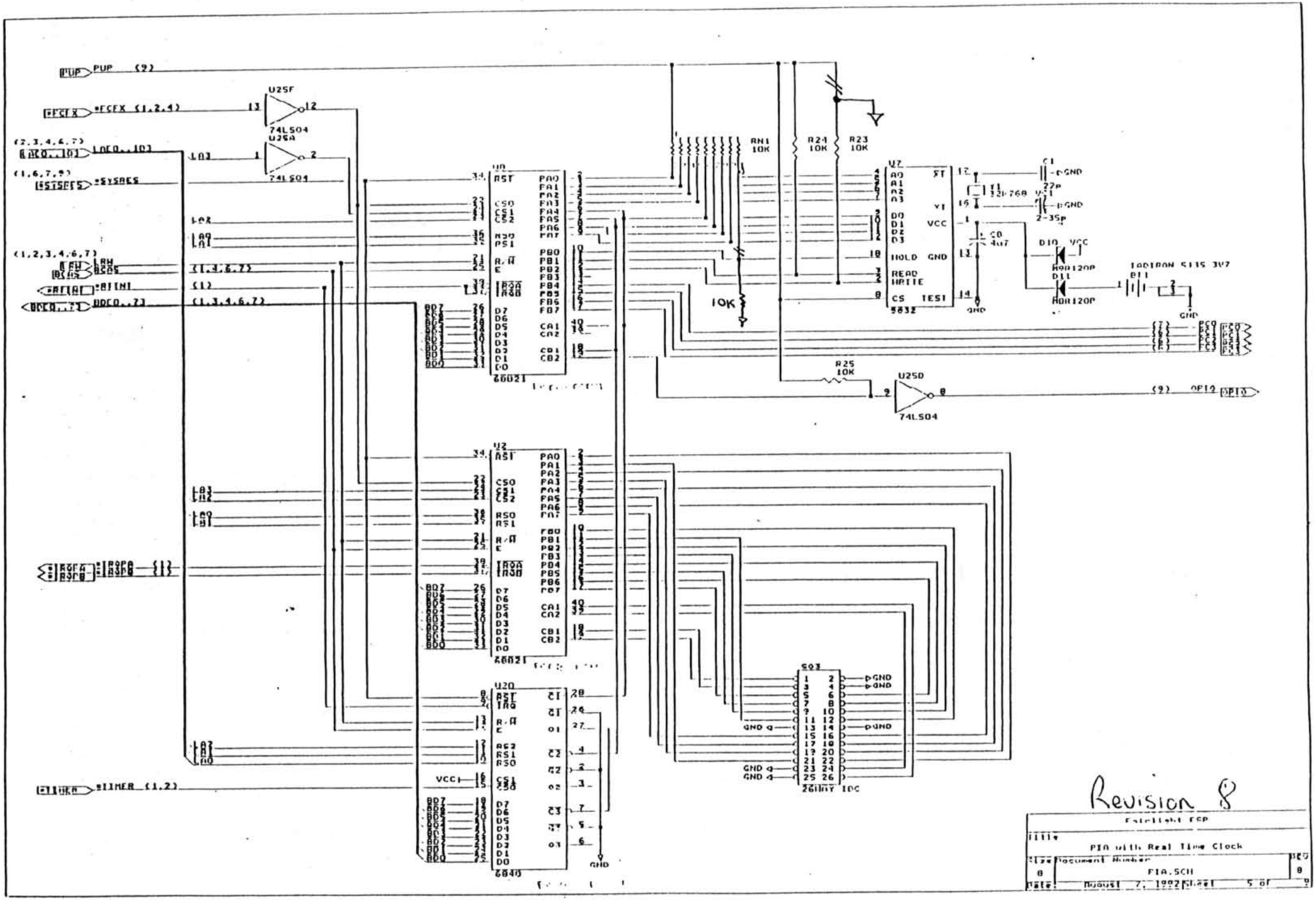
ORIGINATOR: [signature] DATE: 5-2-93	TEST: Marie Perkins 8/3/93 PROD: [signature] DATE: 8/3/93
SERVICE: DATE:	KIT LIST CHANGE: (YES) NO



ROM, RAM, Real-time clock, PIA

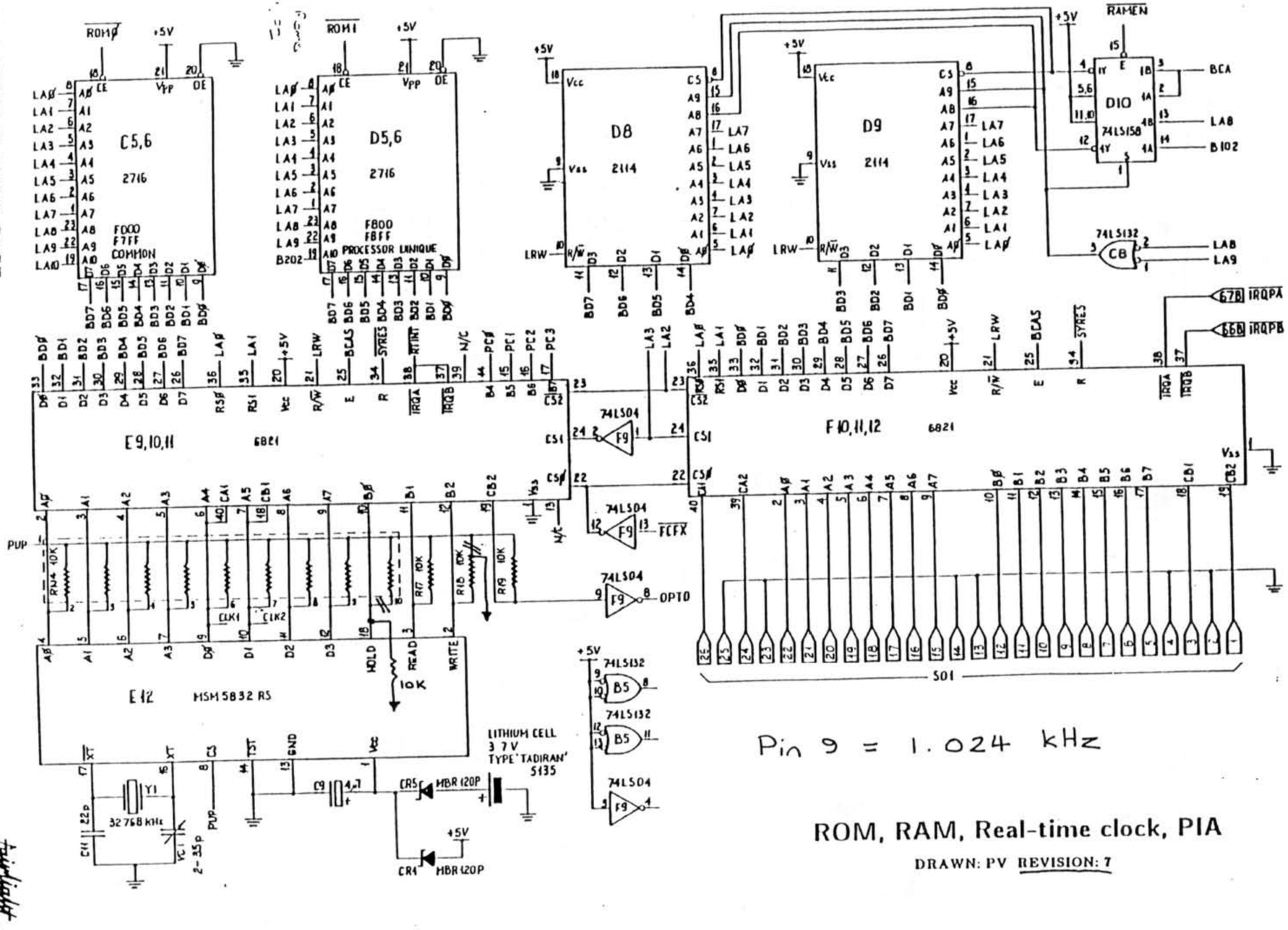
DRAWN: PV REVISION: 7


74LS04
74LS04
74LS04
R24 10K
R23 10K
R25 10K
10K
Revision 8
Pin with Real Time Clock



U25F
74LS04
U25A
74LS04
U25D
74LS04
U0
68B21
U2
68B21
U20
6840
U7
5832
RN1 10K
R24 10K
R23 10K
R25 10K
10K
Y1 32.768
C1 22p
C8 4u7
2-35p
D10
D11
HDR120P
B11
TADIRAN 5115 3V7
S03
26WAY IDC
Revision 8
Fairlight ESP
Title
PIA with Real Time Clock
Size Document Number
B
FIA.SCH
REV
8
Date: August 7, 1992 Sheet 5 of 9

Q133-01 CPU Control Card



ROM, RAM, Real-time clock, PIA

DRAWN: PV REVISION: 7

URGENT FAX TO ALL DISTRIBUTORS fairlight

SUBJECT: FIELD CHANGE NOTICE NO: 121

PLEASE REMOVE THE DE-BUG BATTERY

BEFORE MODIFYING THE DE-BUG CARD.

THANKS AND REGARDS,

SHANE MORRIS

19 MARCH 1993

fairlight

FIELD CHANGE NOTICE

DATE 21/ 10/ 92
NUMBER 108

ORIGINATOR Steve Rance **PRODUCT: CMI / MFX**

ASSEMBLY No. Q-133 **DESCRIPTION** D-BUG CARD

This FCN applies to REV No: Rev. 7.1 **The New REV No is:** Rev 7.2

REASON FOR CHANGE:
Unified ROMS for all revisions of CMI
Q219
CG-1
CG-2
CG-3

DETAILS OF CHANGE:

1. Replace ROM at location D5,6 with F 8 L M R K 17
2. Replace ROM at location C5,6 with Q 9 F 0 M R K 17

Must be done with(previously FCN-109 which is replaced by) FCN119 see attached.

Must be done in new card production.
Can be done to current cards in use.

Marco Paolucci 8/3/93

ORIGINATOR:	**DATE:**	**PROD:** Marco	**DATE:** 02/03/93
SERVICE:	**DATE:**	**KIT LIST CHANGE:**	**YES NO**

ESP

FIELD CHANGE NOTICE

Field Change Notice No 88

PRODUCT CMI Series III

ORIGINATOR: Chris Alfred **DATE:** 12 / 5 / 92

ASSEMBLY No: Q133

DESCRIPTION: CPU Control Card ('Debug Card')

This FCN applies to rev No: 6 and 7 **The New rev No is:** 6.1 and 7.1

REASONS FOR CHANGE:

The refresh address counter on the Q133 card does not refresh enough addresses causing random bit errors in Channel Card memory.
This FCN extends the refresh address to 8 bits.

Effect of this FCN
Fixes channel cards crashing.
Fixes channel memory errors.
Allows 150nsec DRAMS to be used on the channel cards.

DETAILS OF CHANGE:

1. Install a piggy back 74LS244 IC at A3 by bending out all pins except pins 1,10,19,20. Place the 74LS244 over A3 (74LS244) and solder pins 1,10,19,20 to the same pins on IC A3.

2. Connect pin 2 of piggy back 74LS244 to IC A2/13 (4040).

3. Connect pin 18 of piggy back 74LS244 to IC A4/17.

4. Connect pins 4,6,8,11,13,15,17 on the piggy back 74LS244 to pin 10 of the piggy back 74LS244.

DEPT	SIGNATURE	DATE	COMMENTS
Project Manager			
Customer Service			

Introduction

The CPU Control Card provides several support functions required by the CPU card. These include startup and bootstrap ROM, 4 serial communication ports, interrupt prioritisation, dynamic RAM refresh, day/date/time of day clock, P1 DMA daisy chain, and a parallel port.

Address Map

The Debug Card occupies the last 4K bytes of the 65K byte memory addressing space and is set up as follows:-

ADDRESS (HEX)	FUNCTION
F000-F7FF	Rom0 common rom
F800-FBFF	Rom1 processor unique
FC00-FCEF	Available for peripherals
FC80-FC8F	ACIA registers
FC90-FC97	Timer (6840)
FCF0-FCFF	PIA registers, user and clock
FCFC	CPU#1 interrupt prioritiser
FCFD	CPU#2 interrupt prioritiser
FD00-FEFF	Shared 512 byte RAM
FF00-FFFF	Unique 256 byte RAM for each processor

Restart and Interrupt Vectors

RAM space allocated uniquely to each processor provides independent restart and interrupt vectoring. The vector locations are as follows:

ADDRESS (HEX)	VECTOR
FFFE/F	Restart
FFFC/D	NMI
FFFA/B	SWI1
FFF8/9	Unused
FFF6/7	FIRQ
FFF4/5	SWI2
FFF2/3	SWI3
FFF0/1	Unused
FFEE/F (lowest)	IRQ level 7
FFEC/D	IRQ level 6
FFEA/B	IRQ level 5
FFE8/9	IRQ level 4
FFE6/7	IRQ level 3
FFE4/5	IRQ level 2
FFE2/3	IRQ level 1
FFE0/1 (highest)	IRQ level 0 (highest)

Debug Monitor

The Q133 contains two 2K ROMs that contain all the basic driver and initialization routines, such as loading the Disc drivers and Q256's maprams.

The monitor ROM occupies 1K bytes from F000 to F3FF and may be accessed by either processor. Processor-unique workspace RAM is used by the monitor so both processors can be executing the monitor independently.

Commands	
/	Reopen last open address as a 1-byte unit
AAAA	Open 2-byte unit at address AAAA
	Reopen last open address as a 2-byte unit
$A	Open CPU accumulator A
$B	Open CPU accumulator B
$X	Open CPU index register X
$P	Open CPU program counter
$H	Open user SWI handler address
$C	Open CPU Condition Code register
$D	Open CPU D register (A,B concatenated)
$Y	Open CPU index register Y
$U	Open CPU User Stack pointer U
$S	Open CPU Stack pointer S
$R	Open program segment Relocation Register
$G	Open CPU direct page register
$F	Open monitor flag byte
<return>	Close the open location
<linefeed>	Close current, open next location
^	Close current, open previous location
>	Close current, take branch offset and open
@	Open location pointed by current location
AAAA;B	Insert a breakpoint at address AAAA
;L	List all active breakpoints
AAAA;D	Delete breakpoint at address AAAA
;C	Clear all breakpoints
AAAA;T	Insert tracepoint at location AAAA (non-stopping breakpoint)
AAAA;K	Kill tracepoint or breakpoint at AAAA
AAAA;G	Start a user program at address AAAA
;P	Proceed from breakpoint, abort, or call
AAAA;O	Calculate branch offset from open location to address AAAA
HH;F	Fill memory from beginning address to end address
BEG ADDR	User prompt for beginning address
END ADDR	User prompt for end address
<CTRL X>	Abort current command line, take no action
<	Close current location, return to sequence start and open
AAAA,R	Relocate address AAAA by register R. R may be any of the CPU registers, the user relocation register, the monitor flag byte or the currently open location
AAAA.	Relocate address AAAA by Relocation Register $R
:	Same as linefeed (CTRL J) except that no new line is taken, and neither the address nor contents of the next location is displayed
AAAA#LL	Memory dump of LL lines (16 bytes/line) starting from, address AAAA
'<ASCII chr>	Input ASCII character value instead of hex value for any of the above commands

The 6809 monitor will also accept input of signed hex numbers.

System Boot/Disk ROM

This ROM is used by CPU#2 for disk booting operations and occupies locations F800 to FBFF in the unique ROM space for CPU#2.

The following functions calls are provided:-

* Boot load QDOS operating system from disk
* Initialise disk controller
* Read full last sector
* Read partial last sector
* Read verify (CRC check only)
* Write and verify CRC
* Restore head (seek track 0)
* Seek to specified track
* Write test
* Write D.D. mark to sector
* Write sectors and verify CRC
* Write sectors and don't verify CRC
* Check and abort if non-recoverable error

This ROM contains the code to load the actual disk drivers into system RAM. The driver routines themselves are stored in RAM after being loaded from the ROM on the QFC9 floppy controller card, the Q077/Q087 Hard Disk card if present and the Q777 SCSI Controller card.

Address Decoding

(refer schematic Q133-00)

The System Address Buss is buffered by non-inverting buffers A1 and A4. NAND gate B1 generates an output (asserted LOW) when an address in the range FXXX is detected. This is fed out to the buss on edge connector pin 60B. Further decoding by combinational logic at B4, D4, B3, C2 and C1 generate select signals for the two EPROMS, $\overline{\text{ROM0}}$, $\overline{\text{ROM1}}$.

Selection of the on-card static RAM and peripheral devices in the FCFX range are also decoded.

These six select signals are latched by hex flip-flop B6. Hex flip-flops C7 and D7 latch the 11 low-order address bits, as well as the READ/WRITE signal. When any of the on-board devices are read from, inverting data buss transceiver A5 drives the buss. (See drawing Q133-03). At other times, A5 buffers the data into the card.

RAM Refresh Control

Rate multiplier C10 is configured to produce a 1 microsecond pulse every 16 microseconds. This output generates a DMA request for Processor 1 ($\overline{\text{RDMA}}$), via DMA hardware at C8, B10 ,B5 and C4. The refresh has the highest priority in the P1 DMA daisy chain.

The $\overline{\text{ENL}}$ signal, (Enable Next Level), indicates to the next device along the daisy chain when it may make DMA requests. It normally goes low every second P1 cycle, but if a refresh request is pending, the low pulse is inhibited.

When this request is acknowledged by the ACK1 buss signal from the Q209 CPU (asserted HIGH) flip-flop B10 generates a /REF (Refresh, asserted LOW) signal on the buss, which signals a refresh cycle to the dynamic RAMs in the system. At the same time, the output of the refresh address counter A2 is driven onto the buss by tri-state buffers A3. At the completion of the refresh (DMA) cycle, the refresh address counter is incremented ready for the next cycle.

Static RAM

(refer schematic Q133-01)

A small amount of static RAM is provided for use as scratchpad during disk calls and monitor firmware execution. It is organised as follows:

CPU #1 FF00-FFFD
CPU #2 FF00-FFFD
Both FD00-FEFF

The addressing function for this purpose is generated by multiplexer C9 which is driven by an OR funtion of address bits 8 and 9. The RAM itself is in the form of two 1K X 4 devices at D8 and D9.

EPROM

Four kilobytes of U.V. erasable ROM are used. These are 2716s/2516 single 5 volt supply type.

Their functions are:

Location	Address Range	CPU #	Function
D2	F800-FBFF	1	Startup
D4	F800-FBFF	2	Disk boot
D5	F400-F7FF	Both	I/O functions
D6	F000-F3FF	Both	Debug monitor

ACIAS (Asynchronous Communications Interface Adapter)

(refer schematic Q133-02)

6551 ACIAs atE4, E5, E1, E2, E3 are used to receive and transmit serial data. The BAUD rate is determined internally via internal dividers, from the baud-rate generator master 1.8432MHz oscilator at D1.

Interrupts generated by the ACIAs go to the system buss via pin 68B of the edge connector.

Data input and output level conversion for the RS232 standard is provided by circuitry on Sheet 3.

The 6551 used for keyboard data is at location E2, 3. The ACIAs at E4 and E5 have optional RS422 tranceivers at F7 and F8 as well as RS232, at F6 and F5. The 555 timer at D10 is used in the RS422 buss timeout control.

PIA (Peripheral Interface Adapters)

(refer schematic Q133-01)

PIA (F10,11,12) is used to provide two general purpose parallel ports. Peripheral connections are made through a 26-way ribbon cable connector on the front of the card.

Interrupts from the PIA are presented to the buss via pins 66B and 67B.

PIA (E9,10,11) is used to interface the clock/calender chip at E12. This clock has a 3.7 volt Lithium cell to maintain the time when the computer is turned off. The battery is not rechargeable and must be replaced when flat. Battery life is approximately 3 years.

Diodes CR5 and CR4 isolate the battery from the 5 volt supply, so that the battery is only connected to the clock when the 5 volt supply drops. Transistors Q2, Q1 on drawing Q133-03, and associated components interface the PIA's signal levels to the clock and control the power-down function of the clock so that no false writes occur at power-on and off. An optically isolated power down signal is available at connector pins 61B and 62B, from the opto-isolator at A11.

Manual Controls

Restart, halt and interrupt controls are provided on the front-panel card Q137. The sole use is for system debugging. In normal use all signals from the Q137 are inactive.

Activating either HALT switch on the front panel sends /HLT1 or /HLT2 to the corresponding processor on the Q209 CPU. When halted, the Buss Available signals from the CPU card W1 and W2 drive open-collector buffers B12 to turn on the WAIT LEDs on the card.

The system can run without a front panel being connected.

Power-on Reset

555 Timer A12 is used to generate a system-reset signal on power-up or manual restart from the front panel console, if restart is enabled on both processors. This is a low-going pulse of about 500 milliseconds on buss pin 42.

Interrupt Priority Logic

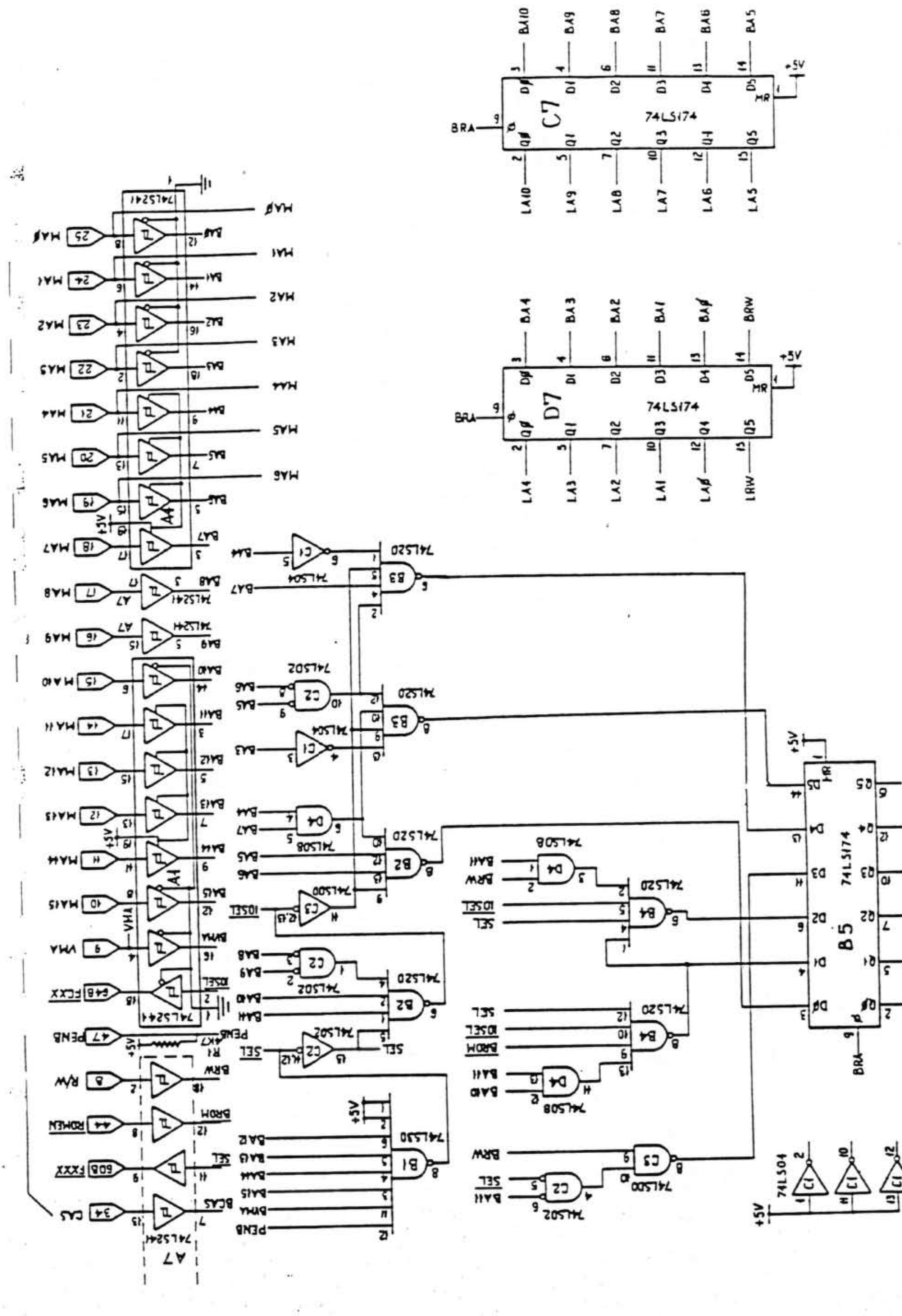
8214 Priority Interrupt Control Units (PICU) are used to latch interrupt requests and generate a priority level which is used by the CPU card to create an interrupt vector address. Each processor has its own PICU.

The priority level for each PICU is established by writing the complement of the desired priority level into the status register. The address for CPU 1 is FCFD, for CPU 2 it is FCFC. Decoding for this purpose is performed by one-of-eight selector B8.

Interrupt requests generated by the PICU are latched by flip-flops B9, which are reset when the PICUs are written to to establish the new priority level mask.

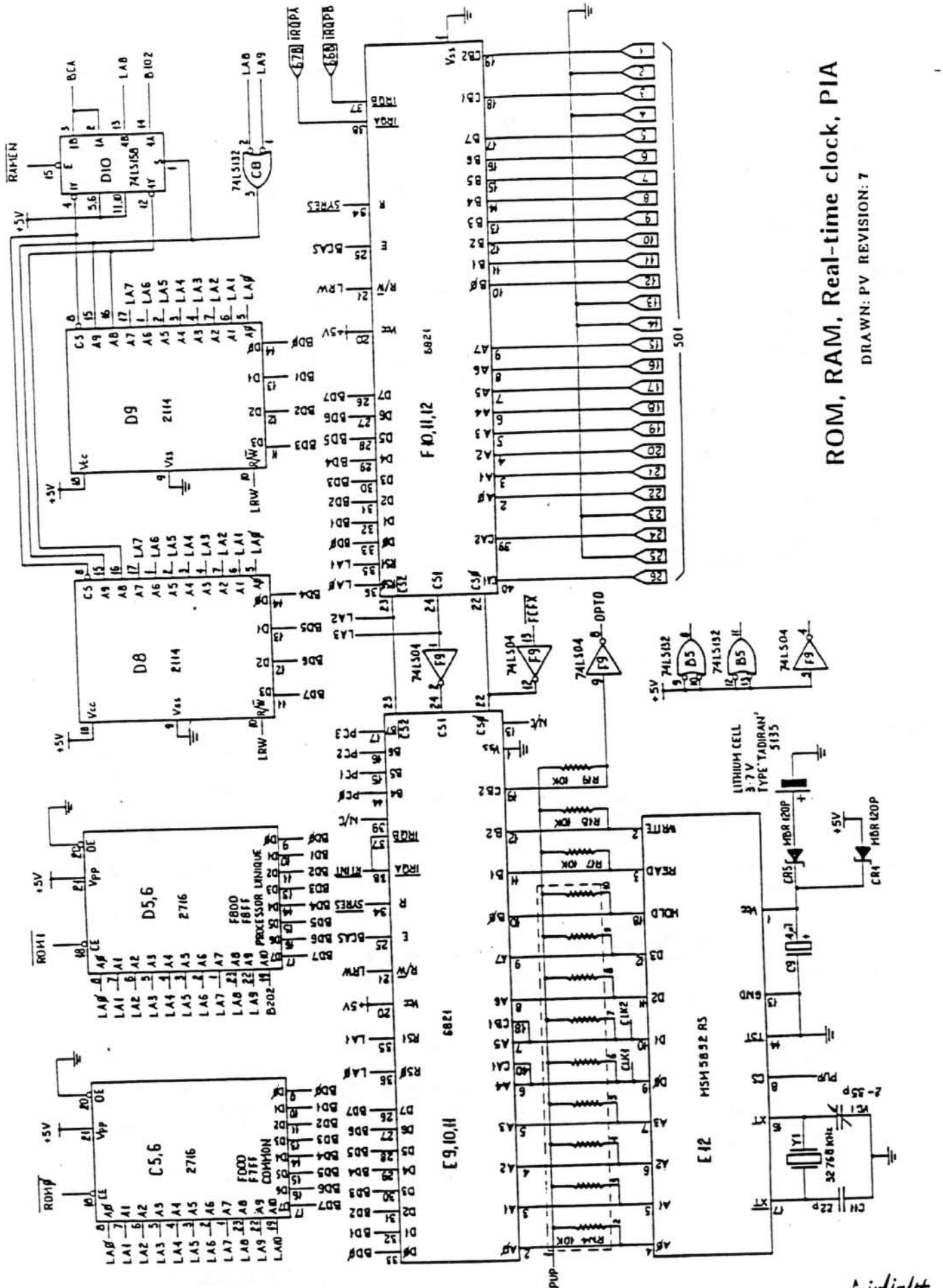
The PICUs are clocked by Interrupt Latch Strobe signals from the bus (ILS1 and ILS2).

Each PICU supports up to eight levels of interrupt.



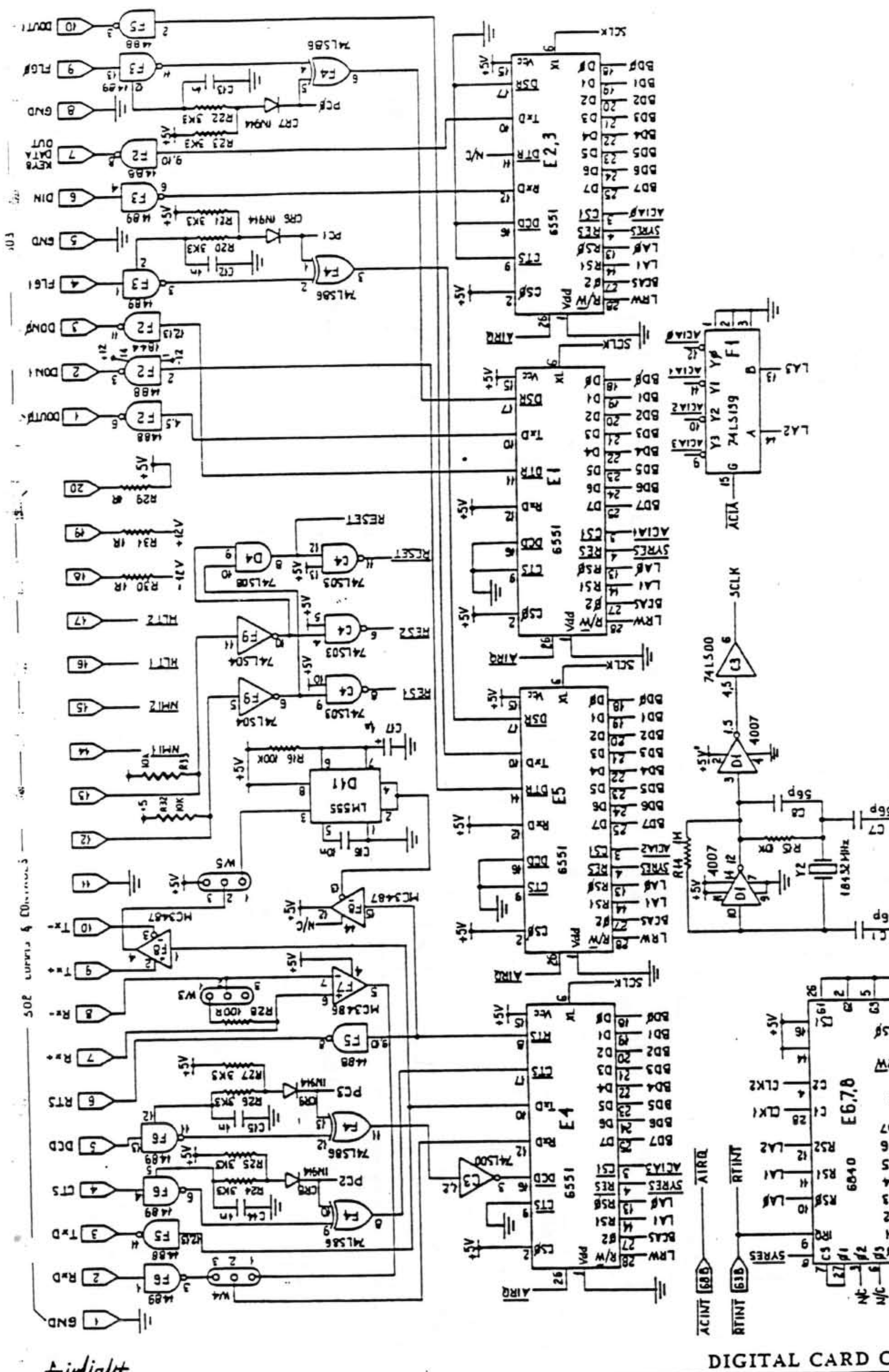
Address Decoding

DRAWN: PV REVISION: 7

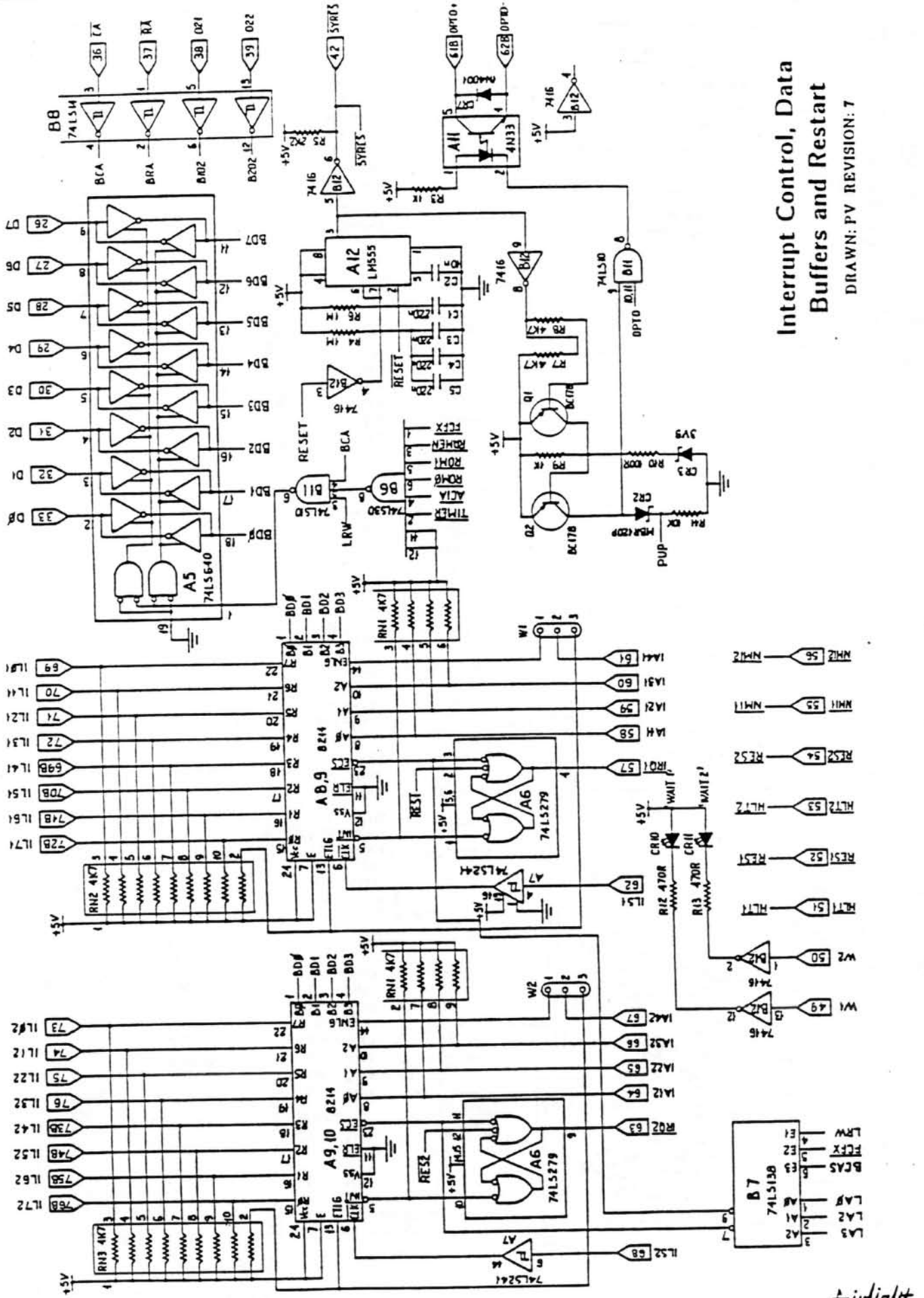

ROM, RAM, Real-time clock, PIA
DRAWN: PV REVISION: 7
D9
D8
D5,6
C5,6
F10,11,12
E9,10,11
E12
501
LITHIUM CELL
3.7 V
TYPE 'TADIRAN'
5135
32768 KHz

Serial Interfaces, Timer

DRAWN: PV REVISION: 7



fairlight


Interrupt Control, Data
Buffers and Restart
DRAWN: PV REVISION: 7

Memory Refresh

DRAWN: PV REVISION: 7