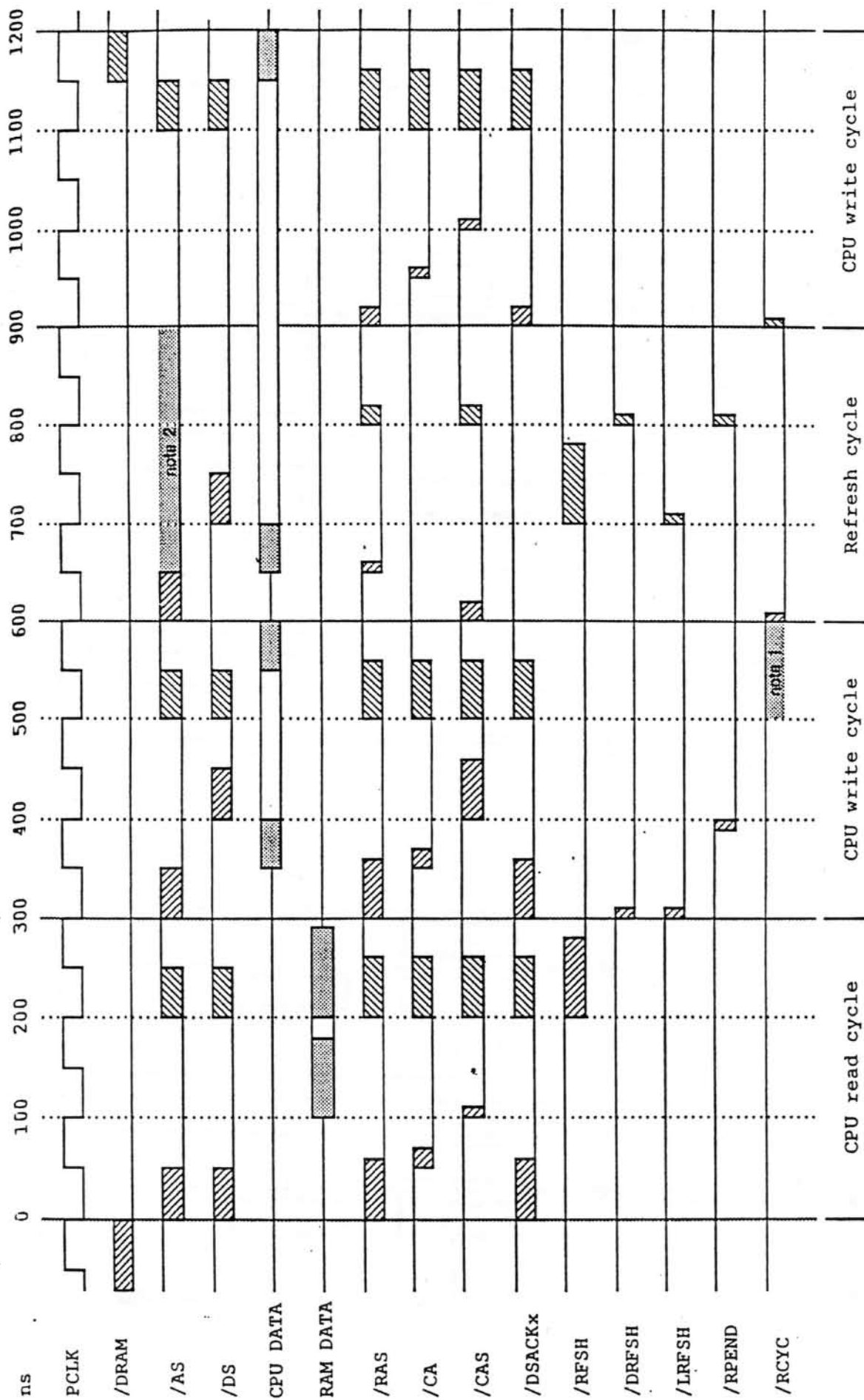


Figure 3 - CMI-41 Dynamic RAM Timing (DRPAL)



- Notes:
1. Refresh cycle delayed by current CPU cycle.
 2. CPU cycle pre-empted by pending refresh cycle (up to 3 wait cycles inserted).
 3. This diagram assumes 12MHz 68020, 120ns DRAMs, 15ns PAL.

Figure 4 - 68450 DMA Controller - bus interchange network (F8-F10)

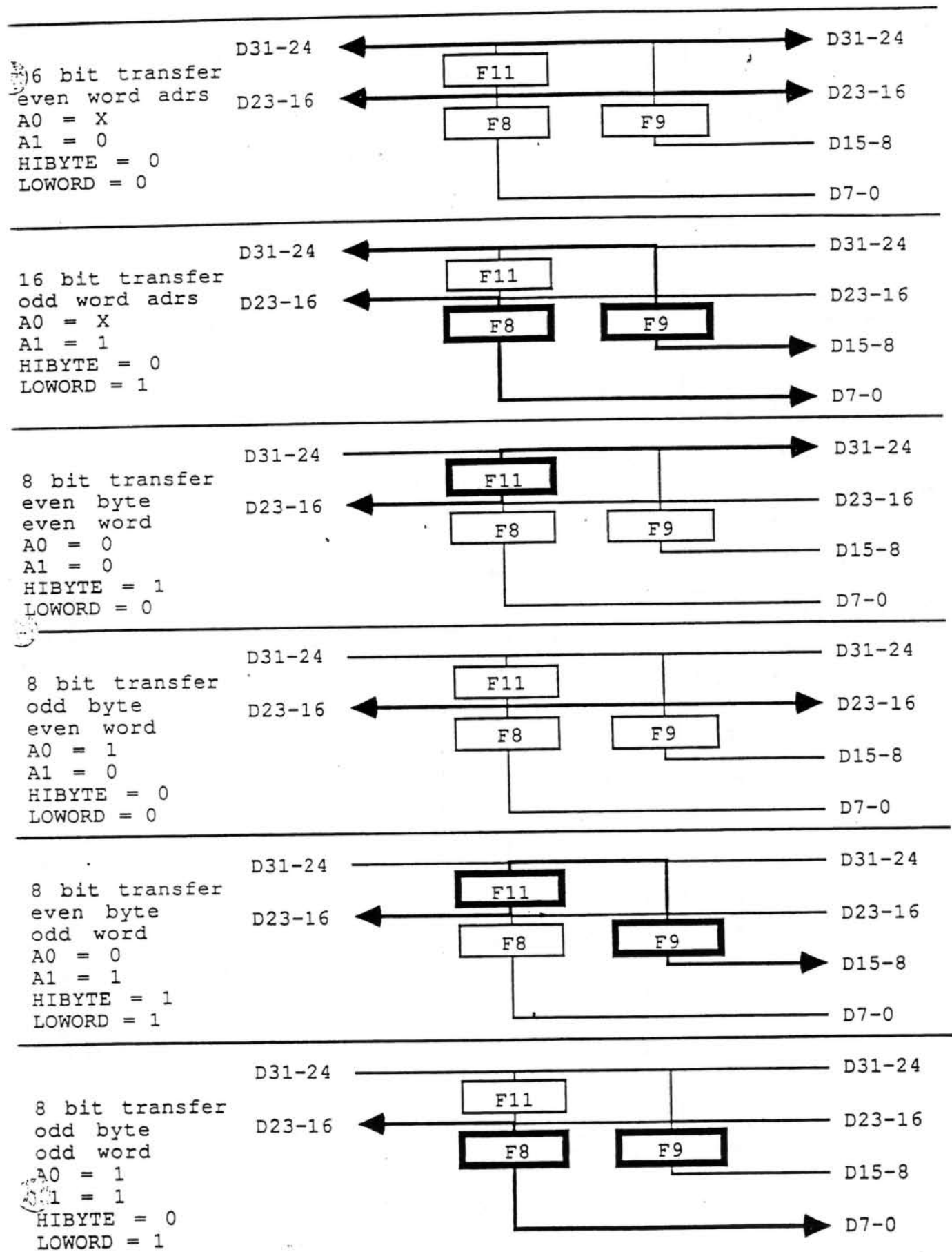


Figure 8 - CMI-41 Sample Card Interface - Serial Link Timing

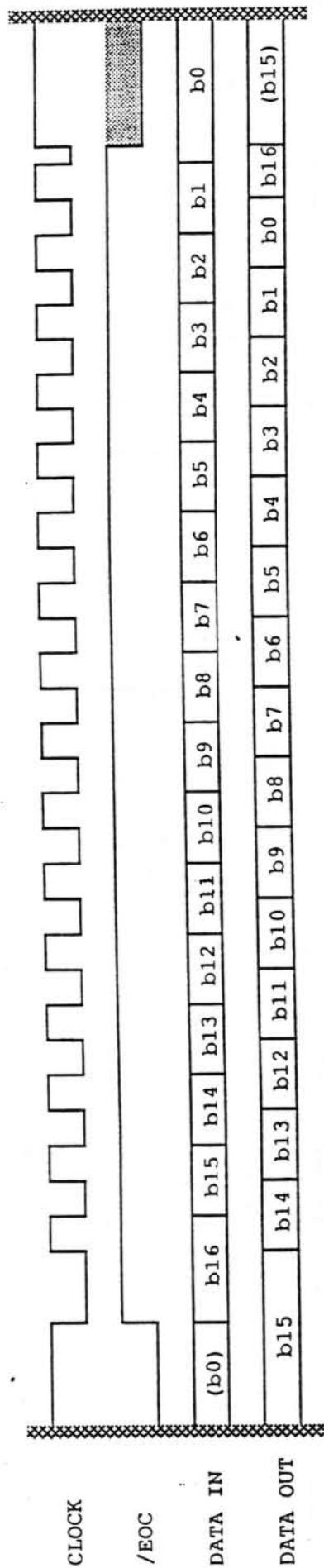
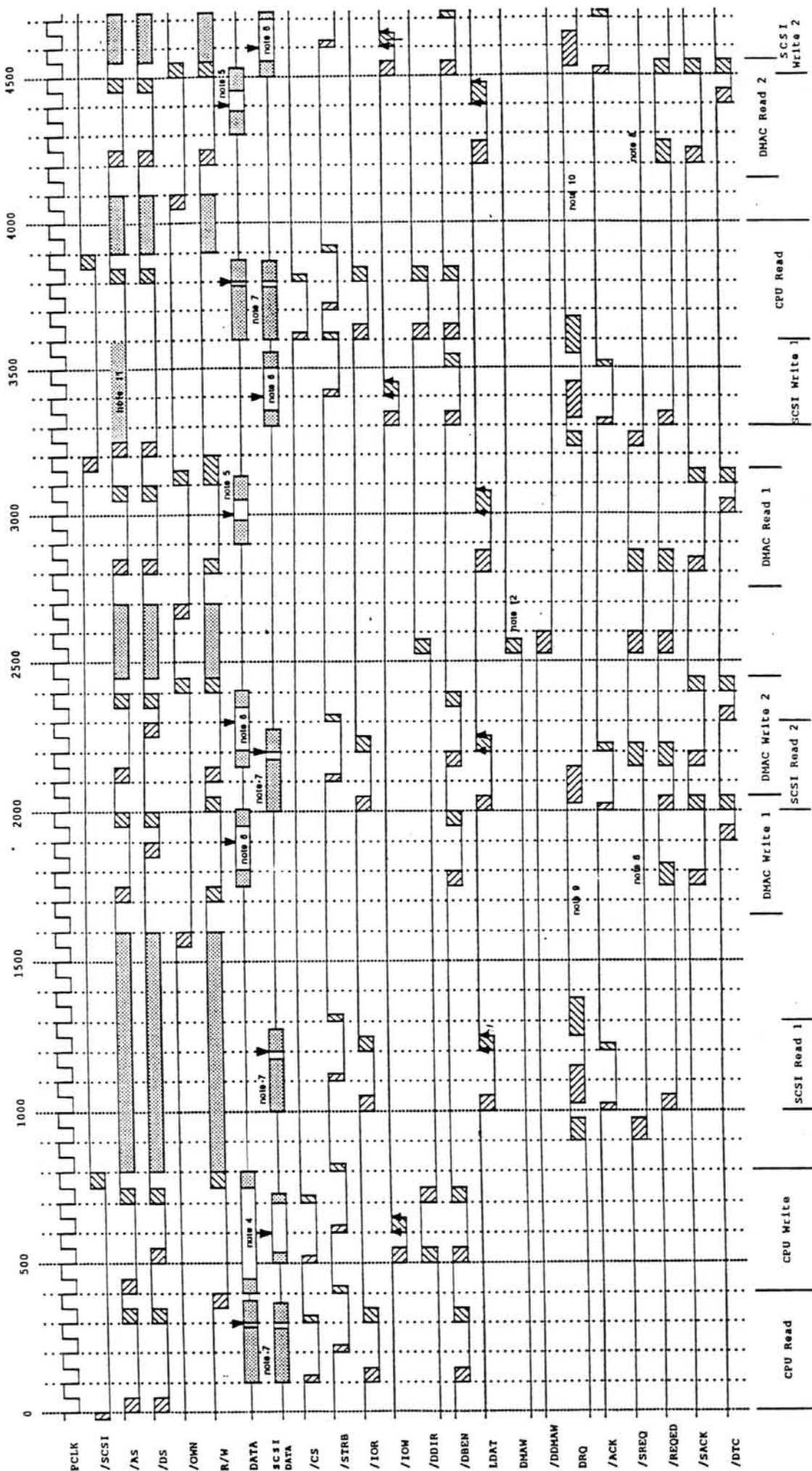
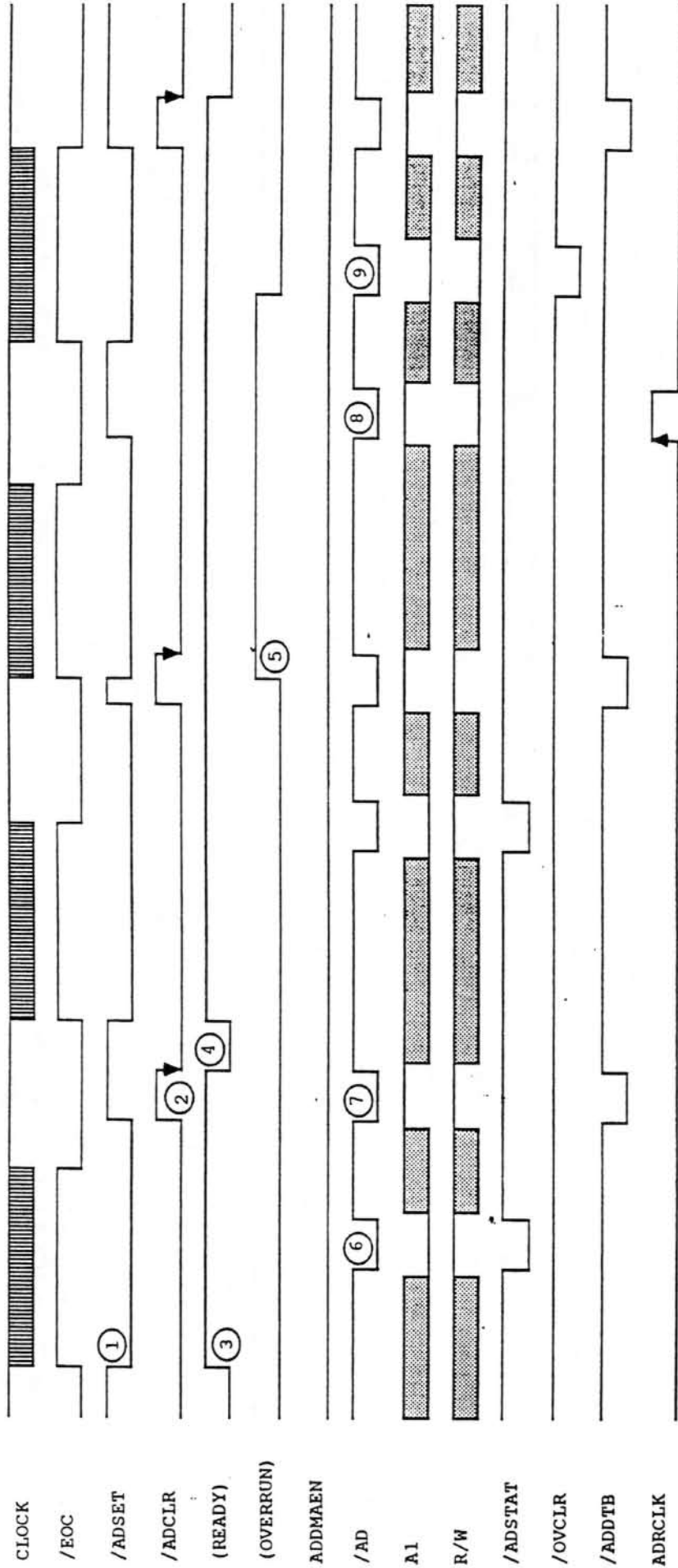


Figure 5 - CMI-41 SCSI Interface Timing - CPU and DMA access



- Notes:
1. This diagram assumes 12MHz CPU, 10MHz DMAC, 25nS PALS.
 2. Nominal data latch points indicated by arrow: ▼
 3. DMAC accesses shown are single address to/from DRAM.
 4. Data from CPU.
 5. Data from DRAM.
 6. Data from 74ACT646 buffer.
 7. Data from NCR5380 SCSI controller.
 8. /SREQ not negated due to pending DRQ.
 9. DRQ pending next DMA write cycle (buffer full).
 10. DRQ pending next DMA read cycle (buffer empty).
 11. CPU cycle pre-empted by SCSI (DRQ) cycle.
 12. SCDMAW control line asserted by CPU.

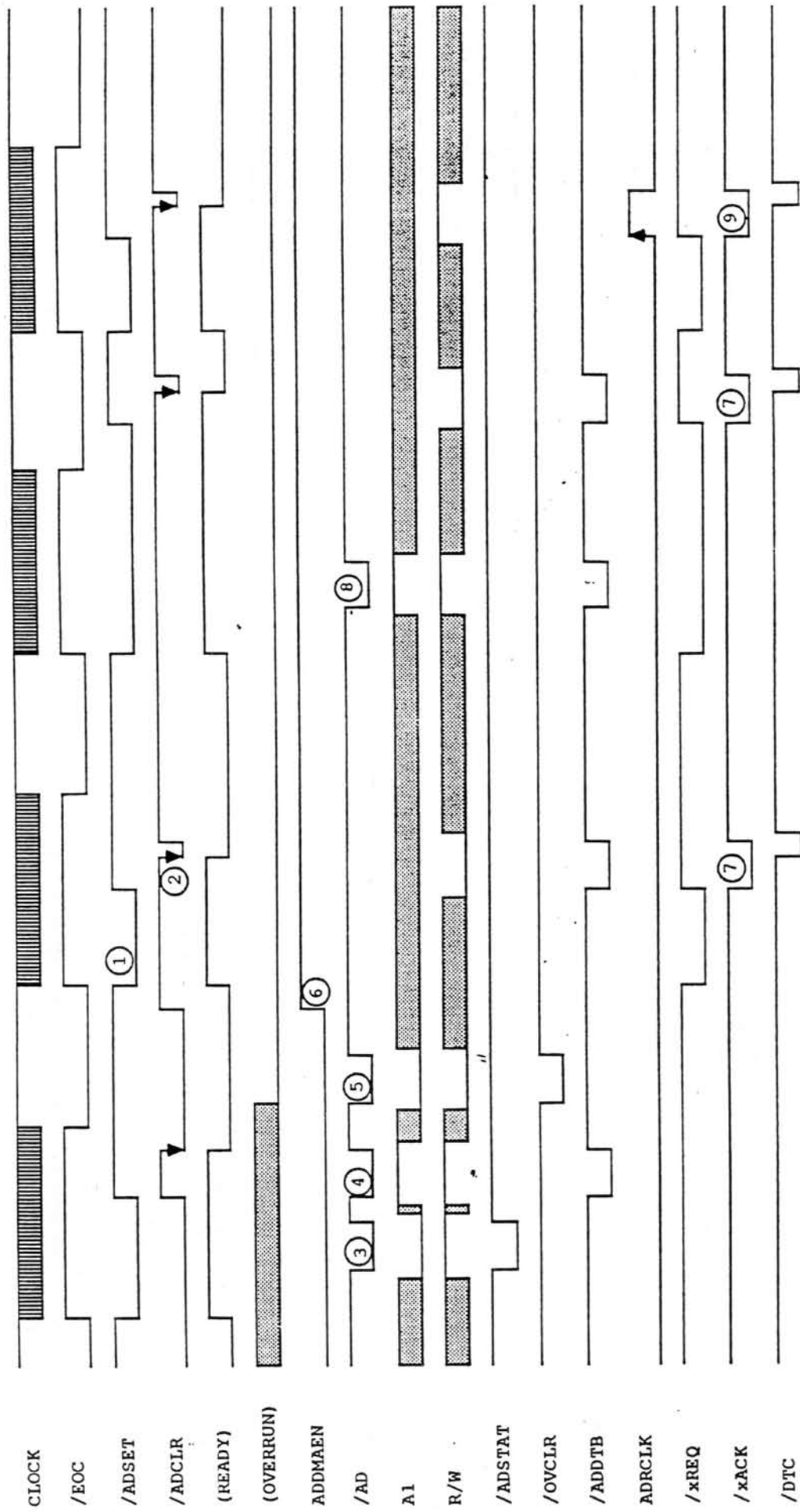
Figure 9 - CMI-41 Sample Card Interface - CPU Access



Notes:

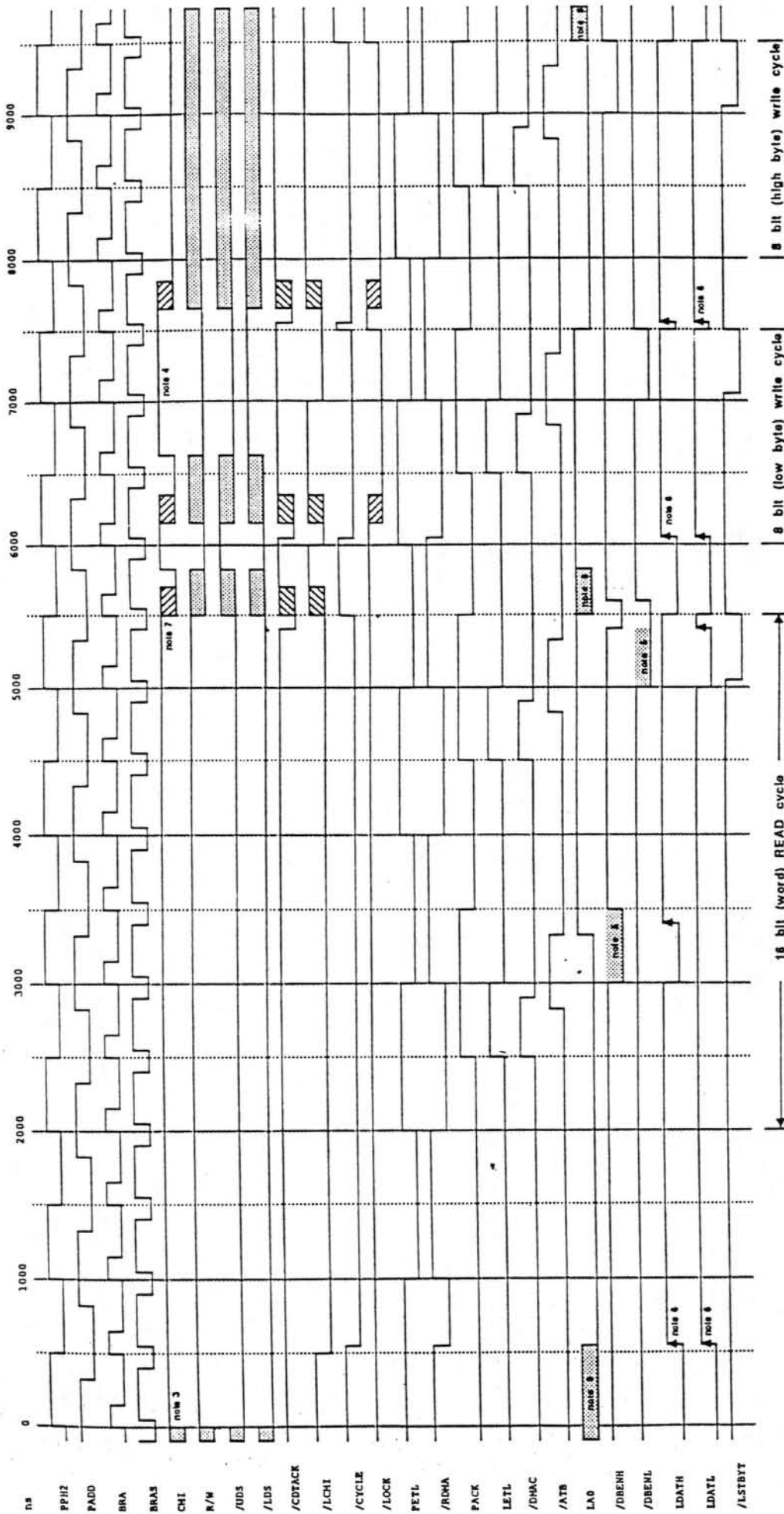
1. /ADSET asserted by /EOC rising and cleared by CPU access to data register in non-DMA mode.
2. /ADCLR = CPU read from data register in non-DMA mode.
3. READY flag set by /ADSET.
4. READY flag cleared by /ADCLR falling.
5. OVERRUN flag set by /EOC rising when READY flag set.
6. CPU read from status register.
7. CPU read from data register (clears READY flag).
8. CPU write to return data register (READY flag not affected)
9. CPU write to clear OVERRUN flag.

Figure 10 - CMI-41 Sample Card Interface - DMA Access (Including Initialisation by CPU)

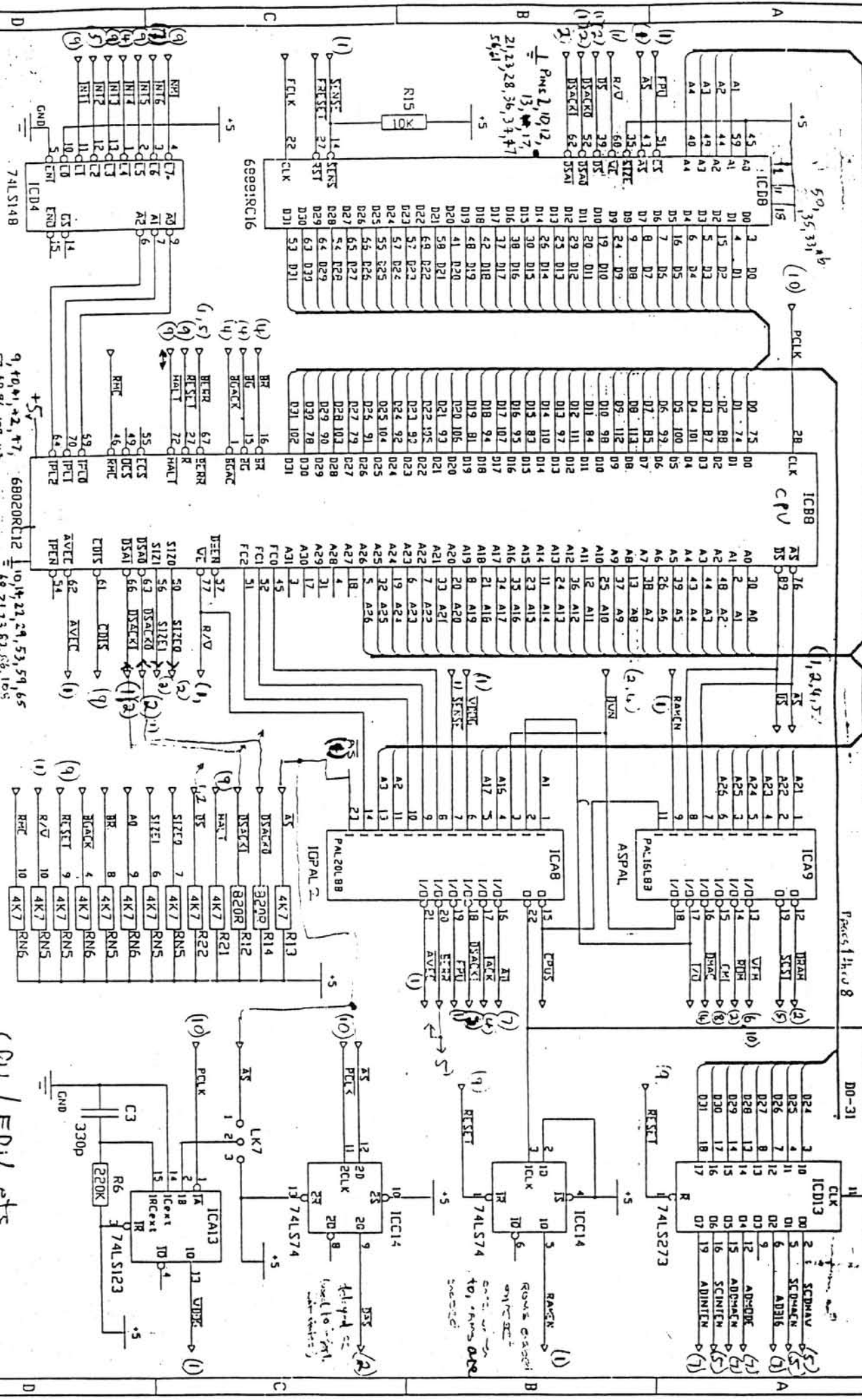


- Notes:
1. ADSET asserted by /EOC falling and negated by ACK in DMA mode.
 2. ADCLR = (ACK & DTC) in DMA mode.
 3. CPU read from status register.
 4. CPU read from data register to clear READY flag.
 5. CPU write to clear OVERRUN flag.
 6. CPU enables DMA mode.
 7. DMA transfer from data register to memory.
 8. CPU read from data register while in DMA mode does not affect DMA control signals.
 9. DMA transfer from memory to return data register.

Figure 11 - CMI-41 CMI BUS Interface Timing - 16 and 8 bit transfers, read and write



- Notes:
1. This diagram does not show gate delays. Signals are shown as if all devices have zero propagation delay.
 2. Effect of higher priority DMA devices not shown.
 3. READ request from CPU shown in maximum latency position.
 4. WRITE cycle delayed by previous concurrent write cycle.
 5. Redundant data buffer enable.
 6. Redundant latch strobe.
 7. Time for negation of CMI, CDTACK etc depends on phasing between CMI bus signals and 68020 clock (PCLK).
 8. When CYCLE is negated /LA0 follows A0 bus line.

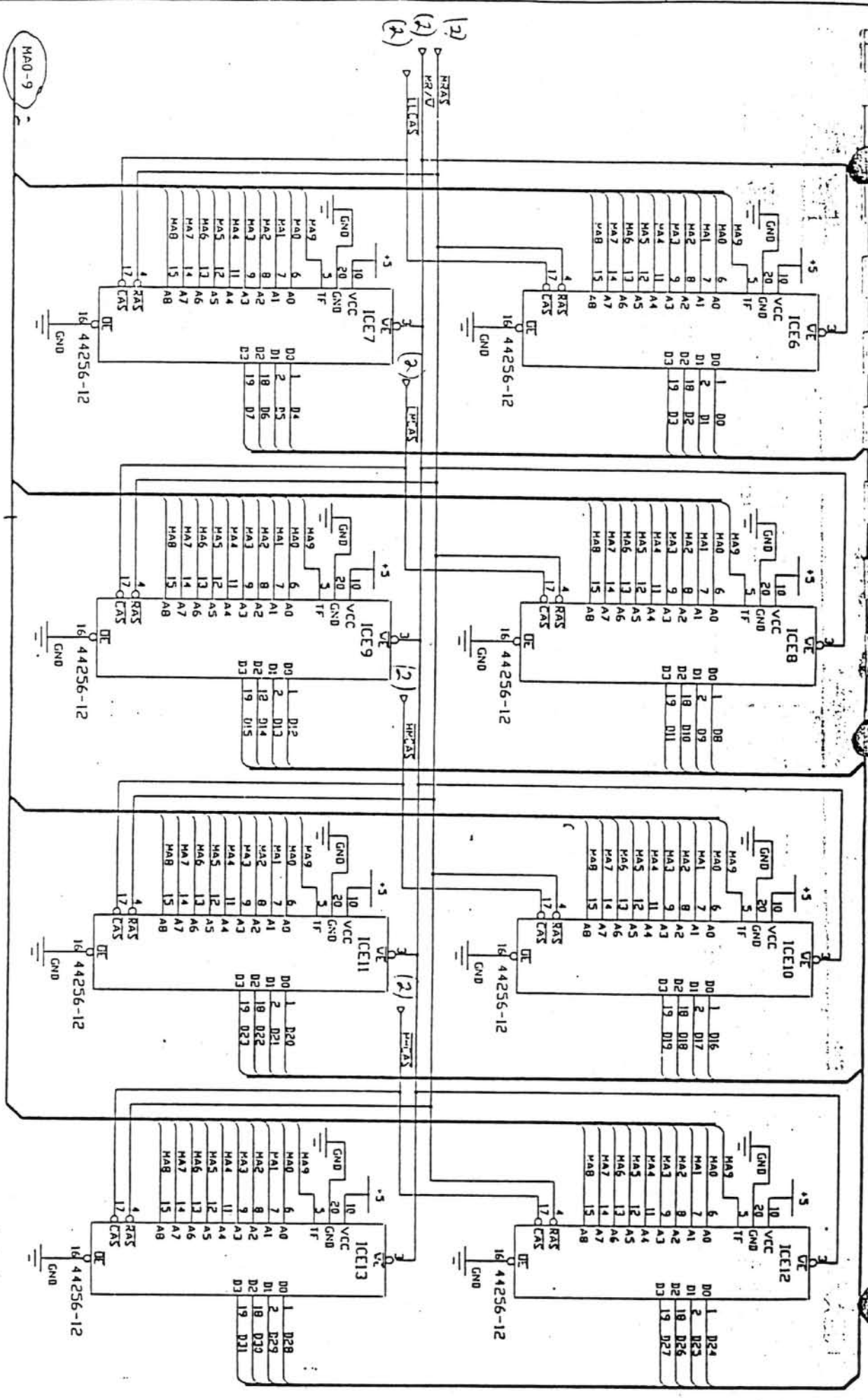


ZONE	DATE	DESIGN BY	TITLE	DESCRIPTION	ISSUE	DATE	APP'D	DRAWING-NO	SHEET-NO	ISSUE
	4th Nov 1987	AJ Cannon	WAVEFORM SUPERVISOR	CPU, PUL INTERRUPTS, ADDRESS DECODING, WATCHDOG, CONTROL LATCH				CMI-41 rev 1	1	DF 10

FAIRLIGHT INSTRUMENTS

CPU/FPV etc

9, 10, 11, 12, 17, 68020RCL12 = 10, 14, 22, 29, 53, 59, 65, 68, 69, 96, 109, 114, 68, 71, 73, 63, 69, 105



MA0-9

DRAM

DYNAMIC RAM ARRAY

DESCRIPTION

ISSUE

DATE

APP'D

FAIRLIGHT INSTRUMENTS

WAVEFORM SUPERVISOR

DRAWING-NO

CM1-41 rev 1

SHEET-NO

3 OF 10

ISSUE

DATE

5th Nov 1987

DESIGN BY

A-Cannon

ZONE

5th Nov 1987

1

DESCRIPTION

WAVEFORM SUPERVISOR

2

ISSUE

3

DATE

3

APP'D

3

FAIRLIGHT INSTRUMENTS

DRAWING-NO

CM1-41 rev 1

4

SHEET-NO

3 OF 10

4

ISSUE

1

5

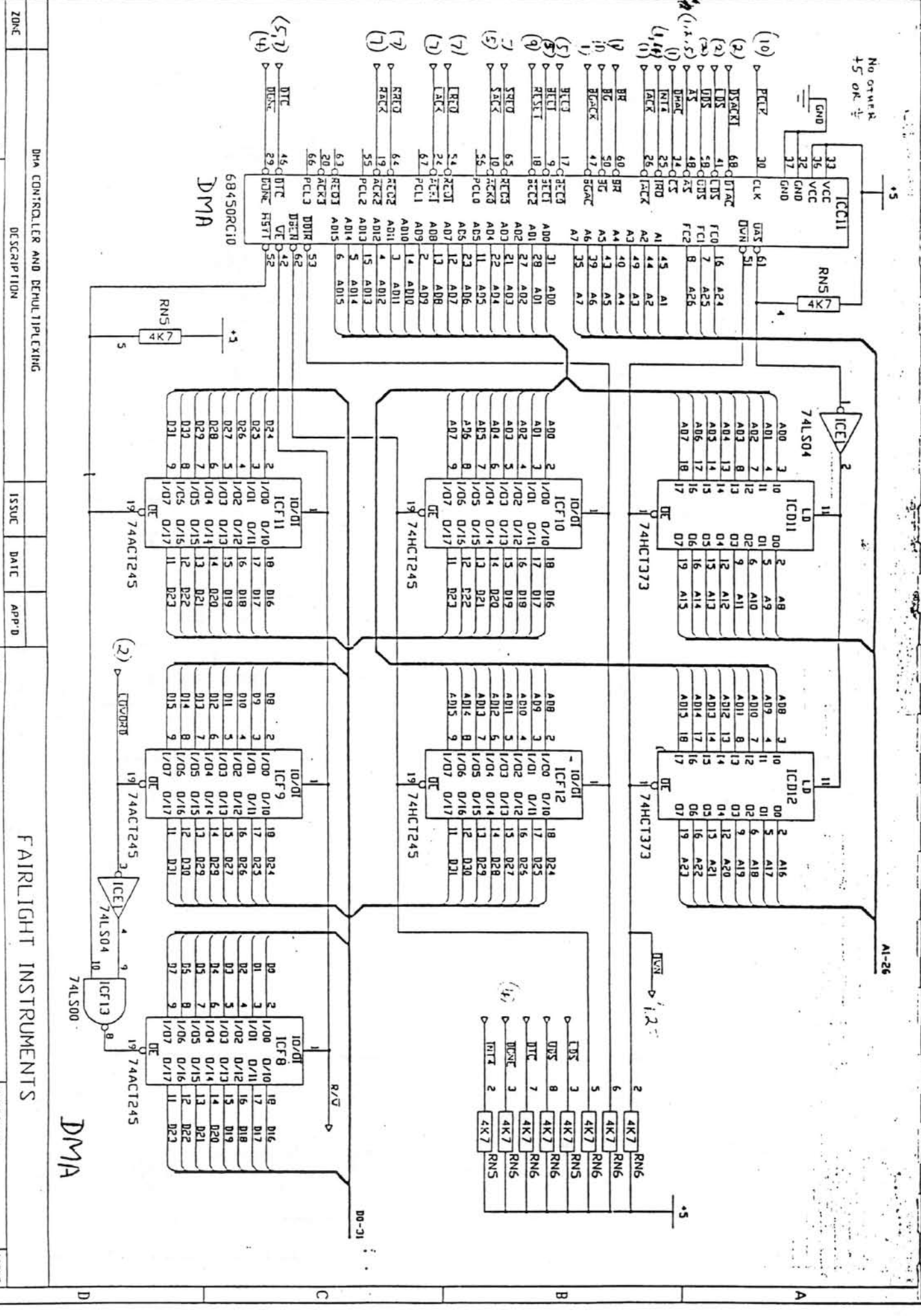
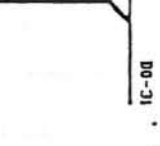
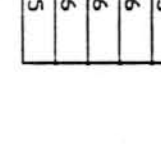
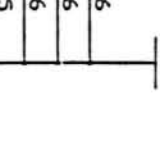
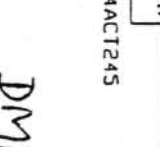
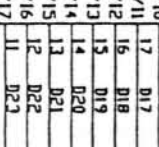
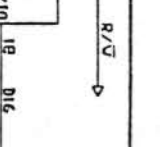
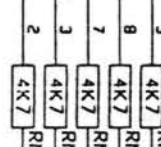
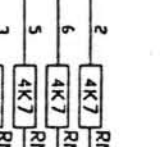
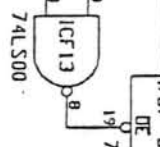
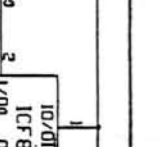
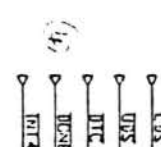
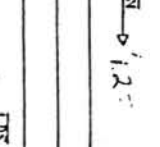
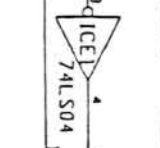
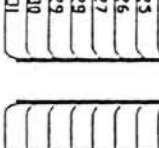
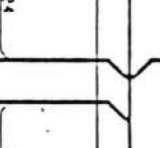
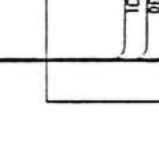
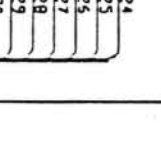
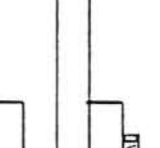
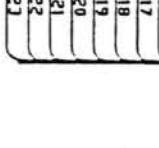
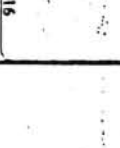
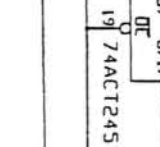
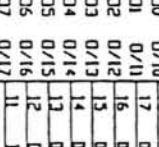
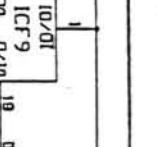
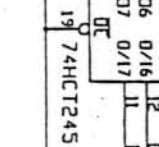
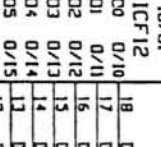
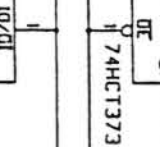
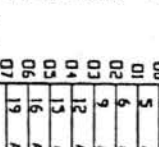
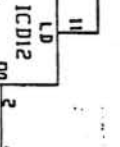
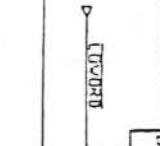
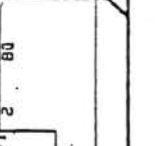
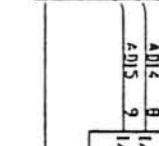
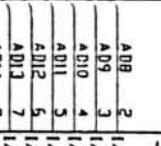
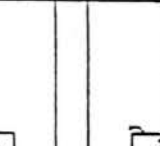
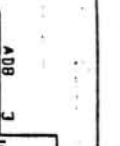
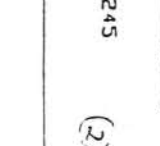
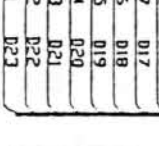
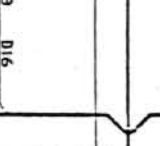
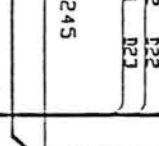
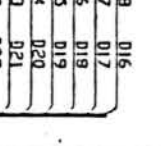
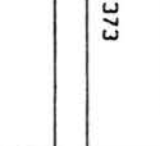
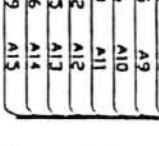
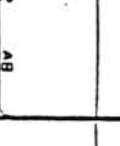
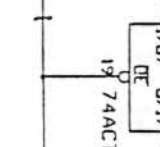
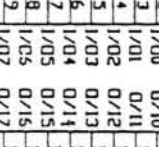
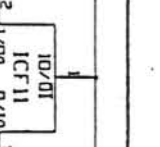
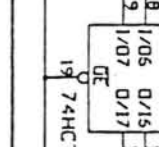
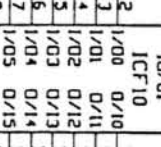
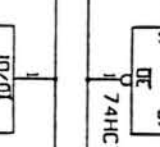
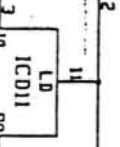
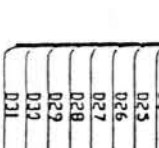
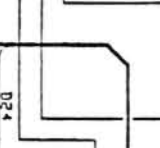
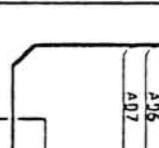
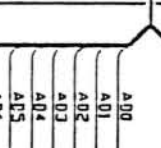
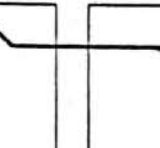
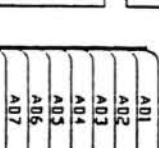
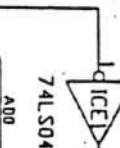
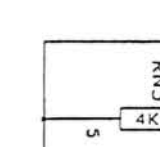
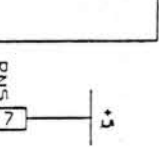
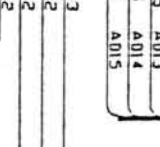
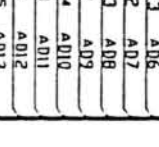
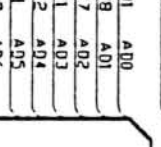
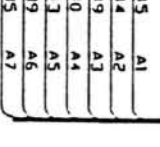
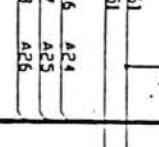
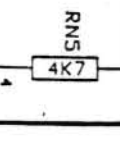
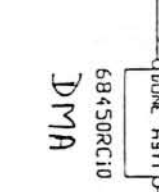
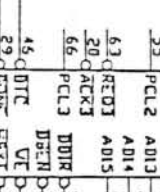
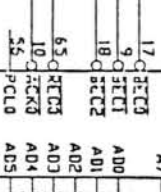
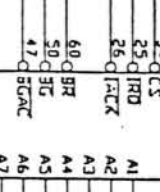
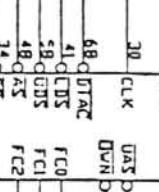
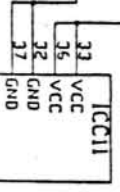
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C

B

A

No OTHER
+5 OR ±



6845ORC10

DMA

DMA

DMA CONTROLLER AND DEMULTIPLEXING

DESCRIPTION

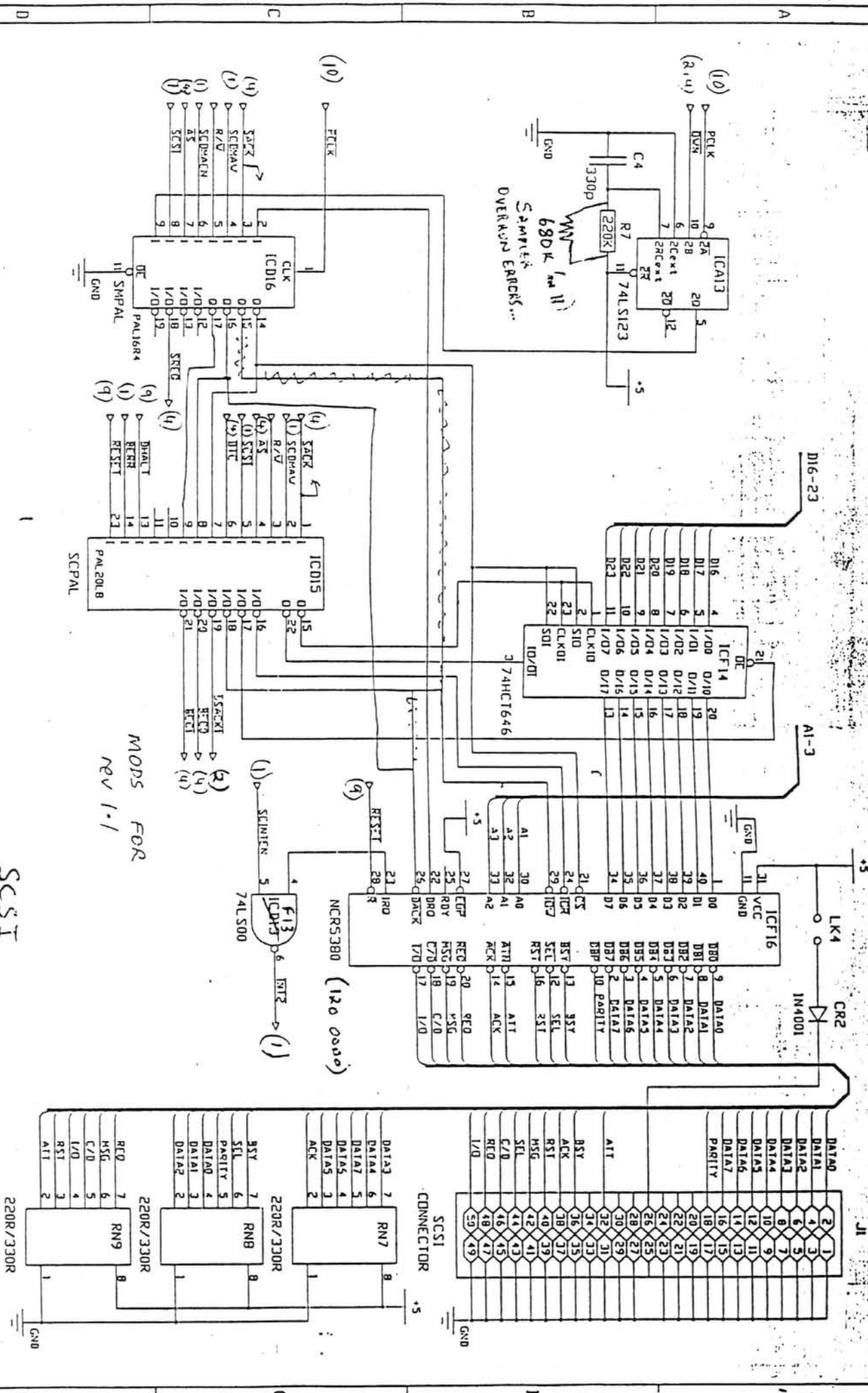
ISSUE

DATE

APP'D

FAIRLIGHT INSTRUMENTS

DM-31



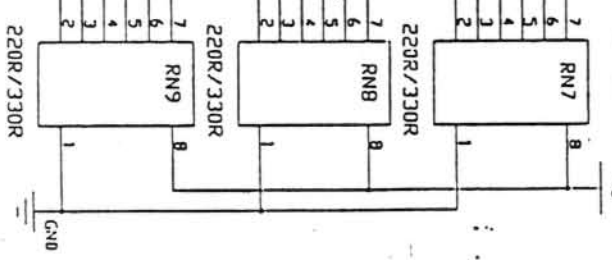
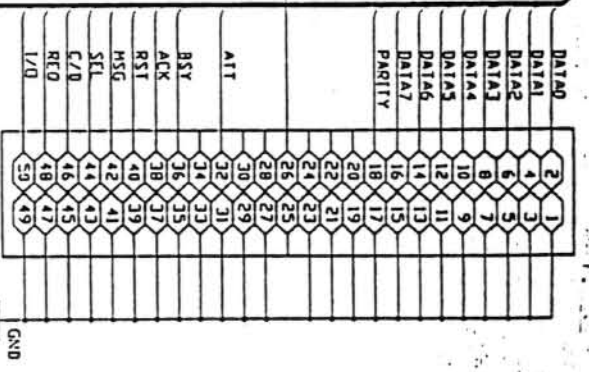
ZONC		SCSI INTERFACE		ISSUE		DATE		APP'D		DRAWING NO	
5th Nov 1987		DESCRIPTION		DATE		DATE		DATE		CM1-41 rev 1	
DESIGN BY A.Cannon		TITLE		DATE		DATE		DATE		SHEET NO	
		WAVEFORM SUPERVISOR		DATE		DATE		DATE		5 OF 10	
				DATE		DATE		DATE		ISSUE	
				DATE		DATE		DATE		1	

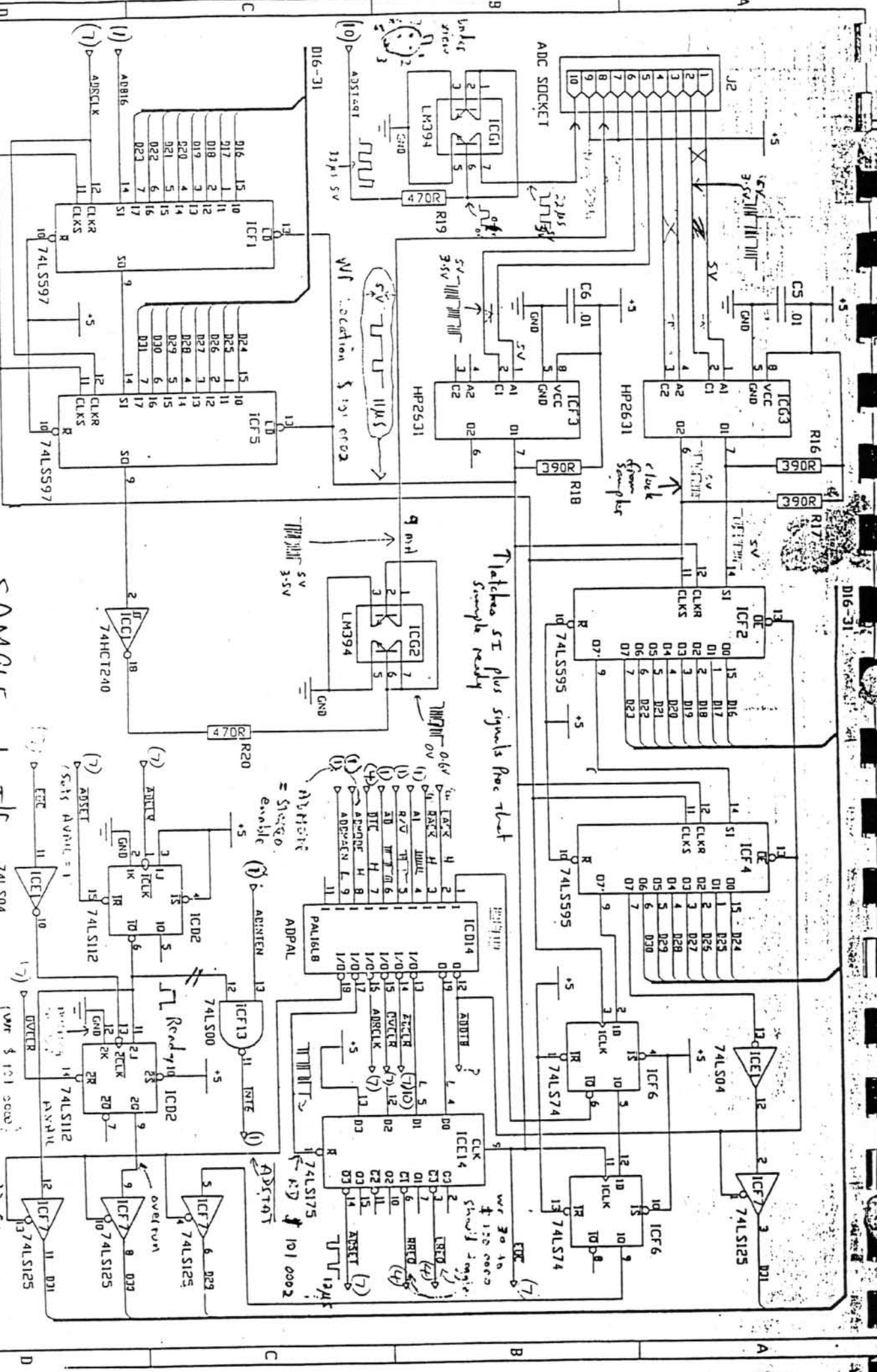
FAIRLIGHT INSTRUMENTS

SCSI

MODS FOR
rev 1-1

SCSI
CONNECTOR

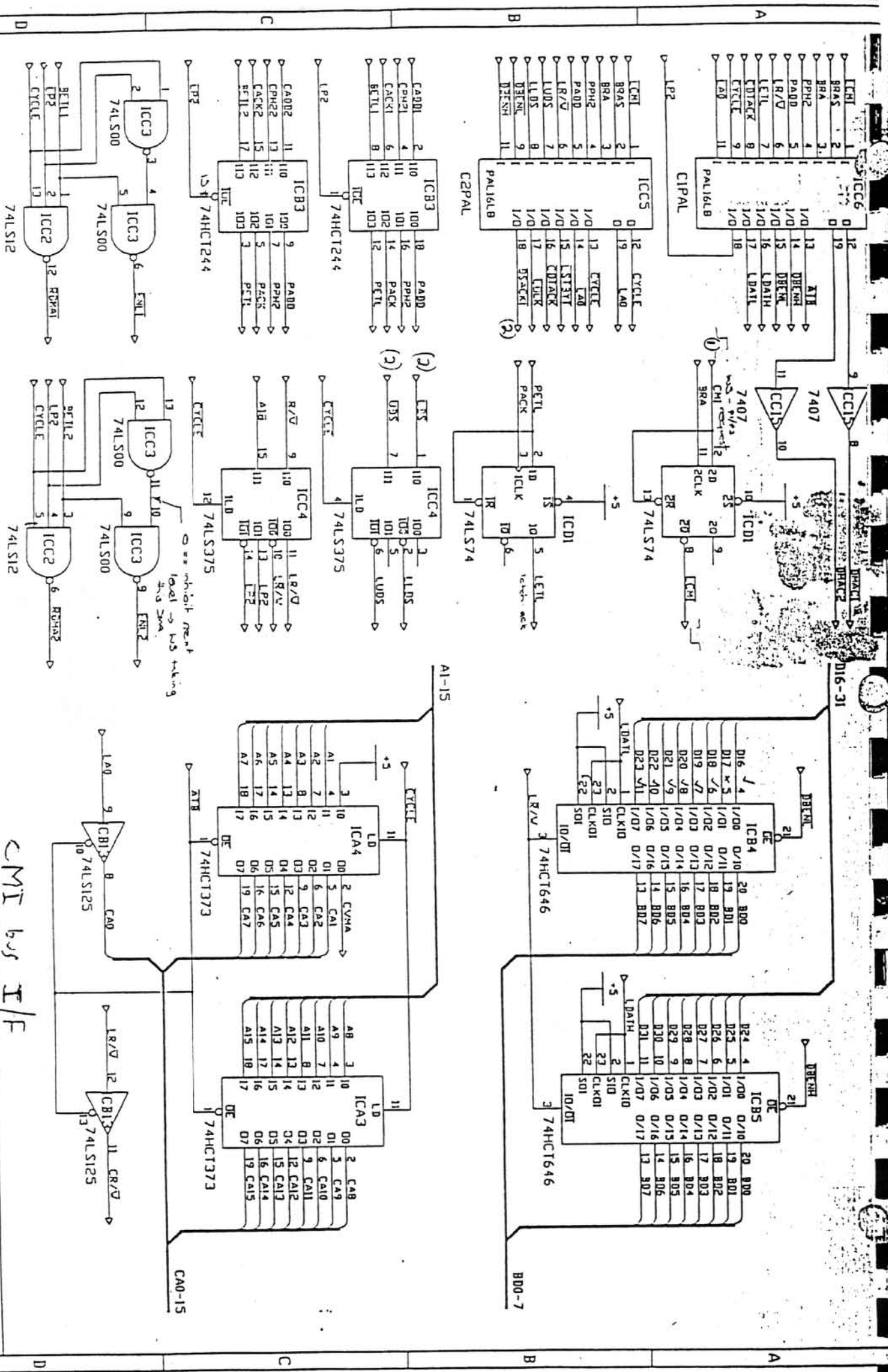




SAMPLE card I/F

FAIRLIGHT INSTRUMENTS

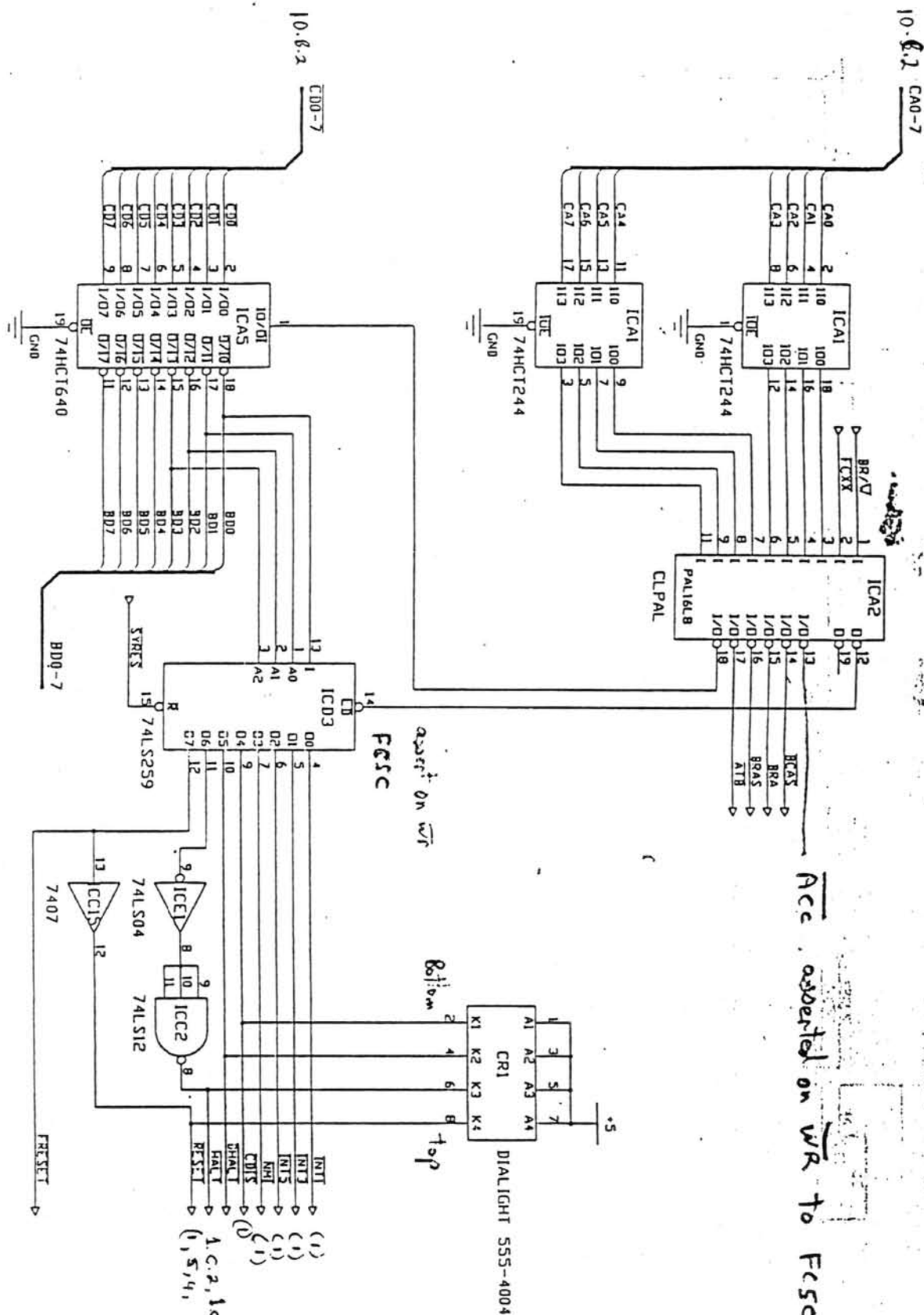
ZONE	DESCRIPTION	ISSUE	DATE	APP'D
	SAMPLE CARD INTERFACE			



DATE	6th Nov 1987	TITLE	WAVEFORM SUPERVISOR
ZONE		DESCRIPTION	
ISSUE		DATE	
APP'D			
DRAWING-NO	CMI-41 rev 1	SHEET-NO	8 OF 10
		ISSUE	1

CMI bus I/F

FAIRLIGHT INSTRUMENTS



Acc asserted on WR to FC5C

Bottom top

FC5C

External control latch

CONTROL LATCH LEADS		ISSUE	DATE	APP'D	DRAWING-NO	SHEET-NO	ISSUE
DESCRIPTION							
ZONE	6th Nov 1987	TITLE	VAVVEFD04 CIRCDVATCND				
DATE							

FAIRLIGHT INSTRUMENTS

