CMI-31

CHANNEL CARD

fairlight

FIELD CHANGE NOTICE

DATE 24/ 3 / 93
NUMBER 124

ORIGINATOR Chris Alfred **PRODUCT: CMI / MFX**

ASSEMBLY No. CMI-31 **DESCRIPTION** Channel card

This FCN applies to REV No: REV 2A4 **New REV No is:** REV 2A5

REASON FOR CHANGE:
Latch refresh to avoid noise corrupting channel card memory.

The noise usually causes channel card 8 to crash.

NOTE: If this FCN is carried out FCN 123 MUST be done to the Turbo SCSI card.

THIS FCN SHOULD BE DONE ONLY WITH THE AUTHORIZATION OF FAIRLIGHT

DETAILS OF CHANGE:

1. Cut solder side track joining I.C.. B9 pin 9 and I.C.. B9 pin 10 (PAPAL)

2. Cut solder side track from I. C. B9 pin 4 to plate-thru between I.C.. B8 pin 16 (74LS174) and I.C.. C8 pin 9 (74LS138)

3. Connect I.C.. B9 pin 9 to plate-thru between I.C.. B8 pin 16 and I.C.. C8 pin 9

4. Replace PAPAL with PAPALR3 (18V10)

5. Update pcb revision.

ORIGINATOR: C Alfred DATE: 24/3/93	TEST: DATE:
	PROD: DATE:
SERVICE: DATE:	KIT LIST CHANGE: YES (NO)

fairlight

Page 1 of

FIELD CHANGE NOTICE

DATE 10/ 9 /92
NUMBER 104

ORIGINATOR Chris Alfred **PRODUCT: CMI / MFX**

ASSEMBLY No. CMI-31 **DESCRIPTION** CHANNEL CARD

This FCN applies to REV No: ALL REV 1 **The New REV No is:**

REASON FOR CHANGE:

To improve assertion of *TSTAKEN signal by using higher current driver.

DETAILS OF CHANGE:

Replace IC [redacted] C16 (74LS03) with 7438.

To be done in conjunction with FCN 72
FCN 72 , R4 120 ohm on CMI-41 allows the higher current through the 7438.

ORIGINATOR: C Alfred DATE: 10-9-92	PROD: Mario Pochis 10.9.92 DATE:
SERVICE: Morris DATE: 10-9-92	KIT LIST CHANGE: (YES) NO

fairlight

FIELD CHANGE NOTICE

DATE 14/ 7 /92
NUMBER 95

ORIGINATOR Chris Alfred **PRODUCT: CMI / MFX**

ASSEMBLY No. CMI-31 **DESCRIPTION** CHANNEL CARD

This FCN applies to REV No: CMI-31 2A.4 **The New REV No is:** SEE BELOW

REASON FOR CHANGE:
It has been noted that channel cards crashing is caused by crosstalk along the mother board. The channel refresh line is induced with signals from the data bus.

DETAILS OF CHANGE:

Add 1 X 180pF capacitor to IC A8 (74LS240) between pins 4 and 10.

Alternatively do FCN 96.

This is an important point as only 1 X 180pF capacitor should be installed !

DO NOT MODIFY BOTH THE 8th CHANNEL CARD AND THE DIGITAL MOTHER BOARD.

This modification is to be done only to the 8th channel card (SLOT 8).

The inside of the front panel and / or card should be marked indicating this change.

ORIGINATOR: C E Alfred **DATE:** 16-7-1992

SERVICE MANAGER: **DATE:**

fairlight

FIELD CHANGE NOTICE

DATE 20/ 3 / 92
NUMBER 85

ORIGINATOR Chris Alfred **PRODUCT: CMI / MFX**

ASSEMBLY No. CMI31 **DESCRIPTION** CHANNEL CARD

This FCN applies to REV No: 2A.4T / 1.9AT **The New REV No is:** 2A.4 / 1.9A

REASON FOR CHANGE:
Lengthen address from channel card to waveform buss
to stop waveform memory errors on sampling

DETAILS OF CHANGE:

Revision 2A.4T
Dissconnect modification wire between Ic G15/10 (74ls32) and Ic F16/14 (74s175)
Connect Ic G15/10 (74ls32) to Ic G16/11 (74s74)
update revision number to 2A.4

Revision 1.9AT
Disconnect modification wire between Ic G14/2 (74ls32) and Ic G16/ 6 (74ls175) ??
Connect Ic G14/2 (74ls32) to Ic F14/3 (74s74)
Update revision to 1.9A

[redacted] 69 must be done on CMI39 2 meg Ram cards
FCN.

ORIGINATOR:	DATE:	PROD:	DATE:
SERVICE:	DATE:	KIT LIST CHANGE:	YES NO

ESP

FIELD CHANGE NOTICE

Field Change Notice No: 73

PRODUCT CMI [X] CVI [ ]

ORIGINATOR: Chris Alfred **DATE:** 29 / 5 / 90

ASSEMBLY No: CMI-31

DESCRIPTION: Channel Card

This FCN applies to rev No: 2A.3T **The New rev No is:** 2A.4T

REASONS FOR CHANGE:

Improve assertion of *TSTAKEN signal by using higher current driver.

DETAILS OF CHANGE:

Replace IC E12 ~~12~~ (74LS03) with 7438.

** TO BE DONE IN CONJUNCTION WITH FCN 72 **
FCN 72 R4 120R on CMI 41 waveform supervisor allows the higher current through the 7438.

DEPT	SIGNATURE	DATE	COMMENTS
Project Manager	C E Alfred	22/8/91	
Customer Service	M. Pocknee	22-8-91	

ESP

FIELD CHANGE NOTICE

Field Change Notice No: 61

PRODUCT CMI [x] CVI [ ]

ORIGINATOR: Chris Alfred **DATE:** 16 / 10 / 90

ASSEMBLY No: CMI 31

DESCRIPTION: Channel card

This FCN applies to rev No: 1.9, 2A.3, **The New rev No is:** 1.9T, 2A.3T,

REASONS FOR CHANGE:

Waveform ram corruption while channel cards are running.
(Most prominent in systems with 2 meg ram cards)

DETAILS OF CHANGE:

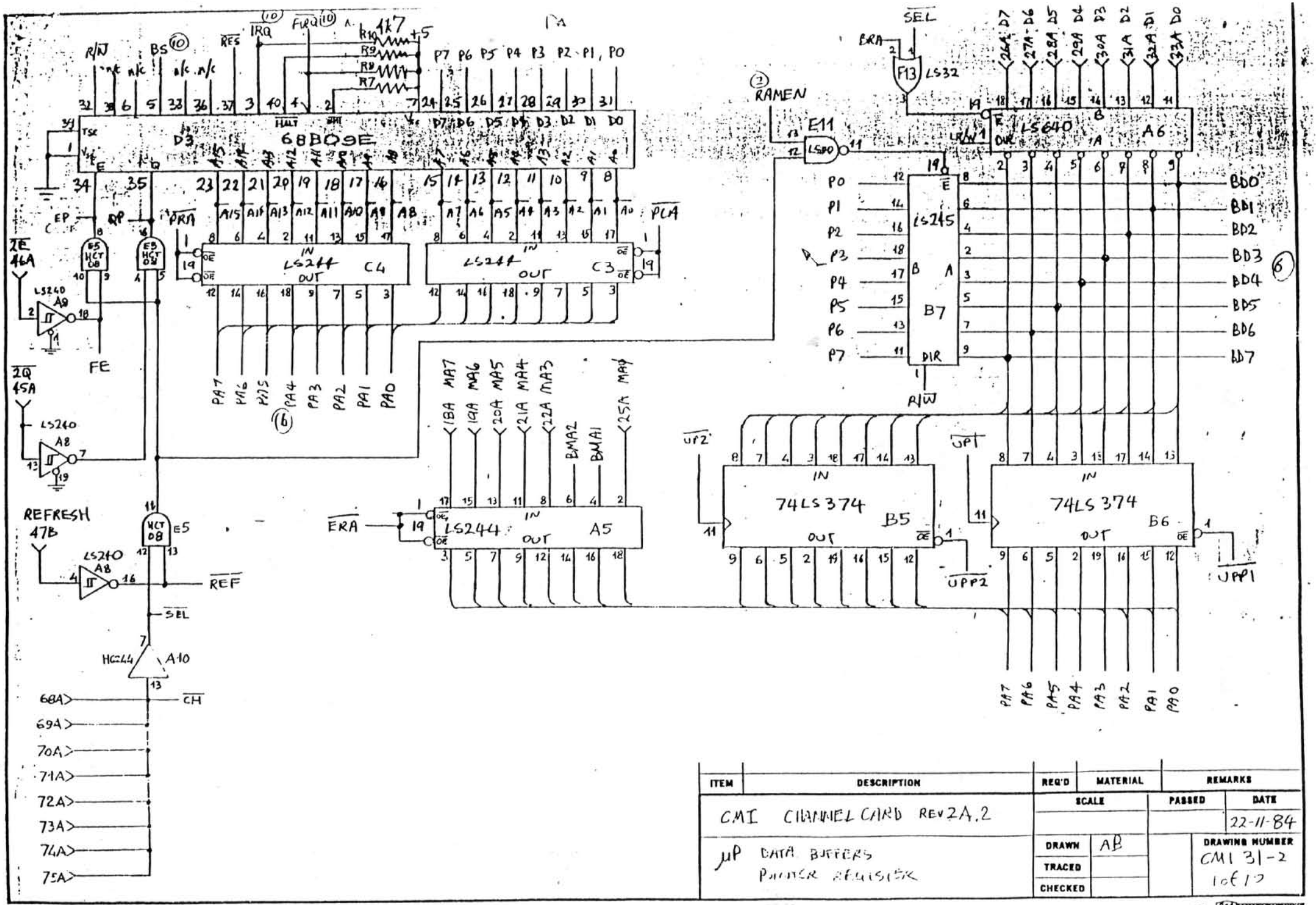
Rev 1.9 cards

1) On solder side, cut track going to G14 (74LS32) pin 2
2) Connect G14 pin 2 to G16 (74LS175) pin 6
3) Update the board revision to Rev 1.9T

REV 2A.3 2A.2 2A.1

1) On component side, cut track going to G15 (74LS32) Pin 10
2) Connect G15 pin 10 to F16 (74LS175) pin 14
3) Update the board revision to Rev 2A.3T or 2A.2T or 2A.1T

DEPT	SIGNATURE	DATE	COMMENTS
Project Manager			
Customer Service			



ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
CMI CHANNEL CARD REV 2A.2		SCALE		PASSED / DATE: 22-11-84
µP DATA BUFFERS POINTER REGISTER		DRAWN: AB		DRAWING NUMBER: CM1 31-2
		TRACED		10 of 12
		CHECKED		

A3

CMI - 31 CHANNEL CARD TEST OS9
continuation

ORIGINAL

TEST FOUR - CHANNEL CARD WAVEFORM ADDRESS CONFLICT

Basically this test for conflict between the Waveform Supervisor and Channel Cards with reference to Waveform addressing.

1\ Boot system from OS9 Hard disk, wait for white square prompt to appear, then press the " TAB " key.
2\ This should leave you in the " Shell " which has a " # " as a prompt.
3\ Type " WSDIAG " then press " RETURN " to enter " KNONDIAG " diagnostics.
4\ Type " XD " then press " RETURN " , then type " MW " then press " RETURN "
5\ Allow to run at least two passes before pressing " ADD " key to stop test.
6\ Any errors will be displayed on the screen.
7\ To exit press " SPACE BAR " then press " RETURN ".

TEST FIVE - SYSTEM OPERATION RECORD/PLAYBACK

This procedure is designed to exercise the Channel card in record mode running under the CMI Disk Recorder

1\ Connect a 1KHz sinewave input from a quality Signal Generator to the reference Analogue to Digital converter, so that you have AES out, which you connect to the Samplers AES input.
2\ Set the AD converter to 48KHz sample rate.
3\ Create a project to accept the reference AES input signal i.e. a stereo/48KHz digital input project. Record at least 4 minutes of audio.
4\ Close the project, then reopen it, enable digital out in usual manner.
5\ Connect AES out from CMI sampler to reference DA converter, and thence the analogue signal to the analogue test device.
6\ Play the recorded clip, and while doing so measure the distortion at the analogue test device, it should be -60 dBu or better , typically -68dBu.
7\ Listening to the clip on playback is highly recommended.
8\ Now copy the clip enough times to other tracks so that all Channels { 16 } are used up. Press play and observe that Channels do not fall over, i.e the Channel leds should not turn off for any period of time during play back.
9\ Setting up a loop on the clip and leaving it loop for about 10 minutes is also advisable, because often cards will show up problems in a loop which would otherwise not be seen.
10\ Creating a 44KHz clip as above is also advised however not an absolute necessity as a 48KHz clip requires more memory and quicker memory access than a 44KHz clip and thus exercises the system to a higher degree.
11\ Take a break, get a cup of coffee and test the next card.

Note: The QDOS tests will test all Channel Cards equally, however the above tests are mainly for Channel card 1 , and as such each card should be tested with the above in slot 1.

JG92

ESP

FIELD CHANGE NOTICE

Field Change Notice No: 59

PRODUCT CMI [Y] CVI [ ]

ORIGINATOR: Mario Paolino **DATE:** 27 / 5 / 90

ASSEMBLY No: CMI 31

DESCRIPTION: Channel Card

This FCN applies to rev No: 1.8 / 1.9 **The New rev No is:** 1.8A / 1.9A

REASONS FOR CHANGE:

1) Malfunctions when auditioning from disc with Rev 8 software.
2) Router occasional mis-routing.

The above problems occur only when Rev 8 software is installed with Rev 1.8 or 1.9 channel cards. The problem is cause by an artwork error in the original PCB design which does not correspond the to circuit diagram. This area of the circiut was previously unused.
One input to an NAND gate was left floating which should have been connected to ground.
About 20% of these cards DO in fact work by chance, however these cards should also have the mods done regardless.

DETAILS OF CHANGE:

1) IC B11 (74HC173) join pin 9 &10 together
2) Mark the board 1.8A or 1.9A respectively.

Revision 2 channel cards do NOT require this modification.

DEPT	SIGNATURE	DATE	COMMENTS
Project Manager			
Customer Service	Mario Paolino	27/5/90	

CMI - 31 CHANNEL CARD TEST PROCEDURE

Requirements:

1 \ Apogee AD500 or similar, Analogue in, AES out
2 \ Apogee DA1000 or similar, AES in, Analogue out
3 \ Hard Disk 1.2GByte running OS9, Rev 10.20
4 \ QDOS Ver 5.01 Diagnostics Boot Floppy Disk
5 \ Neutric A1 or similar, Analogue Test System.

TEST ONE - INTERRUPTS

As an introduction, this test test all Channel Card Interrupts both on board generated and System generated.

1 \ Boot CMI from QDOS Disk by powering up and placing disk in floppy drive. An " = " prompt will appear.
2 \ Type " CHINTTST " then press " RETURN " to open the interrupt test programme.
3 \ Type " INTRPT " then press " RETURN " to set the interrupt test running, any errors will be displayed on the screen. Run test at least twice for consistency purposes.
4 \ Type " Q " then press " RETURN " to quit this test.

TEST TWO - ON BOARD MEMORY

This test verifies correct operation and access to channel card memory from both Channel card processor and System processors.

1 \ Type " CHMEMTST " then press " RETURN " to open memory test programme
2 \ Type " LDRAM " then press " RETURN " to begin on board processor memory test.
3 \ Type " CHRAM " then press " RETURN " to test channel card memory from system processors.
4\ It is recommended to run these tests at least twice.
5 \ All errors found will be displayed on screen
6 \ Type " Q " then press " RETURN " to quit this test.

TEST THREE - PITCH & OCTAVE REGISTER TEST

This test will verify correct operation of on board Pitch and Octave registers.

1 \ Type " CHPITTST " then press "RETURN " to open Pitch/Octave test.
2 \ Type " PIT " then press " RETURN " to begin the test
3 \ Observe the Channel card Leds sequence through the channels as the test runs
4 \ Now type " OCT " then press RETURN " to begin the Octave register test.
5 \ Again it is recommended to run these tests at least twice.
6 \ Any errors occuring will be displayed on the screen.
7 \ No errors , excellent. Now type " Q " then press " RETURN " to quit this test.

As an additional Titbit to the above, if you wish to test only one of a number of Channel cards, then use " SEL ,C=X " where X is the Channel card number. This can only operate from within any of the above programmes.

Now turn over to the OS9 test procedure

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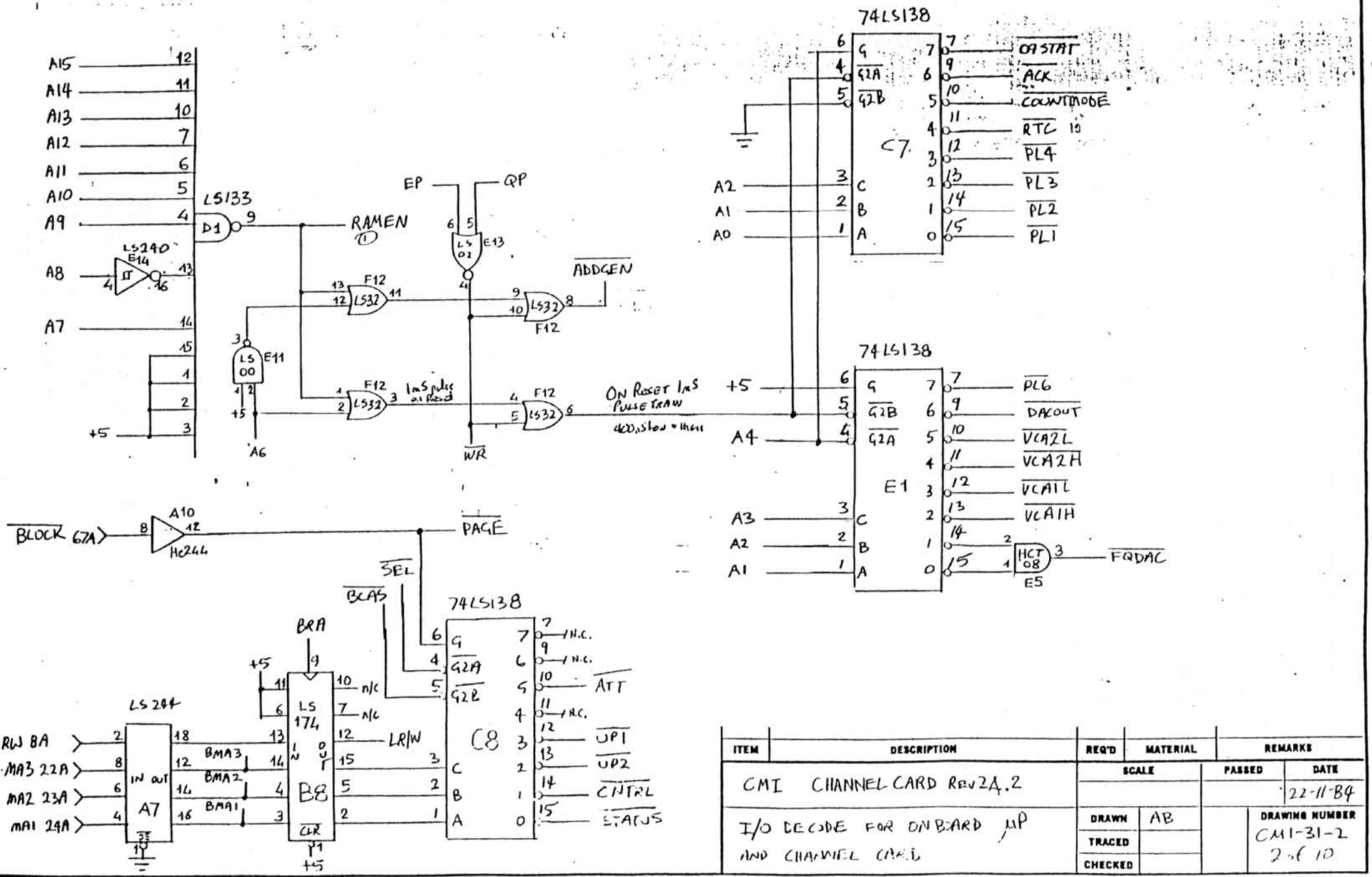
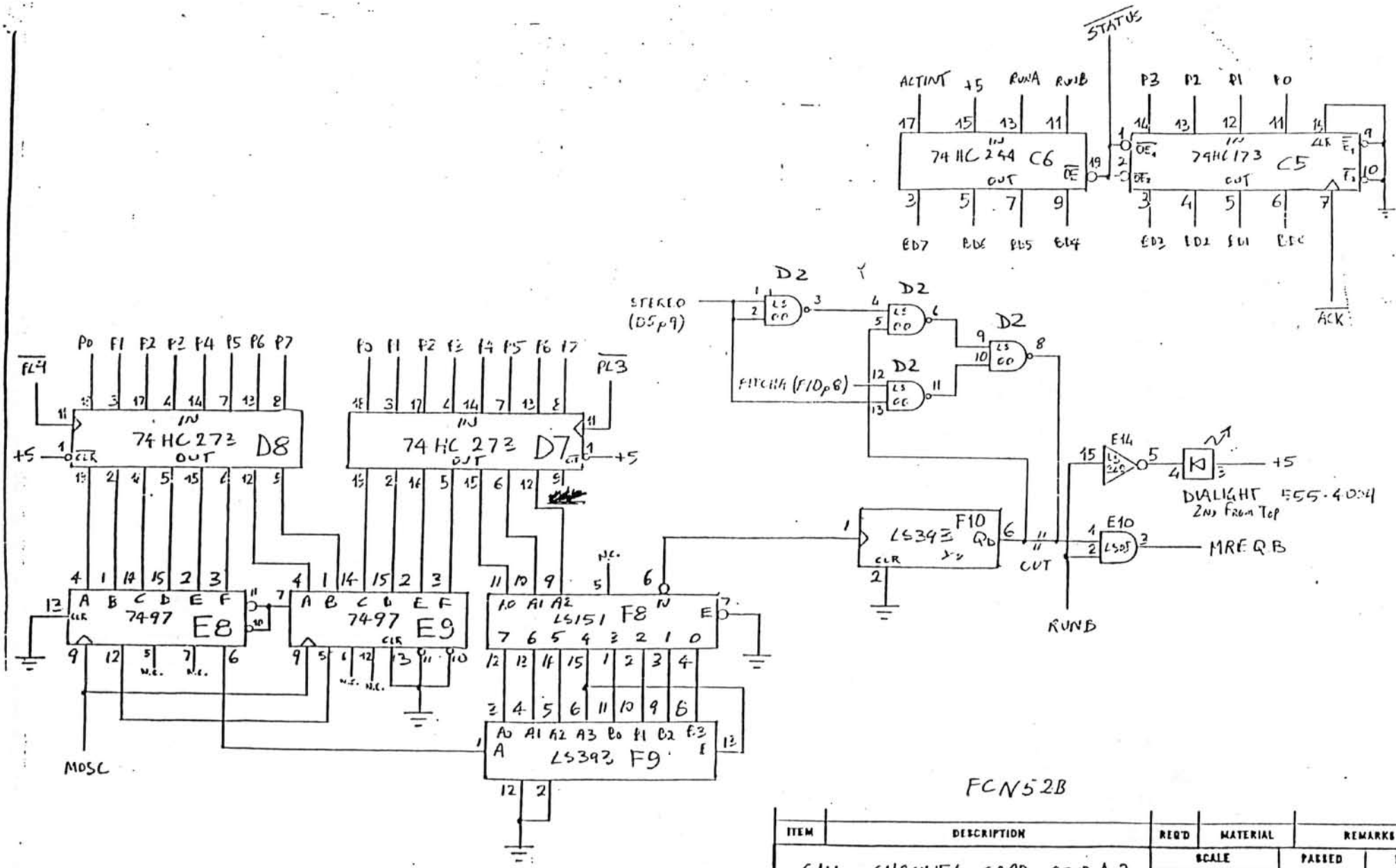


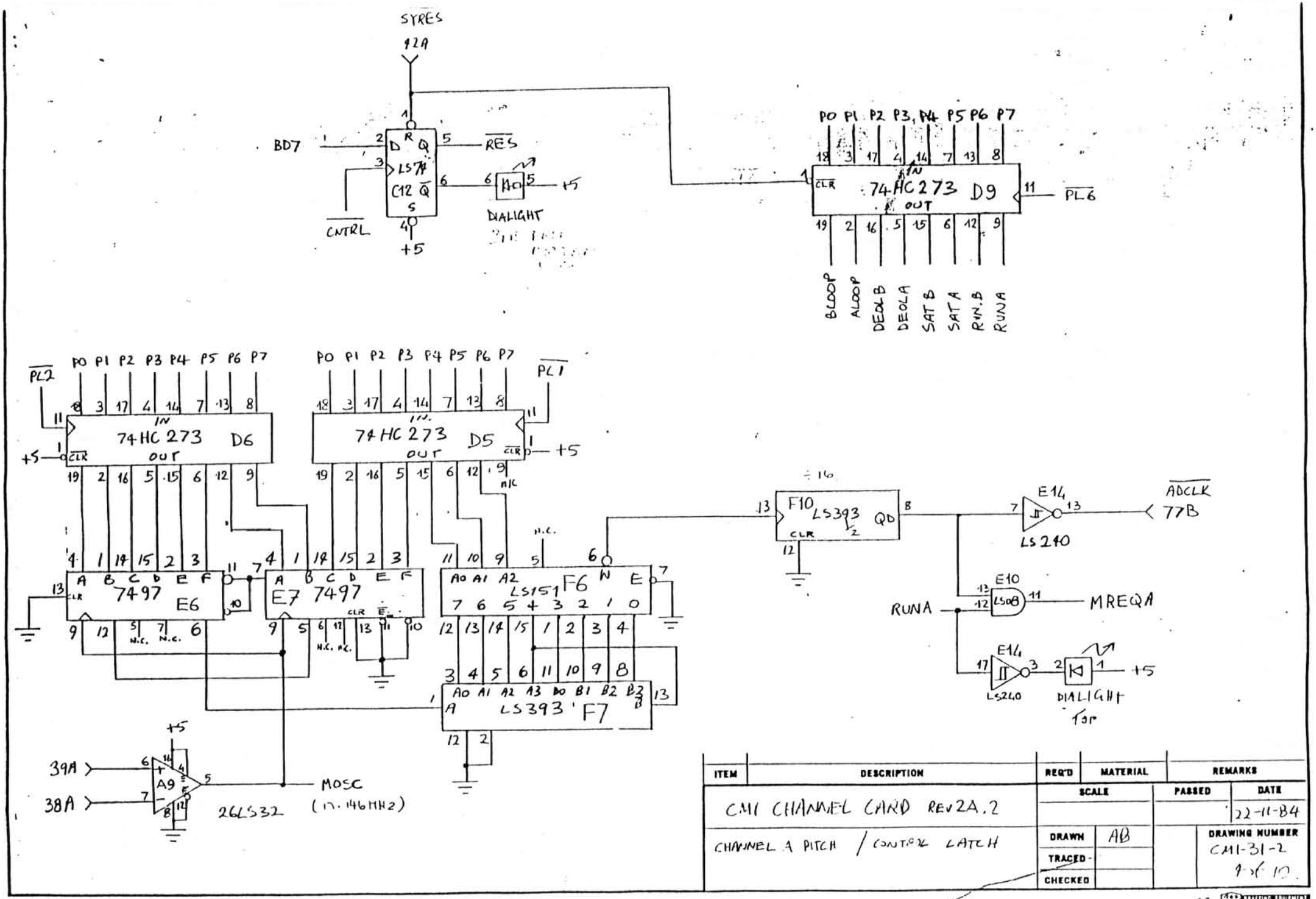
ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
CMI CHANNEL CARD REV 2A.2		SCALE		PASSED / DATE: 22-11-84
I/O DECODE FOR ONBOARD µP AND CHANNEL CARD		DRAWN: AB		DRAWING NUMBER: CM1-31-2 2 of 10
		TRACED		
		CHECKED		

A3



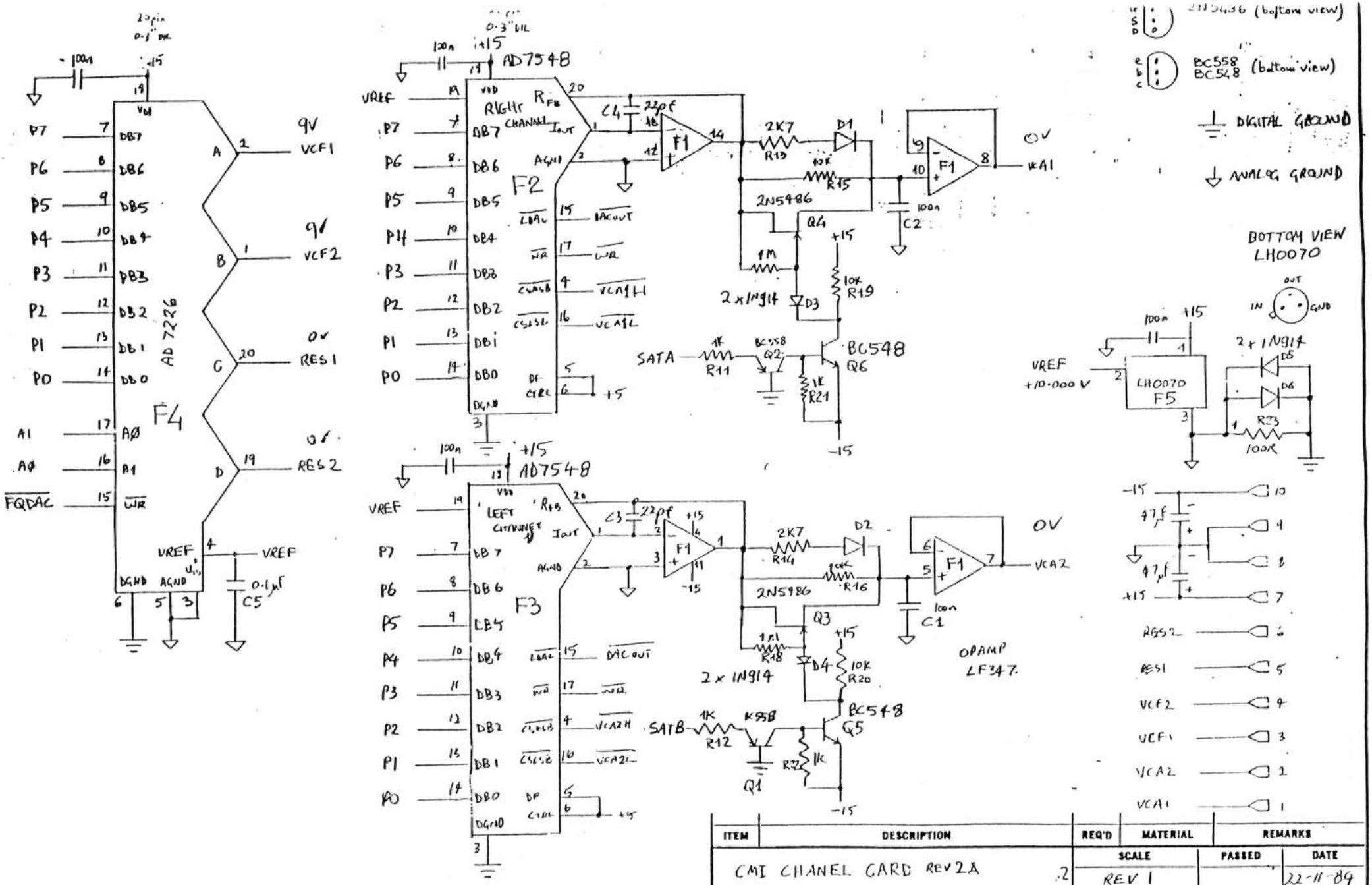
FCN52B

ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
CM1 CHANNEL CARD REV2A.2		SCALE	PASSED	DATE 22-11-84
CHANNEL B PITCH		DRAWN AB		DRAWING NUMBER CM1-51-2 3 of 10
		TRACED		
		CHECKED		



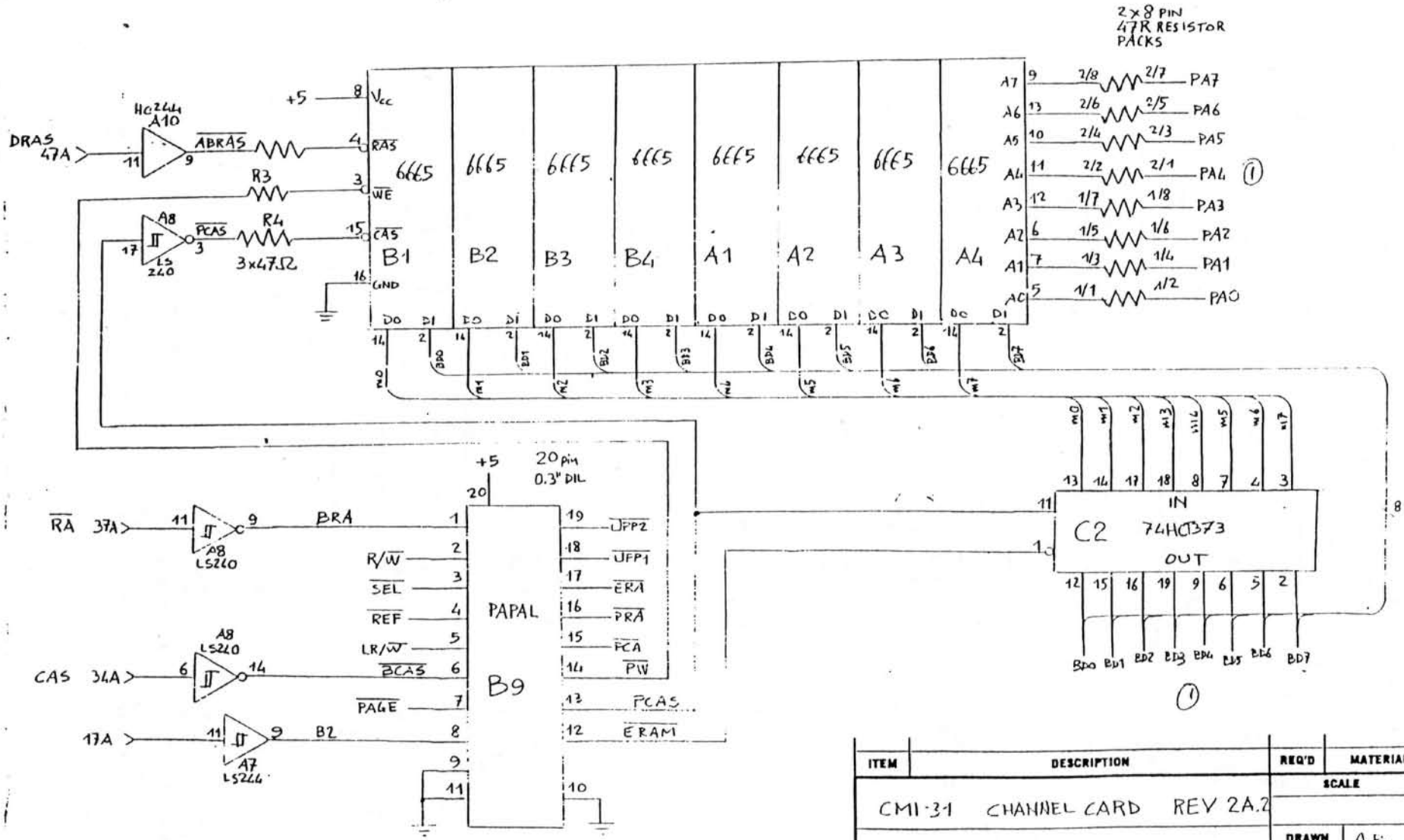
ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
CMI CHANNEL CARD REV2A.2		SCALE		PASSED / DATE: 22-11-84
CHANNEL A PITCH / CONTROL LATCH		DRAWN: AB		DRAWING NUMBER: CMI-31-2
		TRACED:		1 of 10
		CHECKED:		

A3



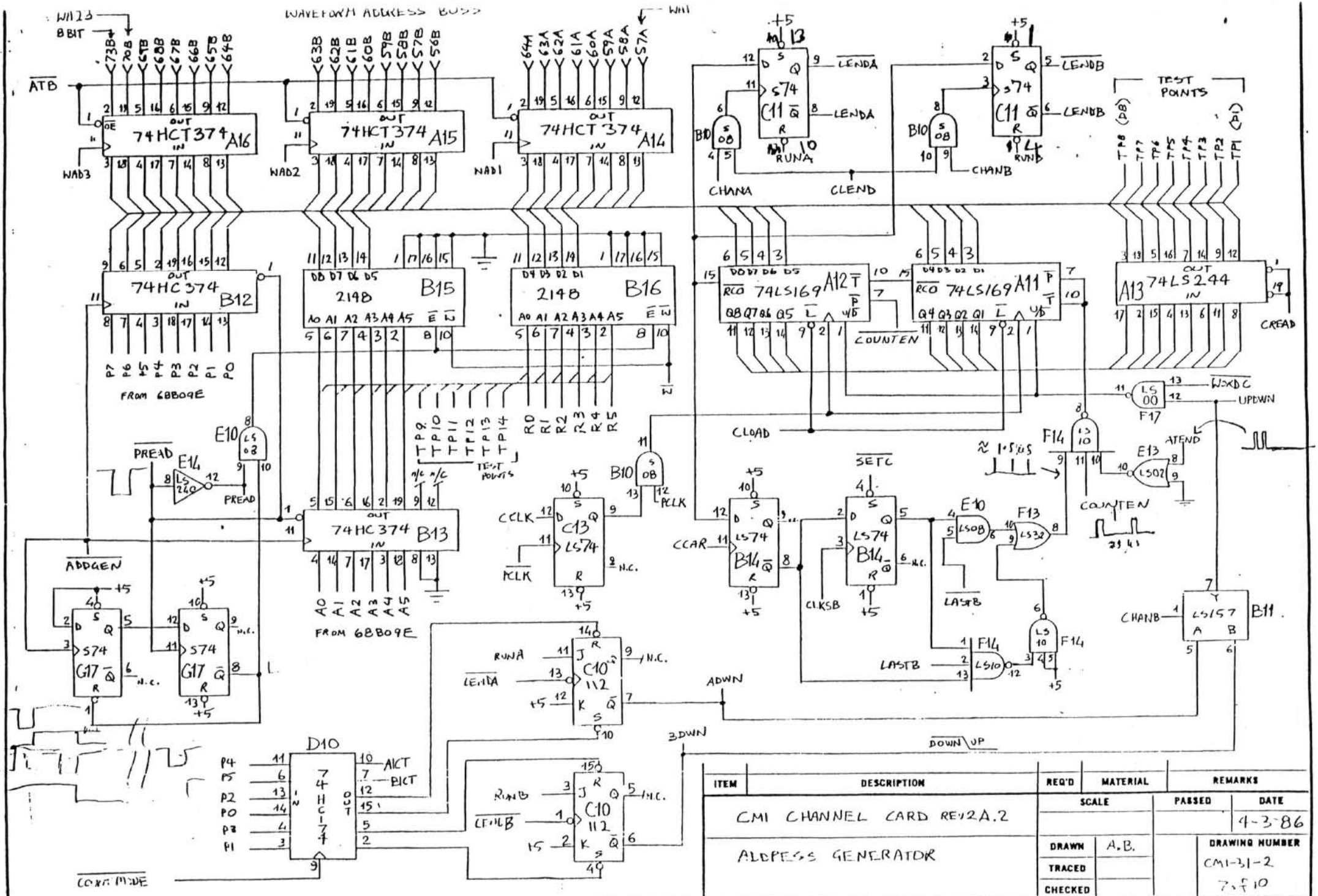
ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
CMI CHANEL CARD REV 2A		SCALE	PASSED	DATE
		REV 1		22-11-84
		DRAWN AB		DRAWING NUMBER
		TRACED		CMI-31-2
		CHECKED		5 of 10

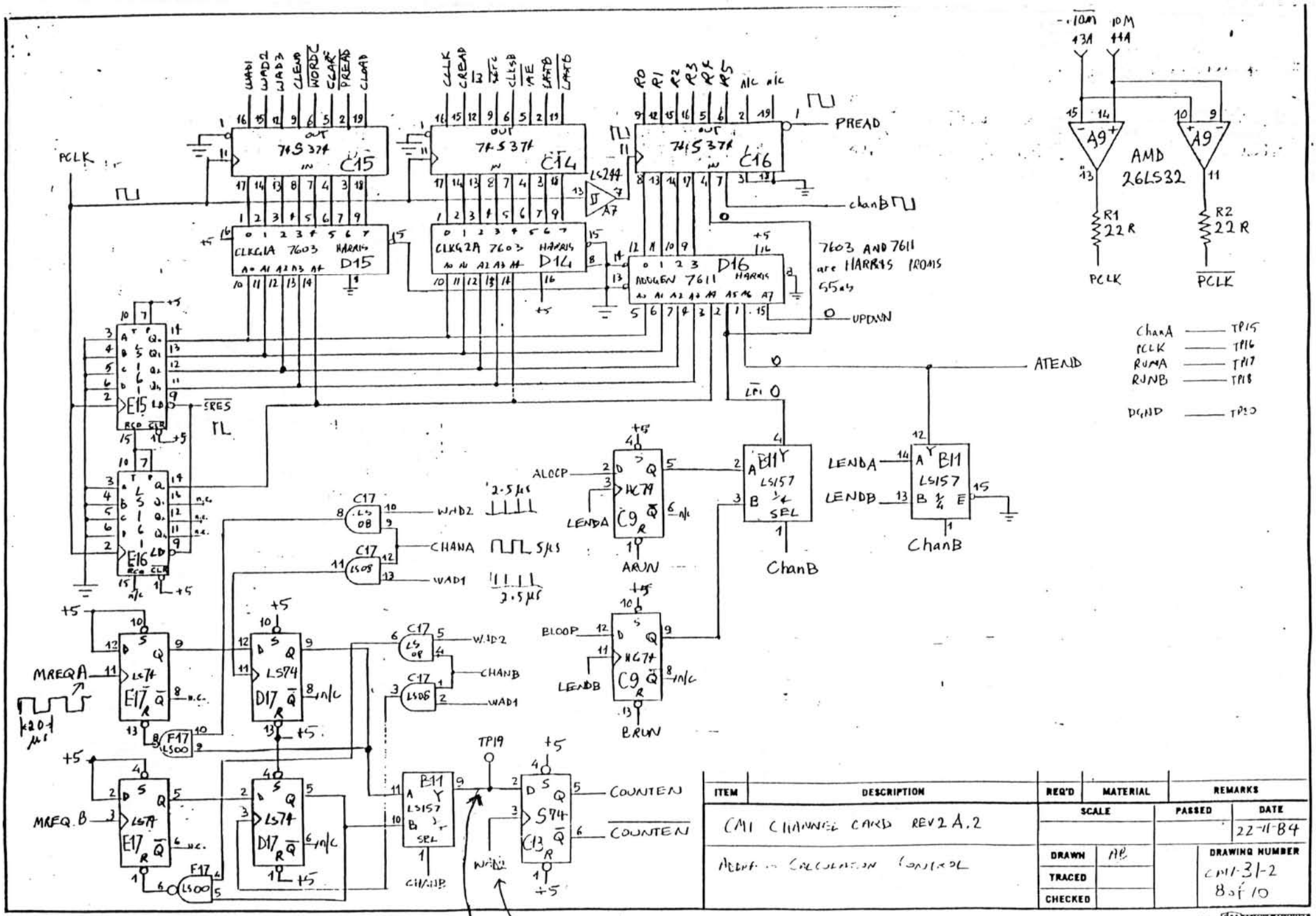
A3



ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
CM1-31 CHANNEL CARD REV 2A.2		SCALE		PASSED / DATE 22-11-84
PROGRAM RAM / ADDRESS CONTROL		DRAWN AE		DRAWING NUMBER CM1-31-2
		TRACED		6 of 10
		CHECKED		

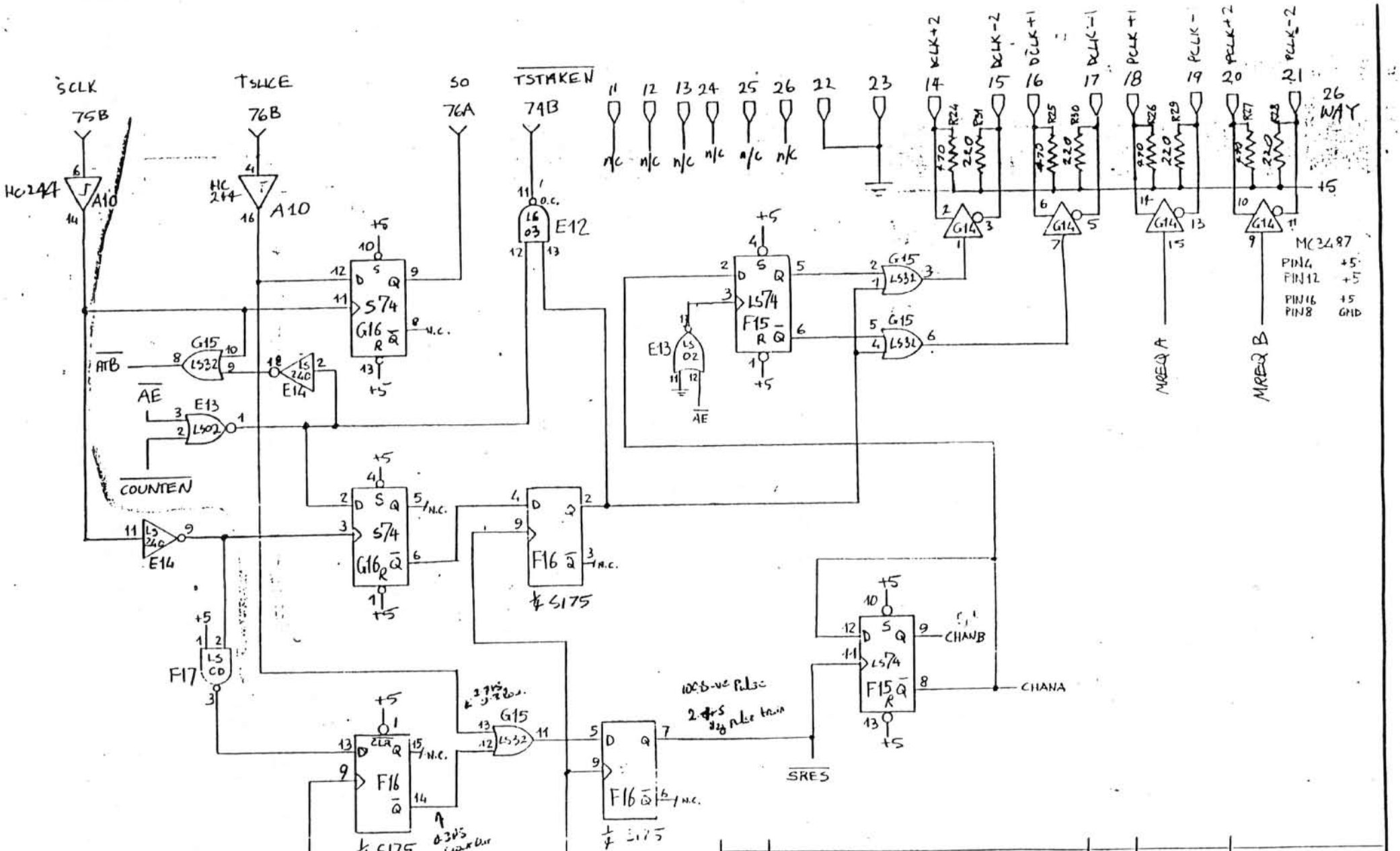
A3


WAVEFORM ADDRESS BUSS
WA23
8 BIT
WA1
ATB
74HCT374 A16
74HCT374 A15
74HCT374 A14
WAD3
WAD2
WAD1
74HC374 B12
2148 B15
2148 B16
FROM 68B09E
74HC374 B13
PREAD
ADDGEN
CCLK
PCLK
CCAR
SETC
CLOAD
74LS169 A12
74LS169 A11
74LS244 A13
COUNTEN
CREAD
WRDC
UPDWN
ATEND
LENDA
LENDB
RUNA
RUNB
CHANA
CHANB
CLEND
TEST POINTS
CLKSB
LASTB
RUNA
LENDA
ADWN
BDWN
DOWN UP
CONTMODE
D10
74HCT74
AICT
BICT
C10 112
C13 LS74
B14 LS74
G17 S74
B11 LS157
F17 LS00
F14 LS10
F13 LS32
E13 LS02
E10 LS08
B10 S08
E14 LS240
B09 LS03
ITEM
DESCRIPTION
REQ'D
MATERIAL
REMARKS
CMI CHANNEL CARD REV2A.2
ADDRESS GENERATOR
SCALE
PASSED
DATE
4-3-86
DRAWN
A.B.
TRACED
CHECKED
DRAWING NUMBER
CMI-31-2
7 of 10
A3



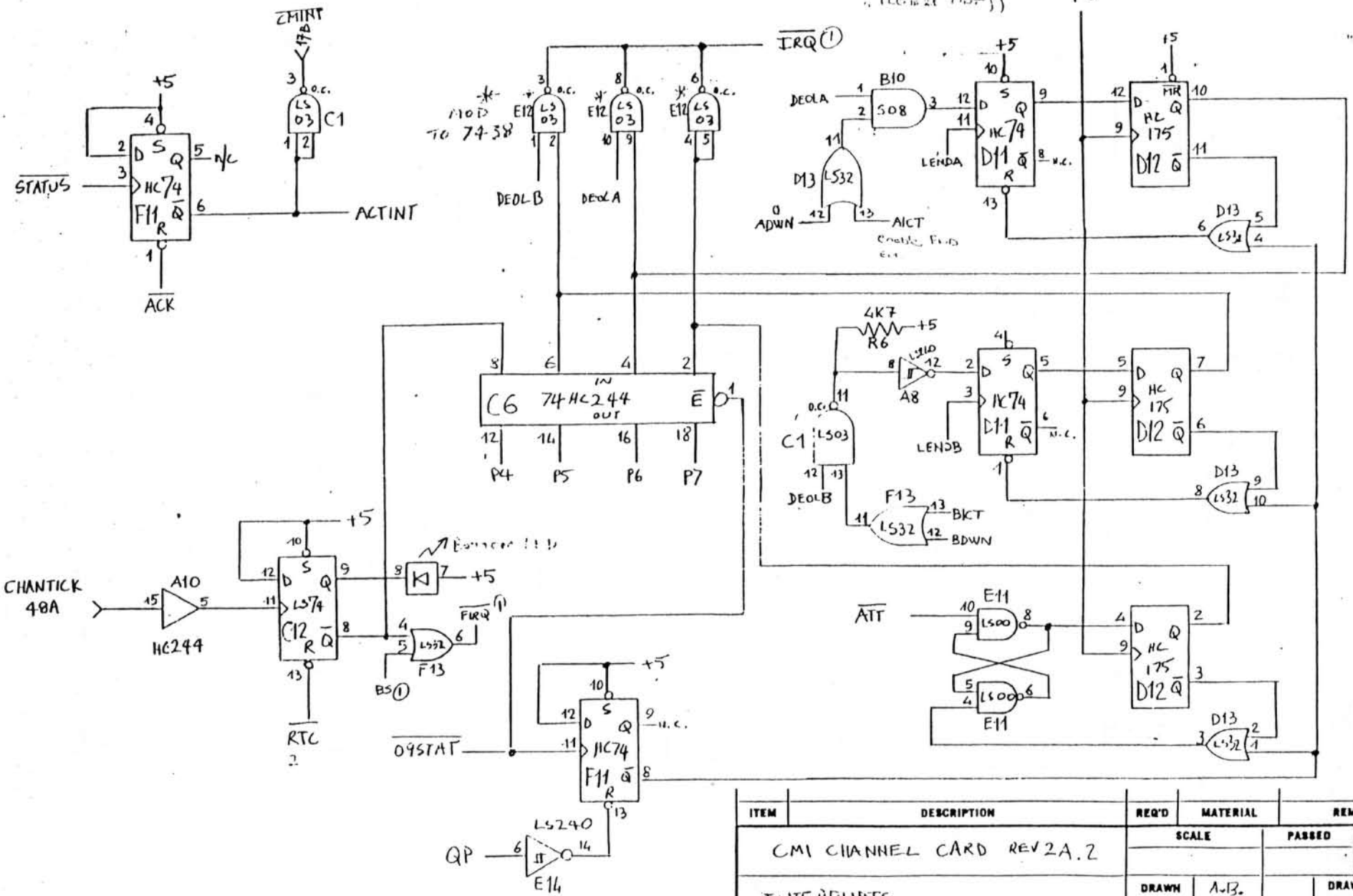
ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
	CM1 CHANNEL CARD REV 2 A.2	SCALE		PASSED / DATE: 22-11-84
	ACQUISITION CALCULATION CONTROL	DRAWN: AB		DRAWING NUMBER: CM1-31-2 8 of 10
		TRACED		
		CHECKED		

A3

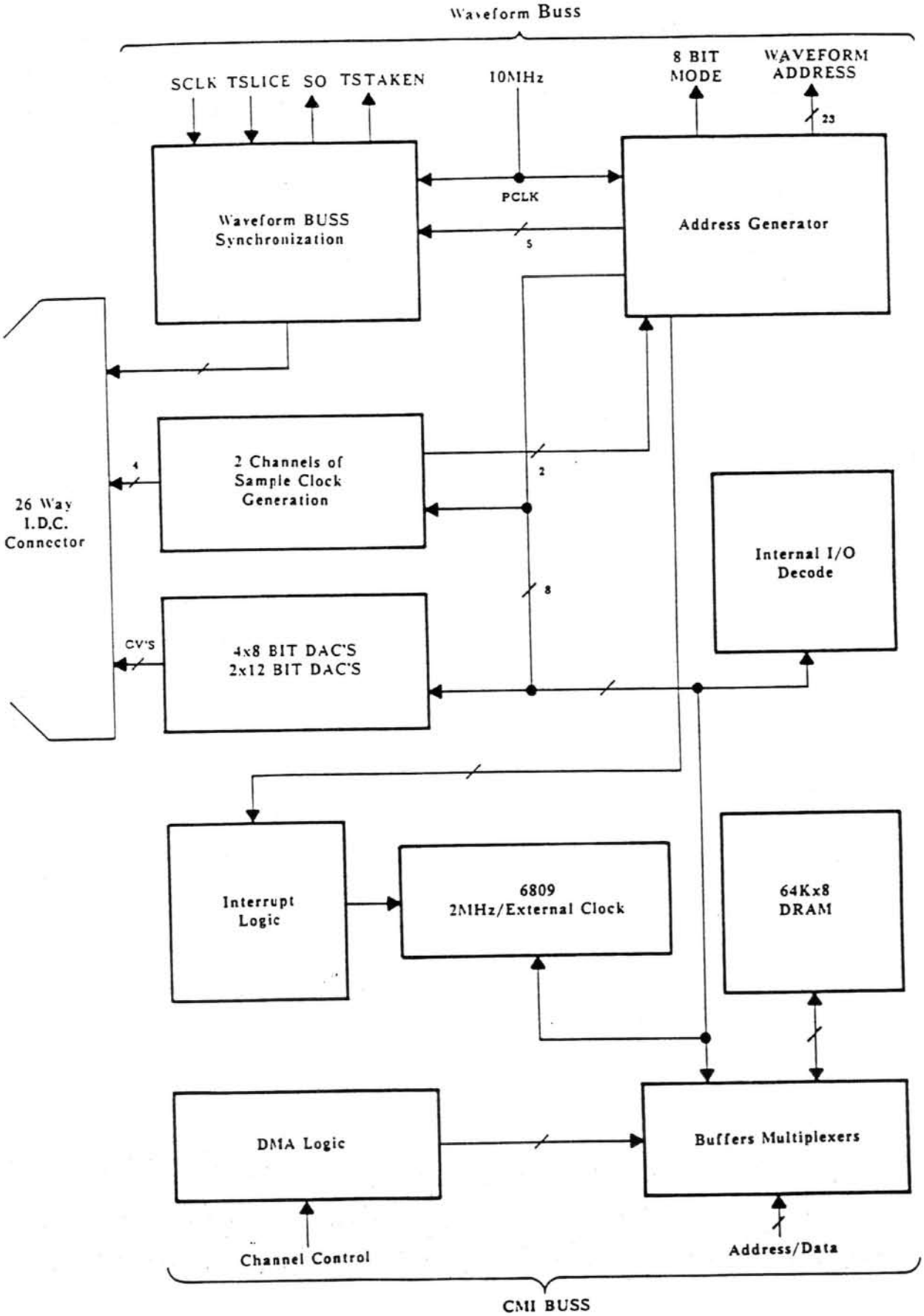


ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
CHANNEL CARD REV 2A.2		SCALE	PASSED	DATE 22-11-84
WAVEFORM BUS SYNCHRONIZATION		DRAWN AB		DRAWING NUMBER CM1-31-2
		TRACED		9 of 17
		CHECKED		

A3


DEOL - enable end of loop interrupt
FE
CMINT
17B
IRQ (1)
+5
STATUS
HC74
F11
D
S
Q
R
N/C
ACK
ACTINT
C1
LS 03
o.c.
E12
MOD TO 74-38
DEOL B
DEOL A
B10
S08
DEOLA
LENDA
D13
LS32
ADWN
AICT
HC 175
D12
D11
4K7
R6
LS10
A8
C1
LS03
LENDB
DEOLB
F13
BICT
BDWN
C6
74HC244
IN
OUT
P4
P5
P6
P7
CHANTICK 48A
A10
HC244
LS74
C12
RTC
BS (1)
FIRQ (1)
09STAT
QP
LS240
E14
ATT
E11
LS00
ITEM
DESCRIPTION
REQ'D
MATERIAL
REMARKS
CMI CHANNEL CARD REV 2A.2
SCALE
PASSED
DATE
1-2-85
INTERRUPTS
DRAWN
A.B.
TRACED
CHECKED
DRAWING NUMBER
CM1-31-2
A3

Channel Card Block Diagram



and resistor on the CC connecting DGND and AGND are to stop the two from drifting too far apart if the AGND and DGND connection is broken.

The DACs cannot be accessed by external CPUs, only the CCP.

The AD7226 at F3 is a quad 8 bit voltage output DAC. It receives the 2 least significant address lines to select its 4 DACs on byte boundaries. This DAC produces 2 channels of filter cutoff and resonance Control Voltage (CV). Each is 0 to 10 volts.

The filter cutoff frequency range is from 20Hz to 20kHz with control values of 0V (00H) to 10V (FFH).
The filter resonance changes from flat, 0V (00H) to oscilation at 10V (FFH).

The AD7548s at F1 and F2 are 12 bit, right justified DACs with an 8 bit buss interface. They are connected so that the 16 bit value written to them is only latched into the 12 bit DAC after pin 15, DACOUT, is accessed as a seperate operation. The output of the current to voltage converters is a CV with the range 0 to -10 Volts. The control range is approximately 95db. 0V (X000H) is maximum attenuation. -10V (XFFFH) is no attenuation, 0db.

When a sound is being played out, its amplitude control voltage will be updated every 1ms and thus the DAC should be accessed at that rate.

These CVs have a software selectable time constant or "zippa filter" .This allows for fast attacks on envelopes and "quiet " amplitude control at other times. This is selected by the SATA and SATB control latch outputs.

Program Ram And Address control
(refer schematic CMI-31-06)

The 64k of DRAM and the address multiplexors are controlled from the PAPLA, (Page Addressing Programable Logic Array). The PAPLA has as inputs CPU buss signals and the 2 CC select signals. The DRAMs require 16 address lines and to get these into the 16 pin package they are latched internally and use an external 8 bit buss and 2 latching strobes, refered to as Row Address Strobe (/RAS) and Column address strobe (/CAS). The CAS signal also doubles as the data enable strobe. Refer to the Memory data books for exact details.

Because of the propagation delay in the PAL, the Row Address Strobe for the RAMs must be delayed in time with respect to the buss RAS signal. This is done on the CSC to generate ABRAS.

Depending on the state of the PAPLA inputs, it will enable to the DRAM's address inputs , the CCPs addresses, P1 PAGE register and the least significant bits of the external address buss, P2 PAGE register and the least significant bits of the external address buss, or the refresh address from the external address buss.

When there are no external accesses or refresh, then the CCPs address is enabled to the RAM.

CAS to the RAMs is disabled whenever an external access to the CCs control registers occurs.
RAM refreshes use dummy reads from the current refresh address.

Address Generator and Control

(refer schematics CMI-31-07.08. Address Generator and Control Signals)

The address generator (ADDGEN) calculates the sample addresses when playing out waveform ram. It calculates 24 bits of waveform address for the 2 audio channels on the card.

The ADDGEN's 24 bit output is interpreted as 23 bits of address and a "mode" bit by the WRAM. The most significant bit is used to select 8 or 16 bit sounds, and must be set accordingly when issuing loop start addresses.

Each audio channel has 2 loops associated with it. Each loop is initialized with a start address and a loop length, in samples. Two loops are needed to allow the contents of one loop to be played while the other is being initialized.

This allows such things as playing the sound in segments that are not sequential. The switching from one loop to the other only occurs at the end of the loop.

The hardware that generates the 24 bit addresses for the waveform does so 8 bits at a time. The machine is basically a small 8 bit wide RAM, B13 and B14, incrementer, B11 and B12 and logic to generate the sequence of clock and enable signals to do the required operations. The sequence of clocks results in operations on 24 bit numbers of load, store, NOP and add 1.

To do a 24 bit increment with this hardware the following sequence must be performed.

The least significant byte is loaded into the incrementer and incremented by one, by enabling the count input of the counter and clocking the counter. The ripple carry out (RCO) of the incrementer is clocked into a F/F to determine if the counter overflowed. This incremented byte is then written back to its original RAM location.

The middle byte is then loaded into the incrementer. The output of the F/F that clocked the RCO from the first byte increment is then fed into the count enable input of the incrementer and the counter clocked. This byte will only be incremented if the least significant byte overflowed. The RCO from the incrementer is then clocked into another F/F and the middle byte written back to its original RAM location.

The most significant byte is then loaded into the incrementer. The outputs of the two RCO F/Fs are ANDed together and feed into the count enable input of the incrementer, and the counter is clocked. The most significant byte will only be clocked if the middle and least significant bytes overflowed. The most significant byte is then written back to its original location.

Address increments, however, are syncronized to the channnels pitch clocks. This means that not all cycles allocated to incrementing the addresses, actually result in the address being incremented. A signal syncronizing the pitches to the ADDGEN hardware disables the incrementing of the address bytes on unused address calculation cylces.