The following is a general outline of the address calculation sequence for one channel.

```
while power applied
do
 write 24 bit waveform address to address latches A14,A12,A13

    if end of loop flag is 1, F13
      then
          reset loop counter to start
          value and clear end of loop flag
      else
         inc loop counter

    end

    if end of loop
      then
          reset wave address to start
          value and set end of loop flag
      else
          inc wave address
          clear end of loop flag
     end
end
```

Address Generator Clock generation

The state counters are E14 and E13. They are made to count to 24 by being reset after 24 clock cycles by the waveform buss syncronization logic, via signal $\overline{\text{SRES}}$. The output of the counters go to the address inputs of the control PROMS, at D14, D15 and D13. These Bipolar PROMS contain the clock and address sequences needed to control the clocking and enabling of the ADDGEN hardware. The PROM outputs are deglitched by the octal latches on their outputs, C14, C15 and C13. There are 15 clock signals generated by the clock generating PROMs. There are 6 address bits generated by the ADDGEN PROM and loop select and channel select lines.

Pitch Clock Synchronization

The sequence of F/Fs and multiplexer at F9, F11 and F15 syncronize the incrementing of waveform addresses to the rising edges of the pitch clocks. The calculation of the next sample address is carried out by the address generator on the next cycle allocated to that calculation after the rising edge of that channels pitch clock. The result is that COUNTEN goes active for one cycle.

The COUNTEN signal is used to enable the increment operation. The ADDGEN is normally going through the sequence that does the address calculations, but nothing in fact is incremented because of the inactive COUNTEN signal.

Active COUNTEN will also pull the TSTAKEN (time slice taken) active and inform the WBUSS control logic on the Waveform Processor that the next waveform memory cycle will be used by a CC.

At the end of the memory cycle the channel card will also generate the clock to clock data into the Audio Rack, via the DCLK1, DCLK2 and PCLK1, PLCK2.

The operations performed in each clock cycle are:-

0 read WADDRESS1 write to output latch 1
1 read WADDRESS2 write to output latch 2
2 read WADDRESS3 write to output latch 3

	if endofloopflag set	if no endofloopflag
3	read looplenght1	read WORDCOUNT1
4	nop	inc
5	write WORDCOUNT1	write WORDCOUNT1
6	read looplength2	read WORDCOUNT2
7	nop	inc
8	write WORDCOUNT2	write WORDCOUNT2
9	read looplength3	read WORDCOUNT3
10	nop	inc
11	write WORDCOUNT3	write WORDCOUNT3
12	nop	

The end of loop F/F is set here if the end of a loop has been reached. It is clear otherwise.

	if end of loop then set endloopflag	if not end of loop clear endloopflag
13	read STARTLOOP1	read WADDRESS1
14	nop	inc
15	write WADDRESS1	write WADDRESS1
16	read STARTLOOP2	read WADDRESS2
17	nop	inc
18	write WADDRESS2	write WADDRESS2
19	read STARTLOOP3	read WADDRESS3
20	nop	inc
21	write WADDRESS3	write WADDRESS3
22	write to control ram from proccessor	
23	nop	

The parameters are organized in the ADDGEN ram so that changing the upper two address lines to the ram, makes the ADDGEN calculate values for the other channel or the other loop.

The current loop for channel A and B is set in F/F C16 by the CCP. These F/F are set to loop1 whenever the channel is stopped.

The end of loop flags, F13, are also set when a channel is stopped. This is done because the only time the loop values are initialized is when an end of loop occurs.

When the CCP writes the loop values to the ADDGEN ram, the CCP's data and least significant 6 bits of address are latched at C11 and C12. This has to be done because the write cycle for the CCP last for 500ns while that for the ADDGEN lasts 100ns. The ADDGEN and the CCP are also not synchronized, so the CCP's data is latched until the ADDGEN is able to write it to its RAM, which happens every 2.4 microseconds. When the write to ADDGEN ram occurs, the latch containing the CCP's address (C12) is enabled instead of the addresses from the ADDGEN PROM (C13).

The 20 test pins are used to connect a logic analyser to the ADDGEN machine for debugging,

Waveform Buss Syncronization

(refer schematic CMI-31-09)

The WBUSS is controlled by the SCLK signal. The Channel cards take turns in using the WBUSS by only using the cycle following an active $\overline{\text{TSLICE}}$ signal on their $\overline{\text{TSLICE}}$ input. Each card uses half of F/F F14 as a bit in a shift register that is shifted left on each rising edge of SCLK. So that only one CC has an active $\overline{\text{TSLICE}}$ signal at a time.

The current channel being calculated by the ADDGEN is determined by half of G15. The other half of G15 is used to steer the data clock to the correct audio channel on the audio board.

CCs only use their allocated WBUSS slice, if COUNTEN is valid. If a WBUSS cycle is granted and COUNTEN is active then $\overline{\text{TSTAKEN}}$ and $\overline{\text{ATB}}$ will be generated as will the DCLKs to the Audio rack.

This will result in a read from Waveform RAM and the data being clocked into the first set of latches on the audio board for the apropriate channel. The WP generates the read and waveform address strobe signal, to the RAM on receiving the $\overline{\text{TSTAKEN}}$ signal from the channel card.

The gated sample clocks are cabled to the Audio Rack via differentian lines.

Channel Card Processor Interupts

(refer schematic CMI-31-10)

The "chantick" from the 6840 on the Channel Card Support is used to provide a real time clock reference to all channel cards. This is an FIRQ to the channel card processors at the 1 msec rate set by the CSC. The FIRQ is used to time the VCA (and VCF) ramp generating software. The rising edge of chantick sets half of F/F E1 which causes an FIRQ to the CCP. This is the only source of FIRQ on the card. The CCP resets this F/F in its interupt service routine by accessing the $\overline{\text{RTC}}$ location.

The CC can interrupt the CMI by accessing its /ACK location which will reset F/F D2. This interupt will be reset when the CMI reads the CC's status register.

There are 3 sources of IRQ on the CC to the CCP. They are the interrupt from the CMI, the end of loop interupt from channel A and the end of loop interupt from channel B. Because of this, a status register is required to determine the source of the IRQ. This is half of the buffer at A5. Valid interupts are cleared when the status register is read. Shortly after the status read pulse occurs, pin 8 of E1 will go low briefly. This will reset the interupt F/Fs D1 and half of F10, that were valid before the previos CCP cycle. This double buffering of interupts is to stop interupts from being lost, if they occurred during the status register read.

Channel Card Equates and Definitions
Addressing from external CPUs.
The hardware equates for the card are:-

```
CNTRL  EQU    2  0= reset CCP
STAT   EQU    0  processor interupt and status byte
PAG2   EQU    5  Page of CC RAM to be accessed by P2
PAG1   EQU    6  Page of CC RAM to be accessed by P1
ATT    EQU    A  access to interupt CCP
```

STAT bit definitions

```
0     command bit
1        "
2        "
3        "
4     RUNB
5     RUNA state
6     channel card processor reset line
7     active interupt from this channel card
```

Support card Mask related equates

```
CHANS  EQU    E080  access channels via the masks
CHAN1  EQU    E000  direct access to channel 1
CHAN2  EQU    E010        "
CHAN3  EQU    E020        "
CHAN4  EQU    E030        "
CHAN5  EQU    E040        "
CHAN6  EQU    E050        "
CHAN7  EQU    E060        "
CHAN8  EQU    E070  direct access to channel 8
```

On board Processor's I/O

The Channel Card Processors equates
Control voltage DACs

```
AFILT  EQU    FE80   8 bit filter cutoff channel A
BFILT  EQU    FE82   8 bit filter cutoff channel B
ARES   EQU    FE81   8 bit filter Q at cutoff
BRES   EQU    FE83   8 bit filter Q at cutoff
AVOL   EQU    FE85   12 bit right justified
BVOL   EQU    FE89   12 bit right justified
DACOUT EQU    FE8C   access to output above two to DACs
```

Rate multipliers

```
APITCH EQU    FE90   15 bits, right justified
BPITCH EQU    FE92   15 bits, right justified
```

Control latch

```
CNTRL  EQU    FE8E
0      channel B loop select  0= loop 1
1      channel A loop select  0= loop 1
2      enable end of loop channel B IRQ
3      enable end of loop channel A IRQ
4      volume zipper noise filter B (1= on)
5      volume zipper noise filter A (1= on)
6      run channel B
7      run channel A
```

Address Generator

Each location is write only and each byte must be written no faster than every 2.4 microseconds
All are 24 bit values, stored least significant byte first.
The most significant bit of the start addresses determine 8 or 16 bit accesses
0 = 8 bit
1 = 16 bit

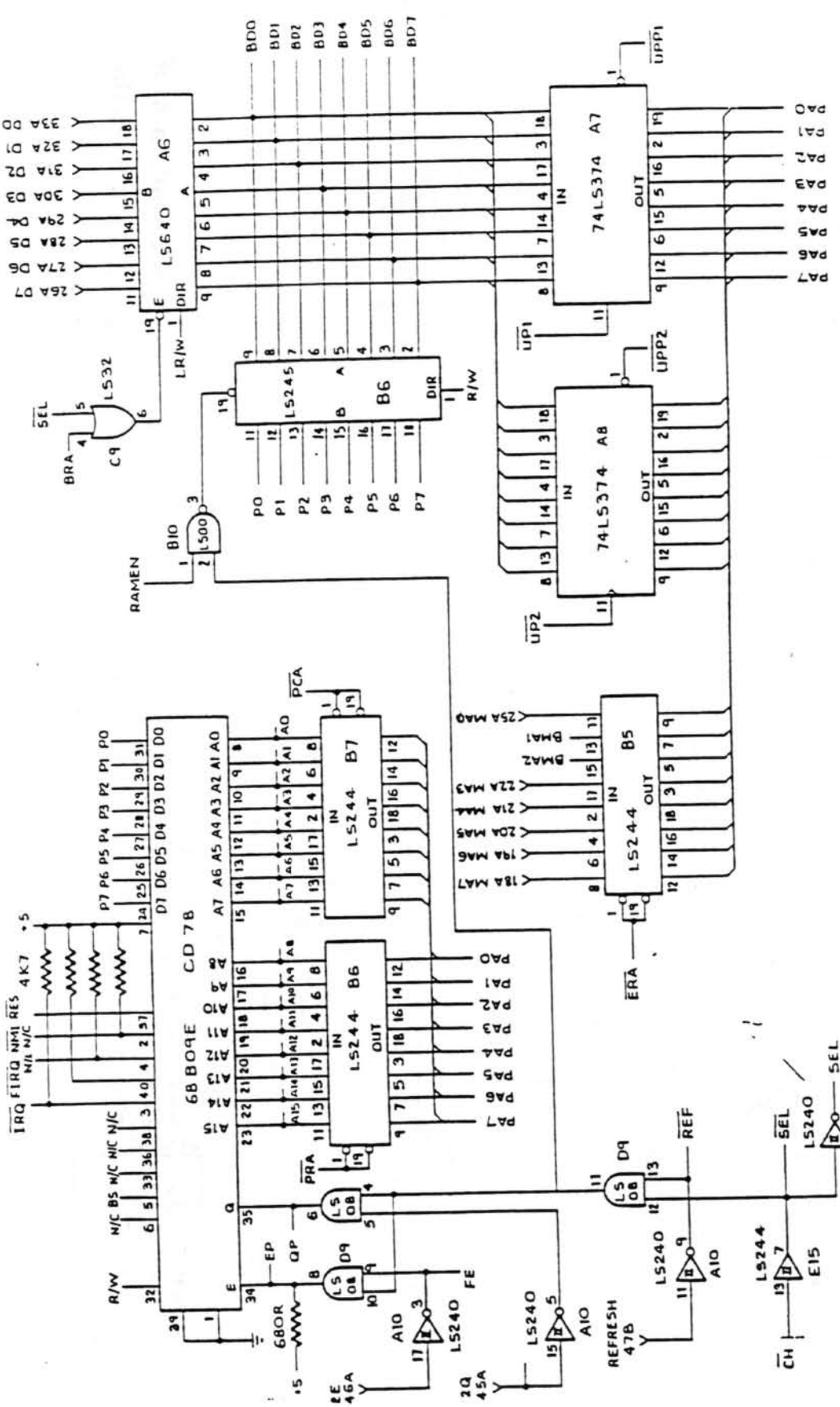
```
ASTRT1 EQU    FEC0   start address channel A loop 1
ALOOP1 EQU    FEC3   length loop 1 channel A
ASTRT2 EQU    FED0   start address channel A loop 2
ALOOP2 EQU    FED3   length loop 2 channel A

BSTRT1 EQU    FEE0   start address channel B loop 1
BLOOP1 EQU    FEE3   length loop 1 channel B
BSTRT2 EQU    FEF0   start address channel B loop 2
BLOOP2 EQU    FEF3   length loop 2 channel B
```

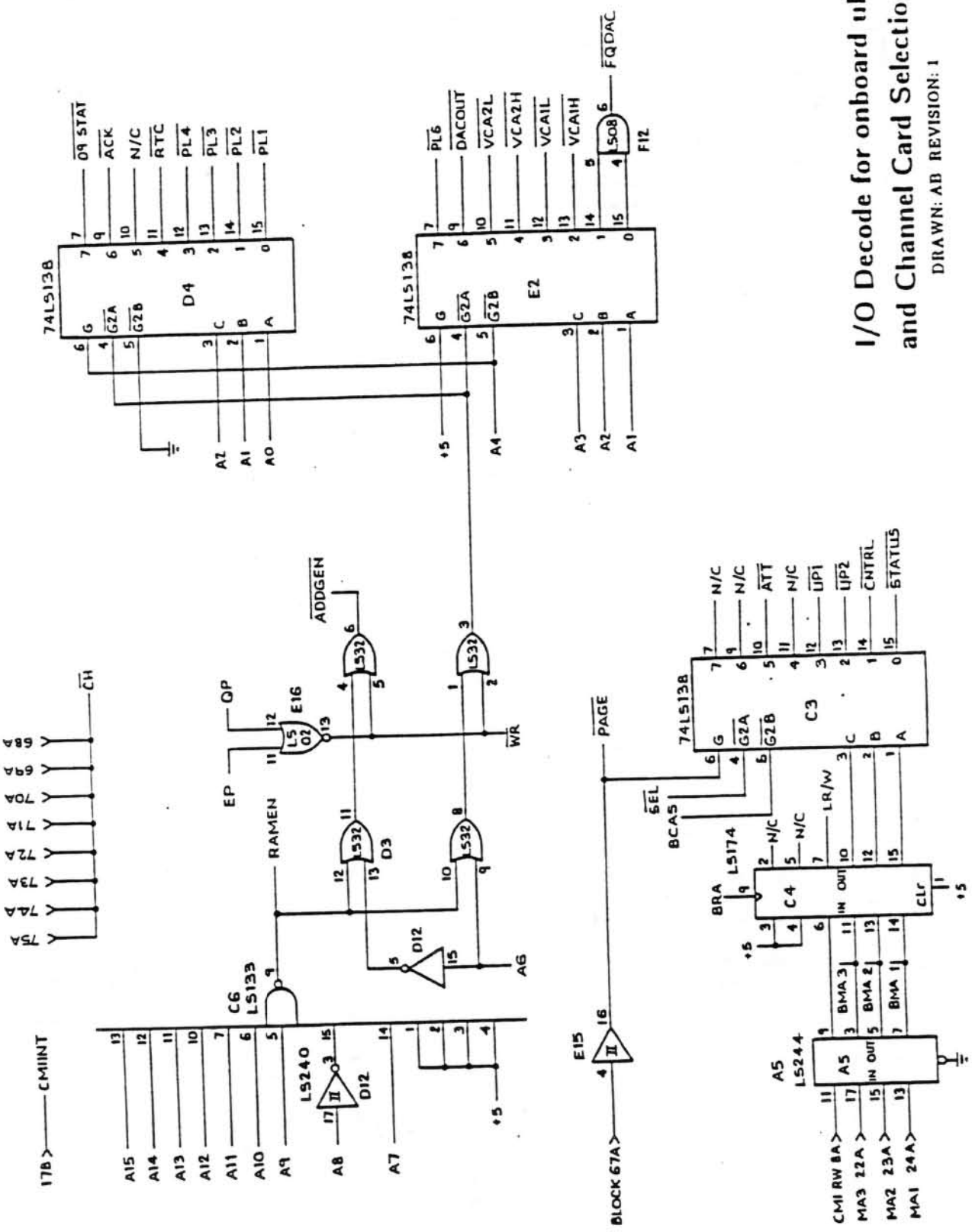
Communications Interrupts

```
COM   EQU   FE96  read or write to interrupt CMI

STAT  EQU   FE97  read for interrupt status
*     Bit definitions
*     4     chantick happened
*     5     end of loop B  interrupt happened
*     6     end of loop A  interrupt happened
*     7     command interrupt happened

RTC   EQU   FE94  access to reset real time FIRQ
```

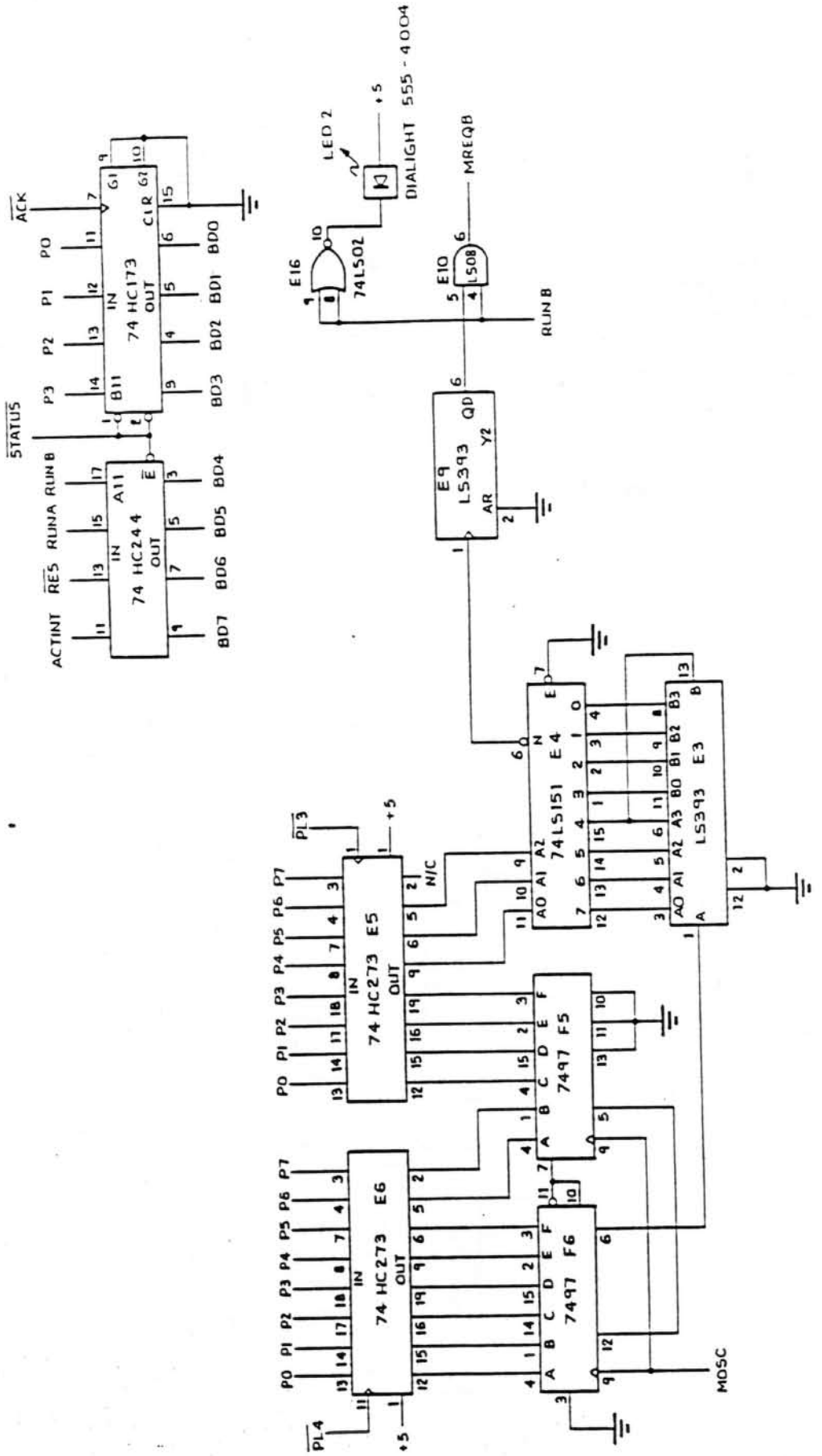
Address Generator 64 Byte RAM Organization.
Unlabeled locations are unused.

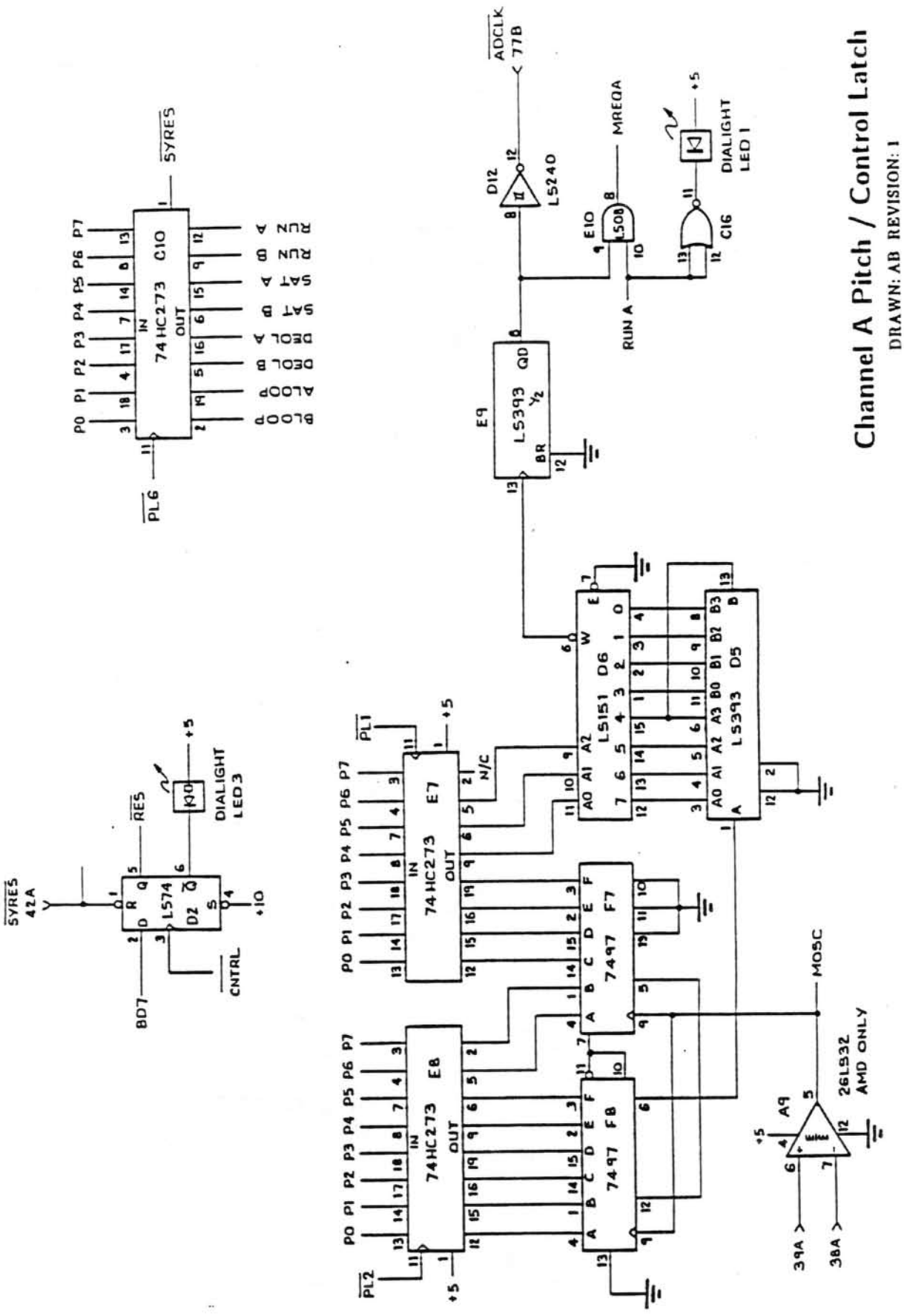
	Channel A		Channel B
0	start loop1 lsb	20	start loop1 lsb
1	" mb	21	" mb
2	" msb	22	" msb
3	loop length 1 lsb	23	loop length 1 lsb
4	" mb	24	" mb
5	" msb	25	" msb
6	word count 1 lsb	26	word count 1 lsb
7	" mb	27	" mb
8	" msb	28	" msb
9	waddress lsb	29	waddress lsb
A	" mb	2A	" mb
B	" msb	2B	" msb
C		2C	
D		2D	
E		2E	
F		2F	
10	start loop 2 lsb	30	start loop 2 lsb
11	" mb	31	" mb
12	" msb	32	" msb
13	loop length 2 lsb	33	loop length 2 lsb
14	" mb	34	" lsb
15	" msb	35	" msb
16		36	
17		37	
18		38	
19		39	
1A		3A	
1B		3B	
1C		3C	
1D		3D	
1E		3E	
1F		3F	

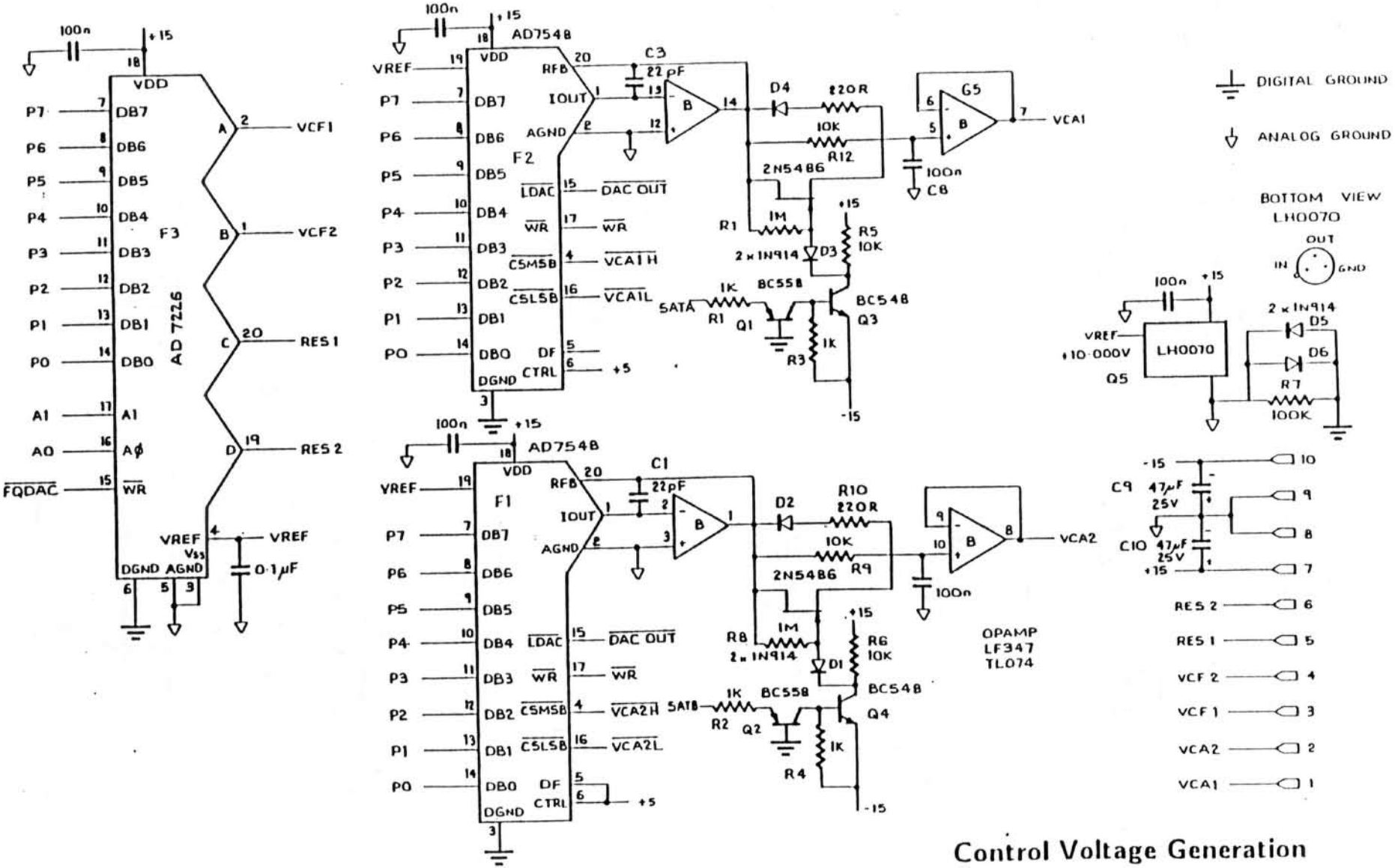

Processor, Data Buffers, and Pointer Registers
DRAWN: AB REVISION: 1
6809E CD 78
74LS374 A7
74LS374 A8
LS640 A6
LS245 B6
LS244 B7
LS244 B6
LS244 B5
LS532
LS00
LS08
LS240
LS244
4K7
680R
RAMEN
R/W
REFRESH 47B
DRAS 47A
RA 37A
CAS 34A


I/O Decode for onboard uP
and Channel Card Selection
DRAWN: AB REVISION: 1
74LS138
D4
E2
C3
C4
C6
A5
E15
E16
D3
D12
F12
LS240
LS133
LS174
LS244
LS32
LS08
09 STAT
ACK
N/C
RTC
PL4
PL3
PL2
PL1
PL6
DACOUT
VCA2L
VCA2H
VCA1L
VCA1H
FQDAC
ATT
CNTRL
STATUS
ADDGEN
PAGE
QP
EP
RAMEN
WR
CH
CMIINT
BRA
BCA5
SEL
LR/W
BMA3
BMA2
BMA1
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
+5
BLOCK 67A
CMI RW 8A
MA3 22A
MA2 23A
MA1 24A

fairlight

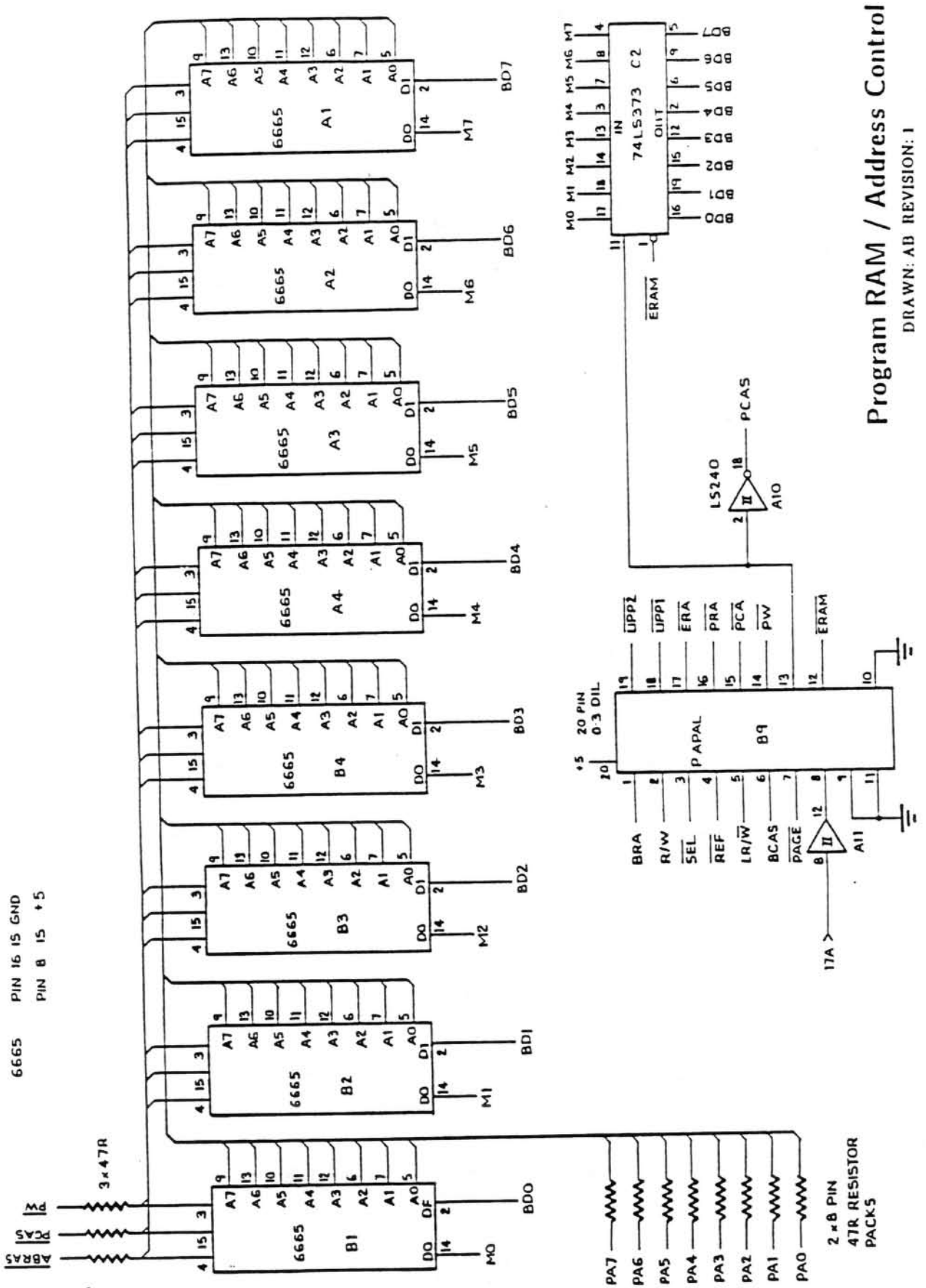

Channel B Pitch Generation
DRAWN: AB REVISION: 1
LED 2
DIALIGHT 555 - 4004
+5
MREQB
RUN B
E16
74LS02
E10
LS08
E9
LS393
QD
AR
Y2
ACK
STATUS
ACTINT
RES
RUNA
RUN B
74 HC244
A11
74 HC173
B11
OUT
CLR
P0
P1
P2
P3
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
74 HC273 E5
74 HC273 E6
74LS151 E4
LS393 E3
7497 F5
7497 F6
PL3
PL4
N/C
MOSC

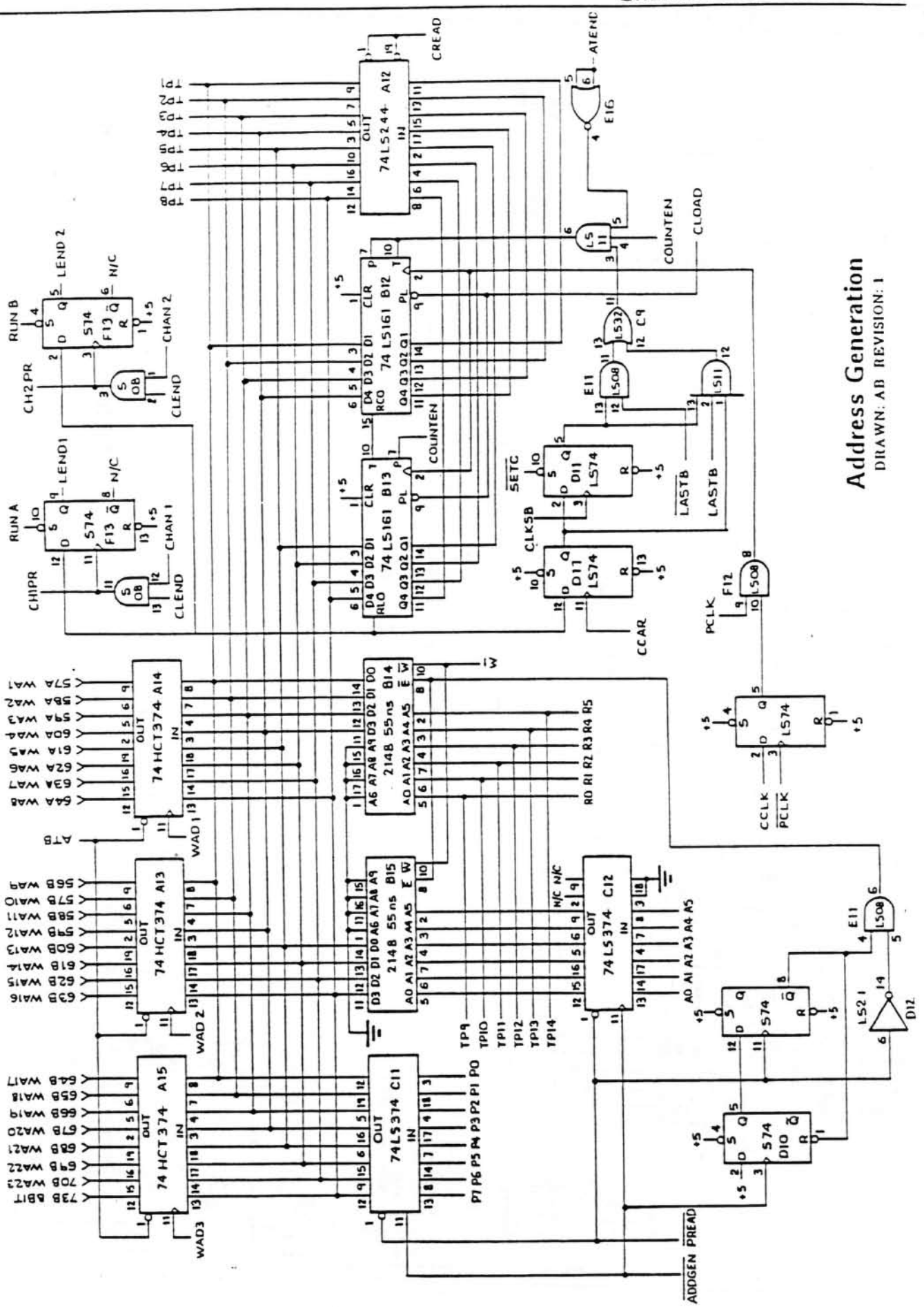

Channel A Pitch / Control Latch
DRAWN: AB REVISION: 1
SYRES
74HC273 C10
PL6
ADCLK 77B
D12 LS240
MREQA
RUN A
E10 LS08
C16
DIALIGHT LED 1
E9 LS393
LS151 D6
LS393 D5
74HC273 E7
74HC273 E8
7497 F7
7497 F8
PL1
PL2
N/C
MOSC
A9 26LS32 AMD ONLY
39A
38A
SYRES 42A
L574
RES
DIALIGHT LED3
CNTRL
BD7
+5
+10

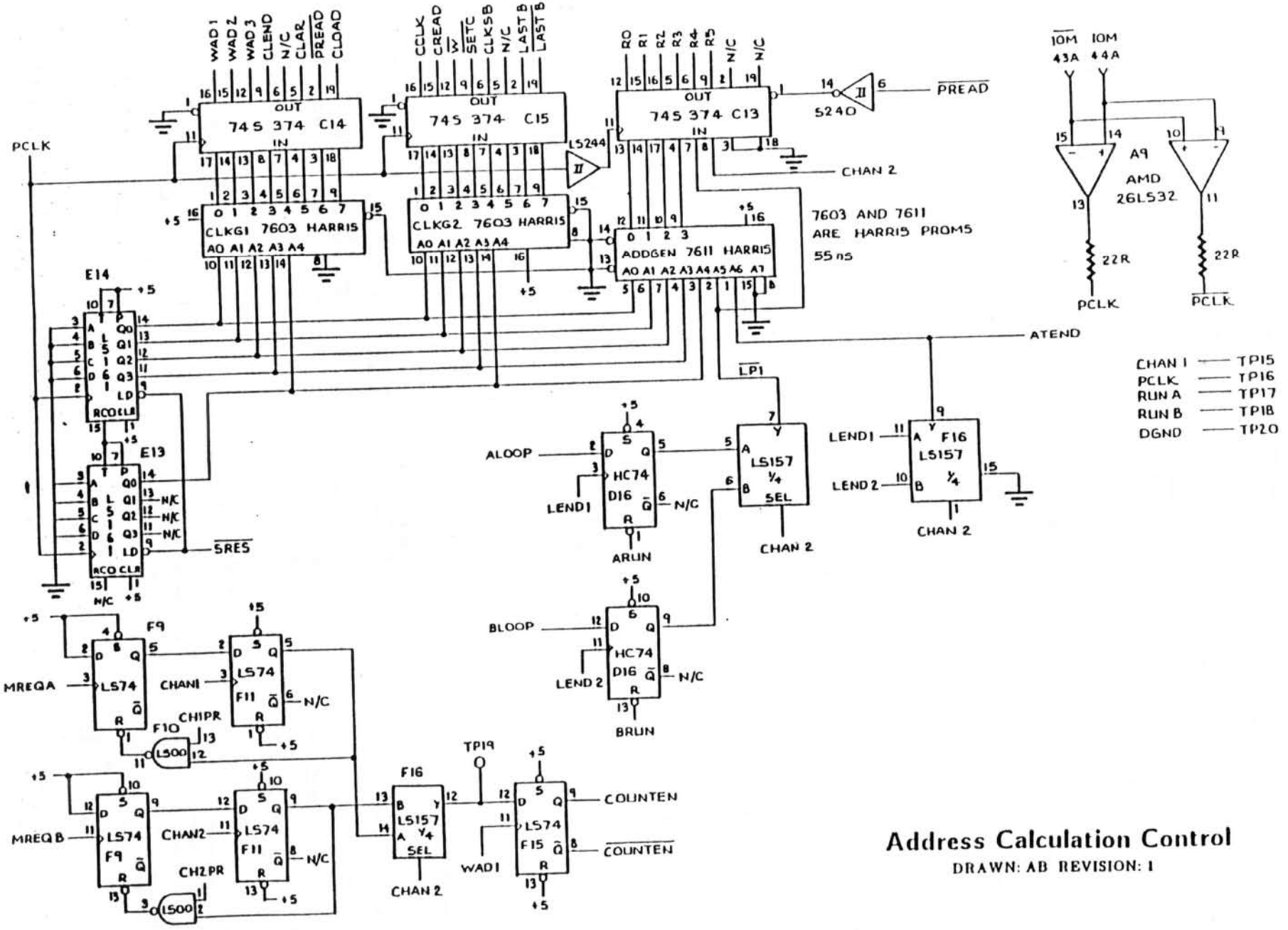


Control Voltage Generation

DRAWN: AB REVISION: 1

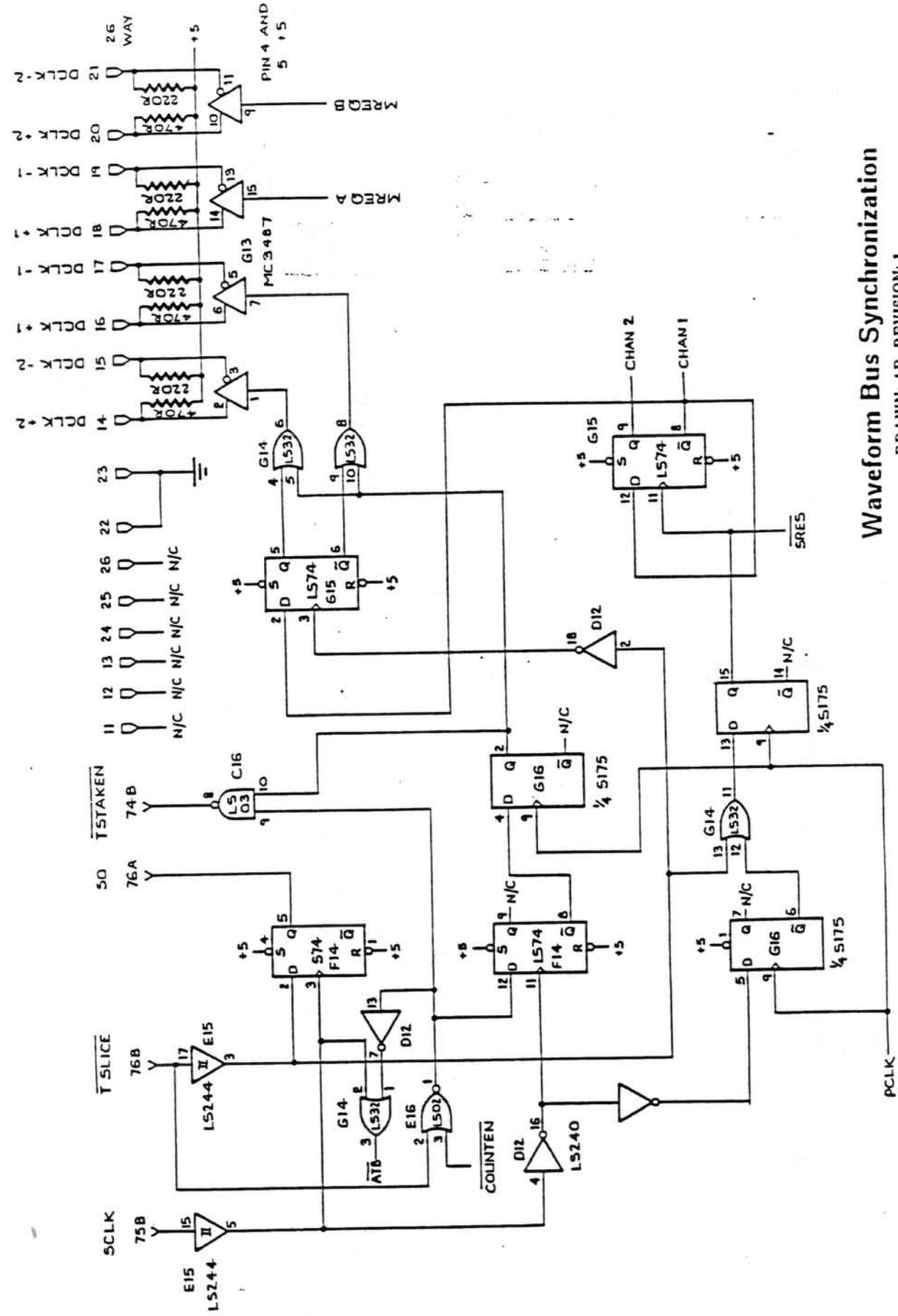

Program RAM / Address Control
DRAWN: AB REVISION: 1
6665 PIN 16 IS GND
PIN 8 IS +5
3x47R
2 x 8 PIN
47R RESISTOR
PACKS
20 PIN
0.3 DIL
P APAL
B9
B1
B2
B3
B4
A1
A2
A3
A4
74LS373 C2
LS240
ERAM
PCAS
A10
A11
17A
BRA
R/W
SEL
REF
LR/W
BCAS
PAGE
PA7
PA6
PA5
PA4
PA3
PA2
PA1
PA0
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0
M7
M6
M5
M4
M3
M2
M1
M0

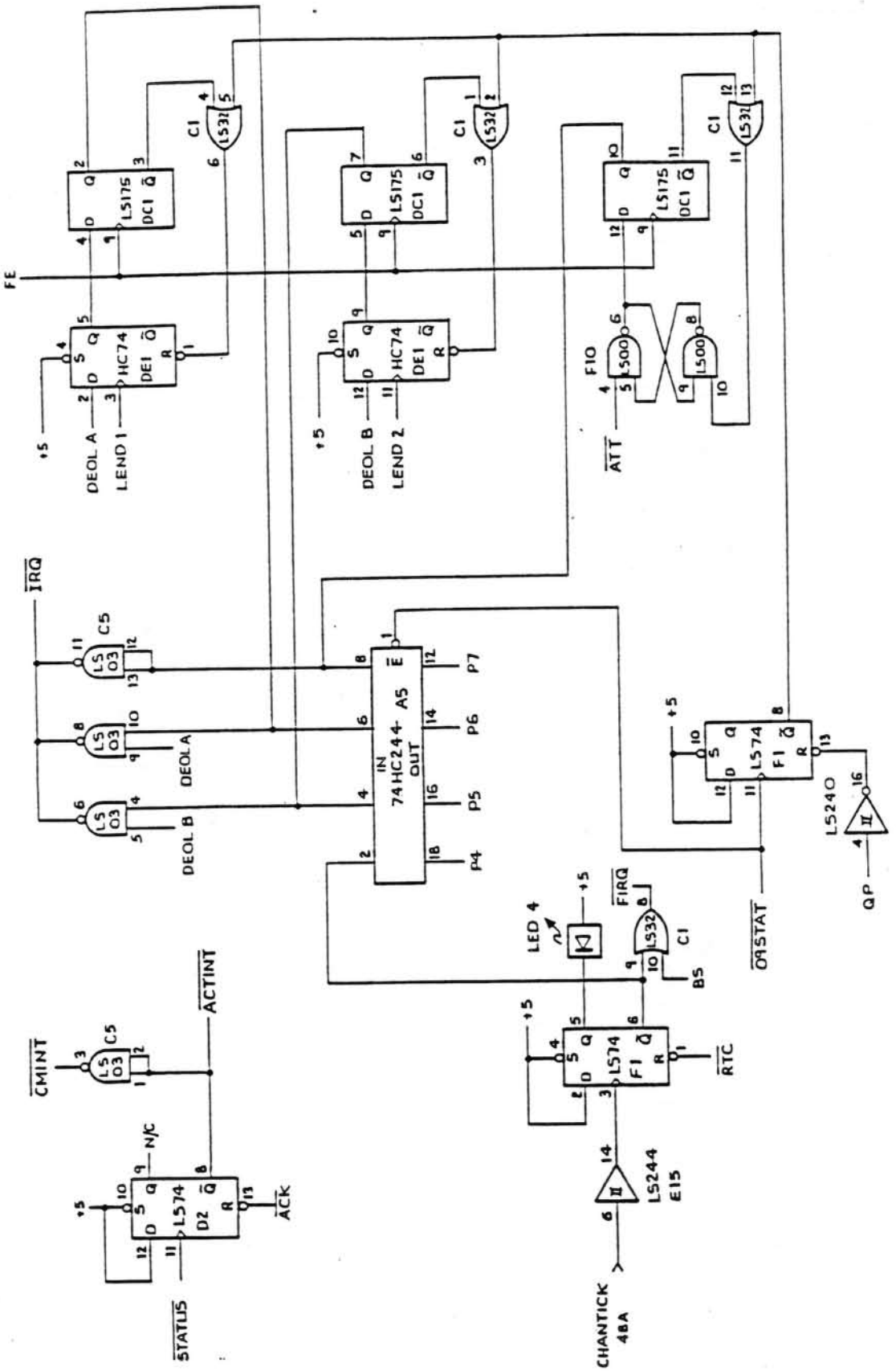

Address Generation
DRAWN: AB REVISION: 1
74 HCT 374 A14
74 HCT 374 A13
74 HCT 374 A15
74 L5374 C11
74 L5374 C12
74 L5244 A12
74 LS161 B13
74 LS161 B12
2148 55ns B14
2148 55ns B15
LS74
LS08
LS32
LS11
LS04
CHAN 1
CHAN 2
CLEND
CHIPR
CH2PR
RUN A
RUN B
LEND1
LEND2
N/C
CREAD
ATEND
COUNTEN
CLOAD
SETC
CLK5B
LASTB
CCAR
PCLK
CCLK
WAD1
WAD2
WAD3
ADDGEN
PREAD



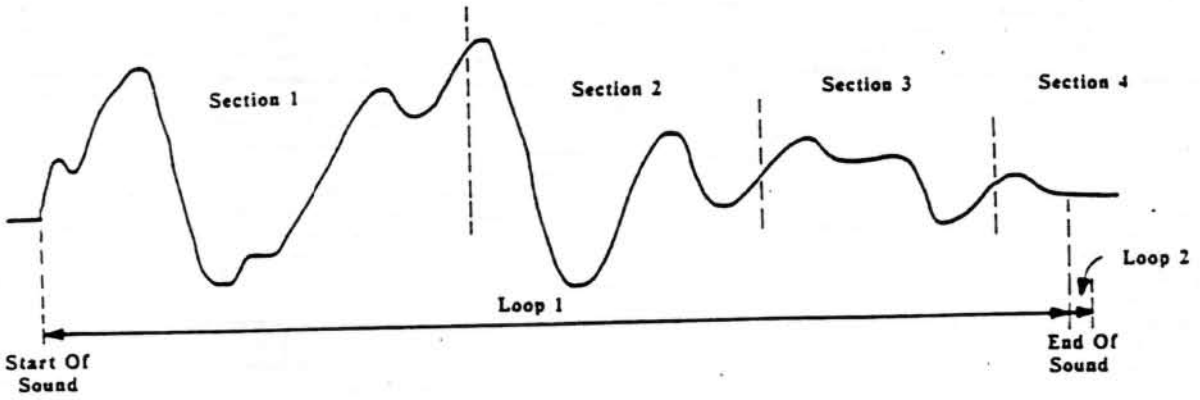
Address Calculation Control

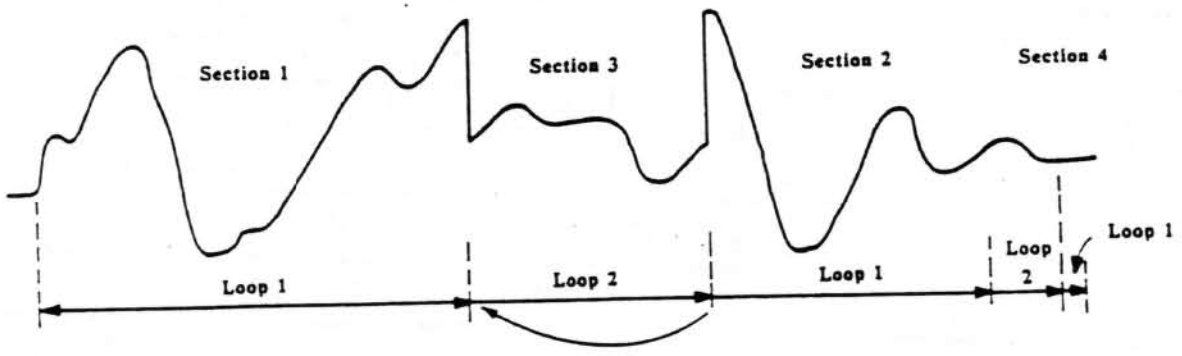
DRAWN: AB REVISION: 1

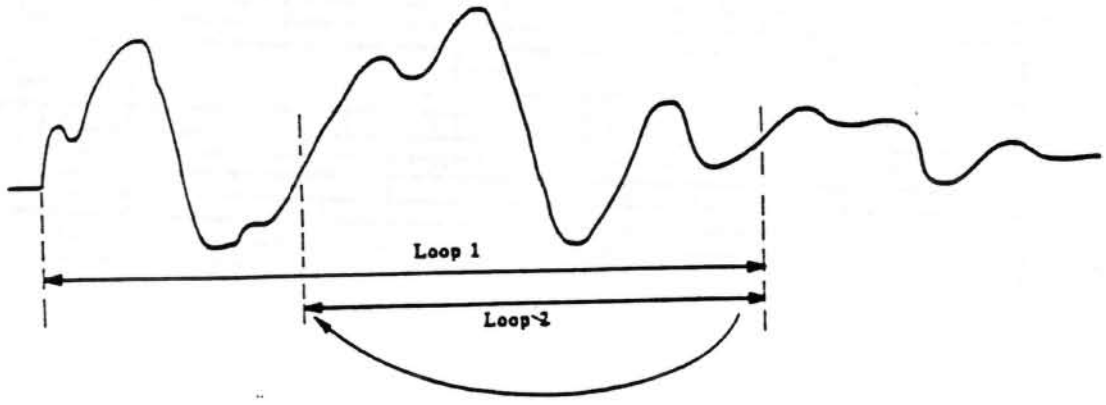

Waveform Bus Synchronization
DRAWN: AB REVISION: 1
26 WAY
PIN 4 AND 5 +5
DCLK -2
DCLK +2
DCLK -1
DCLK +1
220R
470R
G13
MC3487
G14
LS32
LS74
G15
G16
CHAN 2
CHAN 1
SRES
N/C
D12
LS175
LS03
C16
TSTAKEN
74B
76A
T SLICE
76B
E15
LS244
SCLK
75B
ATB
E16
LS01
COUNTEN
LS240
PCLK


Interrupts
DRAWN: AB REVISION: 1
FE
IRQ
DEOL A
LEND 1
DEOL B
LEND 2
ATT
DEOL A
DEOL B
P7
P6
P5
P4
LED 4
FIRQ
BS
OPSTAT
QP
L5240
RTC
CMINT
ACTINT
ACK
STATUS
CHANTICK
48A
LS244
E15
N/C

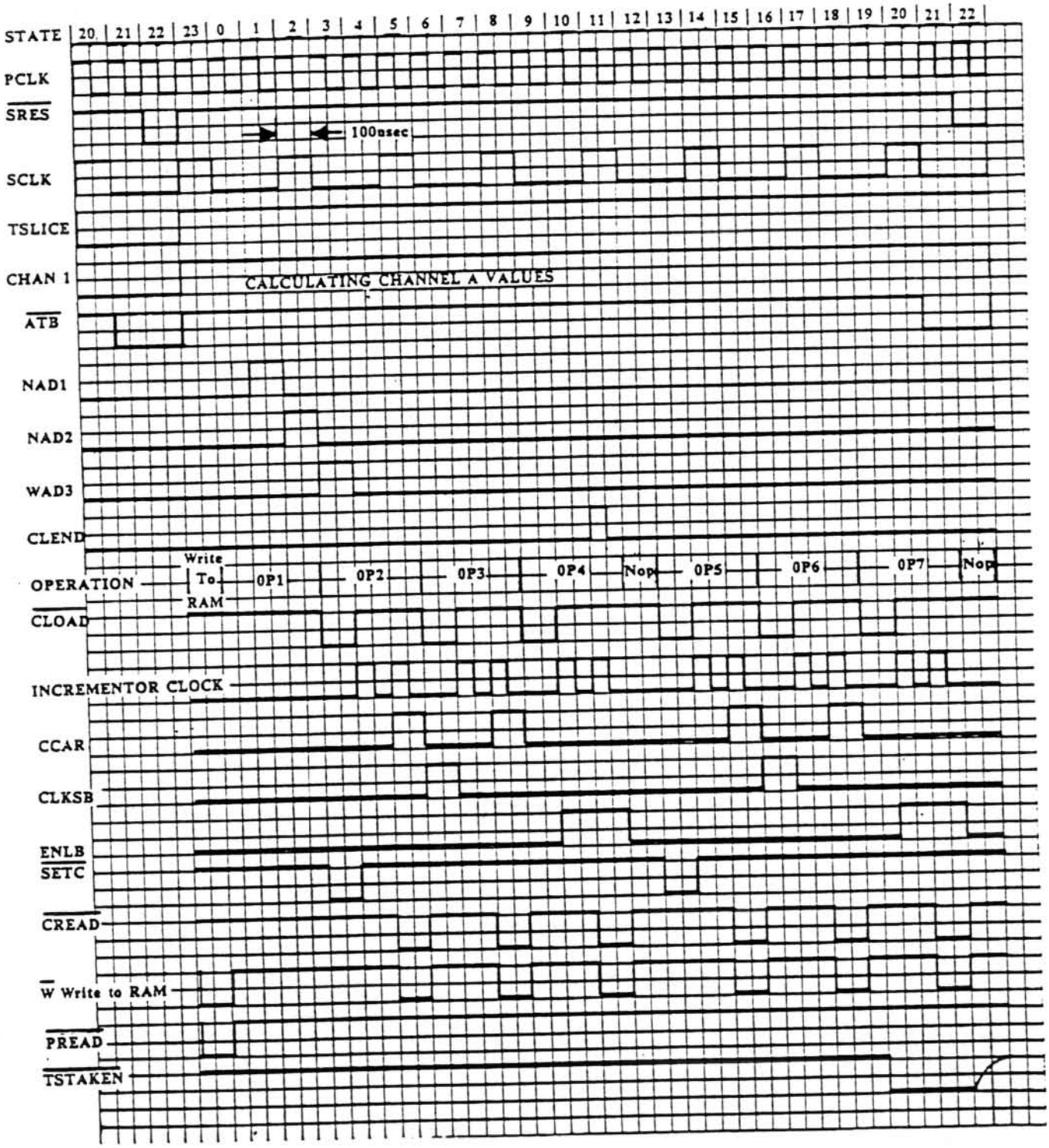
Address Generator Loops



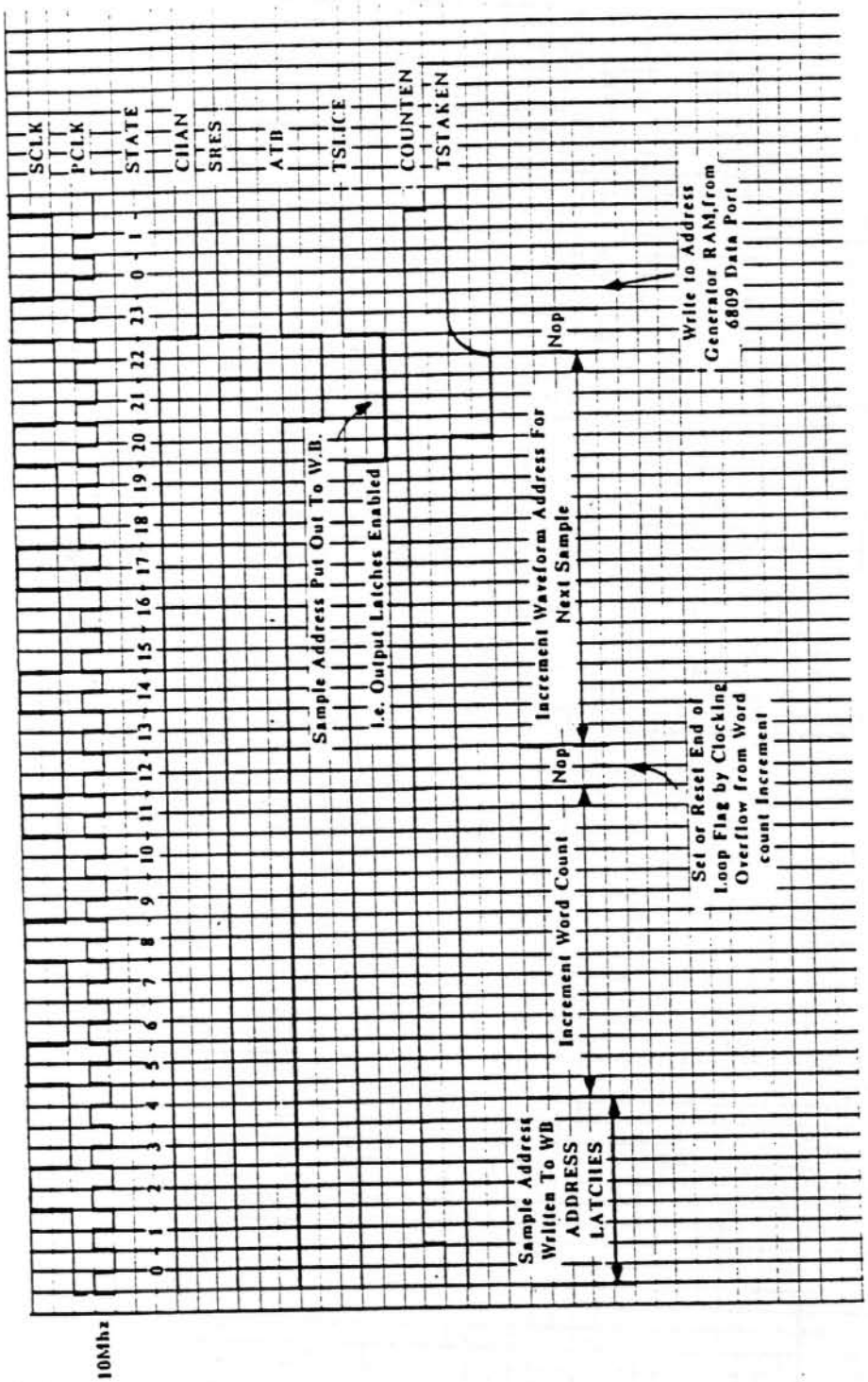


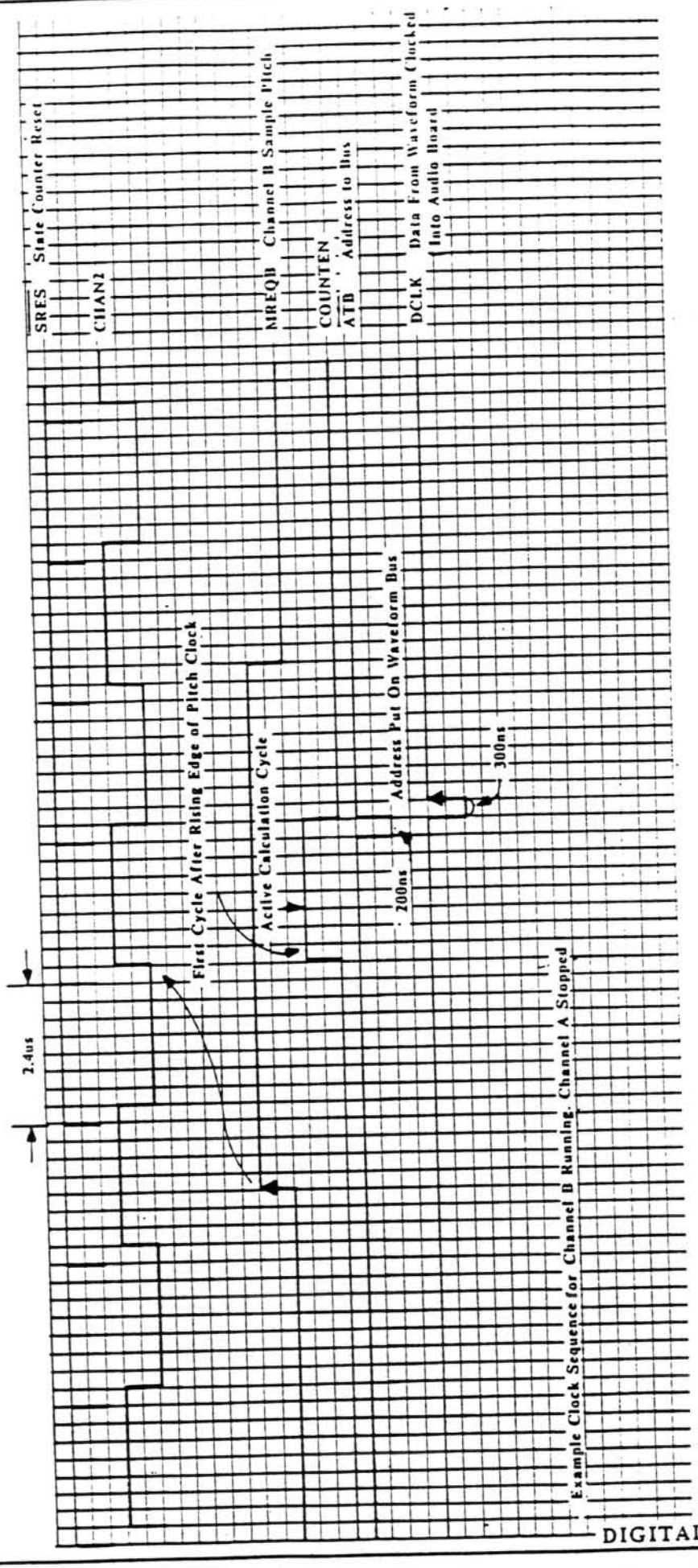


Address Generator Control Signals

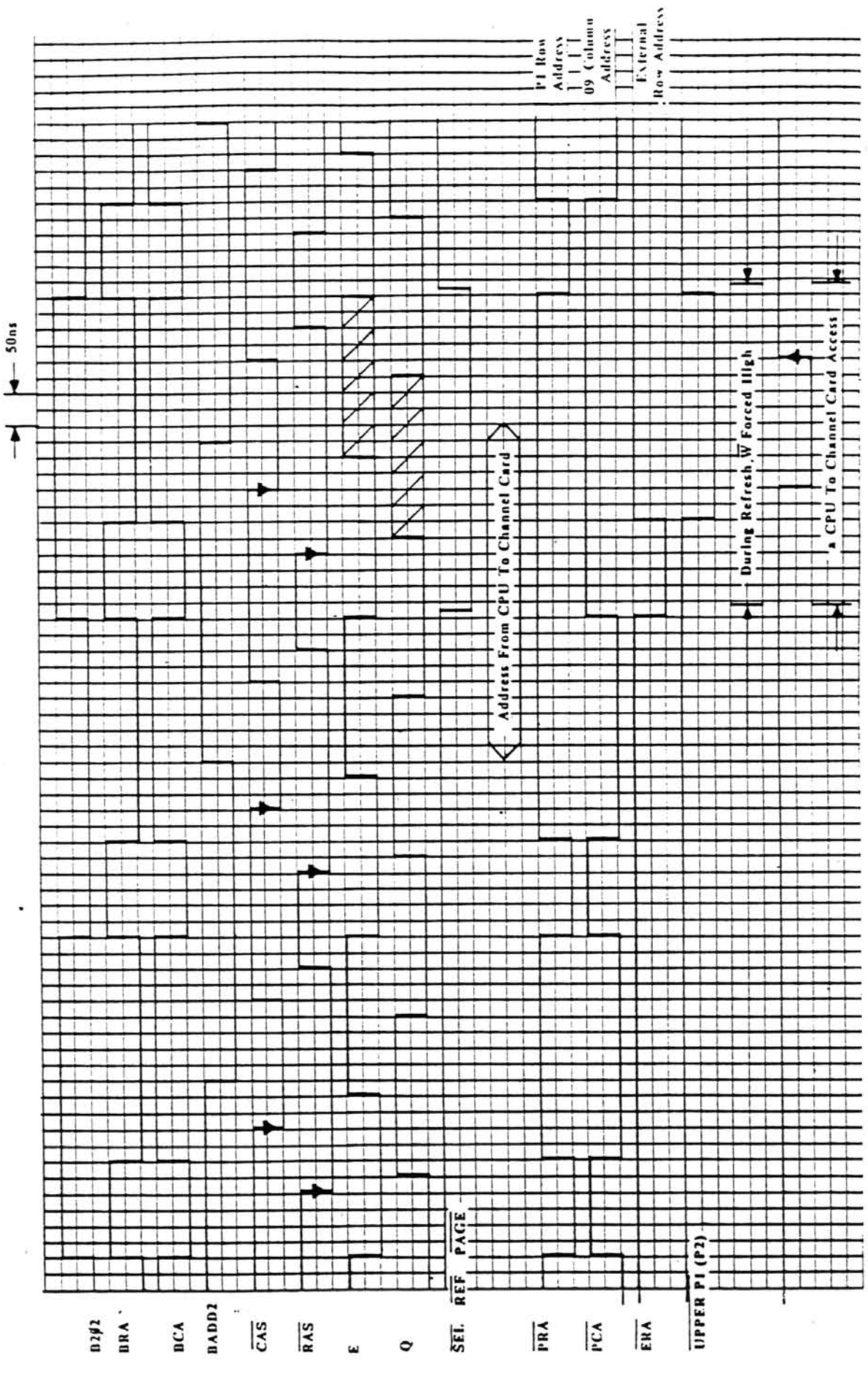


An active address generator cycle





The operation of count enable



CMI Bus Interface