

CMI-43D

8 MEG RAM





FIELD CHANGE NOTICE

DATE 3 / 5 / 93
NUMBER 126

ORIGINATOR John Gavin

PRODUCT: CMI / MFX

ASSEMBLY No. CMI-43D DESCRIPTION 8 MEG RAM CARD

This FCN applies to REV No: REV 1.0

New REV No is: REV 1.1

REASON FOR CHANGE:

To correctly document changes made to production boards. All REV 1.0 boards have the following modifications done at the time of manufacture.

DETAILS OF CHANGE:

1. Cut track from IC H7 pin 15 on solder side.
2. Link pin 13 to pin 15 on IC H7.
3. Cut track between pin 1 and pin 3 of IC ML 6 on solder side.
4. Cut track between pin 3 and pin 5 of IC ML 6 on solder side.
5. Connect pin 2 IC ML 6 to pin 4 IC GF 6.
6. Connect pin 1 IC R 7 to pin 4 IC ML 6.
7. Connect pin 4 IC R 7 to pin 3 IC ML 6.
8. Connect pin 6 IC R 7 to pin 1 IC ML 6.
9. Cut track to pin 6 IC R 7 on component side.

Relabel revision number to REV 1.1

ORIGINATOR: <i>JGavin</i>	DATE: <i>3/5/93</i>	TEST: <i>Markus Paulino 4/5/93</i>	DATE:
SERVICE:	DATE:	PROD: <i>4 gmm</i>	DATE: <i>3/5/93</i>
		KIT LIST CHANGE:	YES <input checked="" type="checkbox"/> NO

CMI-43 8Mb Waveform RAM Card

Manual Update

- 1. Functional Specification**
- 2. Installation Instructions**
- 3. Hardware Description**

1. Functional Specification

The CMI-43 8Mb Waveform RAM (WRAM) card is an alternative to the CMI-39 2Mb Waveform RAM card or the CMI-40 4Mb card in the Series III CMI. Doubling of the memory density per WRAM card has been achieved by use of the latest 1Mb memory chips, and has led to a total sound storage capacity of 56Mb per CMI rack unit arranged as 28Mwords by 16 bits across seven 8Mb cards. The Channel cards however, still only generate 24 bit addresses allowing them to access a maximum of 16Mwords or 32 Mb across only four cards. 32Mb provides a total sound storage capacity of more than 6 minutes at a 44.1kHz sampling rate. The additional cards above four, if installed, can only be used as auxiliary storage by the Waveform Supervisor, e.g. as a RAM disk for fast page changing.

Unnecessary hardware has been eliminated from the design by deleting the 8-bit mode of operation provided in the CMI-39 WRAM card, which has not proven to be a particularly useful feature and which is no longer supported in software.

CMI-43, CMI-40 CMI-39 cards may be mixed in the same system but care must be taken to follow the installation instructions with regard to card numbering to ensure that the system is configured with a single contiguous body of memory.

There are two versions of the CMI-43 card:⁽¹⁾ the CMI-43D card uses Dual-In-Line 1Mb memory Packages (DIPs), and the CMI-43Z uses Zig-Zag-In-Line Packages (ZIPs). This gives the greatest flexibility in parts procurement. The two cards are functionally identical and have the same logic design.

System Hardware and Software Versions

The Waveform Supervisor running Revision 7 CMI System software or higher must be installed to take advantage of the extra memory available. The CMI-43 WRAM card is compatible with Waveform Processor systems running earlier revisions of software (except for the 8-bit mode) but still a maximum of 14Mb total WRAM will be accessible. There is no point installing more than 2 CMI-43 cards in a Waveform Processor system.⁽²⁾

NOTES

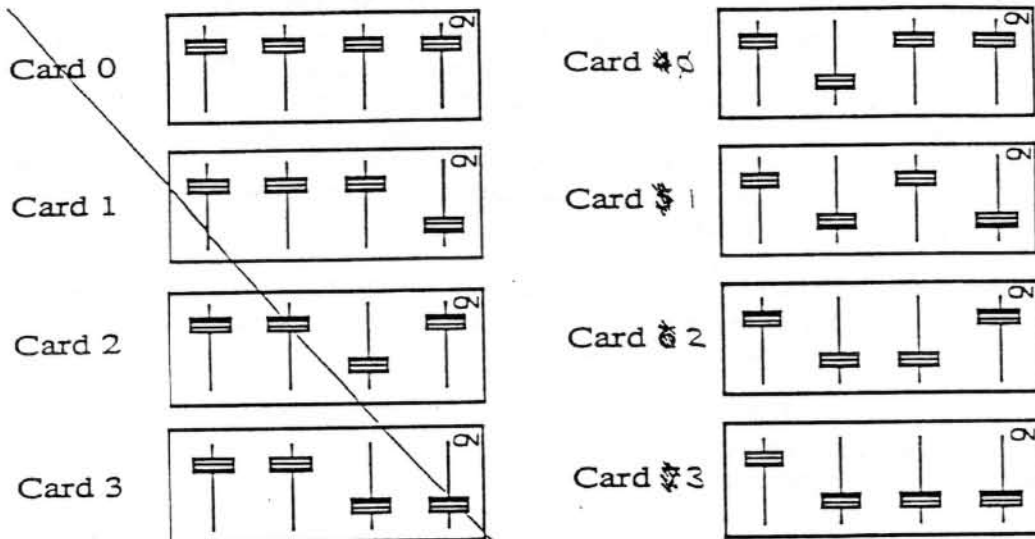
(1) CMI-43Z was never made

(2) Modifications on schematics allow installation in 32 M system

2. Installation Instructions

Card Numbering *(NCE setting has changed refer to RAM installation doc)*

A DIP-switch card numbering system is used to configure the 8Mb WRAM cards in the same manner as the CMI-39 and 40. The card number select DIP-switch is at location J6 on the Revision 1 card. To set appropriate card numbers, the DIP switches should be set as follows:



Notice that the switch setting can be considered as a 4-bit binary number, where a '1' is set by moving the switch to the "off" position.

Installation of 8Mb cards only in Waveform Supervisor Systems

Up to seven WRAM cards may be installed in a CMI system, usually numbered 0 through 6. If fewer cards are installed they should be numbered consecutively starting from card 0. WRAM cards may be installed in any order in the left most 7 card cage slots but for convenience a convention is adopted whereby Card 0 goes in slot 1, Card 1 in slot 2, etc.

Note: The leftmost DIP switch has no function.

Left most DIP switch must be on to use in 32Mb system

Installation of Mixed 2Mb, 4Mb and 8Mb Cards in Waveform Supervisor Systems

Users wishing to expand their waveform memory without discarding all 2Mb or 4Mb WRAM cards can do so by configuring the WRAM card number settings appropriately to achieve a contiguous physical memory. While the switch settings for a given card number are the same on both 2Mb, 4Mb, and 8Mb cards, the physical memory space occupied by that card number differs depending on whether it is a 2Mb or 4Mb card. Selecting card numbers to achieve a contiguous waveform memory configuration is thus akin to building a solid wall with different sizes of bricks. Also, it is not necessary to perform FCN 48 provided the 8-bit mode alias images of 2M cards 0-3 do not coincide with any 4M or 8M cards. It can be all terribly confusing but if you carefully follow the following configurations, all will be well:

Note: With 4 or more 8Mb cards, no 2Mb or 4Mb cards can be used.

Any slots left unused in the configurations below can be filled by 8Mb cards numbered from 4 upwards. The extra RAM thus provided will not increase the space available for sounds, but may be used by the Waveform Supervisor as extra data storage space.

8Mb cards mixed with 2Mb cards

Configuration 1: Up to 3 8Mb cards and up to 4 2Mb cards: Max 32Mb total

Slot 1:	8Mb card 0	
Slot 2:	8Mb card 1	
Slot 3:	8Mb card 2	
Slot 4:		2Mb card 4
Slot 5:		2Mb card 5
Slot 6:		2Mb card 6
Slot 7:		2Mb card 7.

If less than 3 8Mb cards: delete card 0 then card 1.
If less than 4 2Mb cards: delete card 7, 6, then 5 in that order.

Configuration 2: 2 8Mb cards and 5 2Mb cards: 26Mb total

Slot 1:	8Mb card 0	
Slot 2:	8Mb card 1	
Slot 3:		2Mb card 0
Slot 4:		2Mb card 1
Slot 5:		2Mb card 2
Slot 6:		2Mb card 3
Slot 7:		2Mb card 4.

Note: FCN 48 required on 2Mb cards 0-3. Since this implies non-equivalence between different WRAM cards, this configuration is undesirable.

Configuration 3: 1 8Mb card and 6 2Mb cards: 24Mb total

Slot 1:	8Mb card 0	
Slot 2:		2Mb card 0
Slot 3:		4Mb card 1
Slot 4:		2Mb card 2
Slot 5:		2Mb card 3
Slot 6:		2Mb card 4
Slot 7:		2Mb card 5.

Note: FCN 48 required on 2Mb cards 2 and 3. Since this implies non-equivalence between different WRAM cards, this configuration is undesirable.

8Mb cards mixed with 4Mb cards

Configuration 4: 1 8Mb card and up to 6 2Mb cards: 32Mb total

Slot 1:	8Mb card 0	
Slot 2:		4Mb card 2
Slot 3:		4Mb card 3
Slot 4:		4Mb card 4
Slot 5:		2Mb card 5
Slot 6:		2Mb card 6
Slot 7:		2Mb card 7.

Configuration 5: 2 4Mb cards and up to 4 2Mb cards: 32Mb total

Slot 1:	8Mb card 0	
Slot 2:	8Mb card 1	
Slot 3:		4Mb card 4
Slot 4:		4Mb card 5
Slot 5:		4Mb card 6
Slot 6:		2Mb card 7
Slot 7:	Unused	

Configuration 6: 3 8Mb cards and up to 2 4Mb cards: 32Mb total

Slot 1:	8Mb card 0	
Slot 2:	8Mb card 1	
Slot 3:	8Mb card 2	
Slot 4:		4Mb card 6
Slot 5:		4Mb card 7
Slot 6:	Unused	
Slot 7:	Unused	

Installation of 8Mb cards only in Waveform Processor Systems

Installation of Mixed 2Mb and 8Mb Cards in Waveform Processor Systems

Installation of Mixed 4Mb and 8Mb Cards in Waveform Processor Systems

3. Hardware Description

Introduction

The Waveform RAM (WRAM) provides the bulk memory required for storage of multi-sampled sounds, disc recorder buffering, fast page changing and any other purpose. It resides on a 24 bit address bus which is controlled by the Waveform Supervisor and Channel cards and the data path is 16 bits wide. When accessed by a Channel card, the data output from the WRAM is received not by the Channel card but the Channel Support card for transmission to the Audio Motherboard and eventually the DACs on the Audio Output modules. The only device which can write to the WRAM is the WS.

*** add WP/Channel card views of WRAM from CMI-39 manual *****

Timing Generation

(refer schematic CMI-43-01 and timing diagram)

All timing is generated from one bus signal SCLK, which originates from the Channel Support Card, and control signals from the Waveform Bus arbitration logic on the WS. The whole Waveform Bus is synchronised to SCLK, which has a 300nS period and a 1:3 duty cycle. On the CMI-43, SCLK is inverter buffered by an HCT14 and fed into a ten-tap, 25nS/tap digital delay line. Four delayed versions of SCLK are then combined in various ways to produce the waveforms required to drive the dynamic RAM array.

A valid access cycle is indicated by a low on either data strobes /WUDS or /WLDS. Previous WRAM designs used /BAS in addition to the data strobes; the Waveform Supervisor and the CMI-43 exploit this redundancy to expand the address range above 32Mb, with /BAS interpreted as simply another address line. The WS accesses the top half of memory by asserting either or both data strobes but leaving /BAS high. A refresh cycle is indicated by a low on /WREF (Waveform Refresh). In either case, /RAS (Row Address Strobe) is clocked on the rising edge of the 4th delay line tap (TAP4) and is cleared again by the next low on the 3rd tap. The 125nS /RAS pulse is driven through an AC244 buffer to the RAM array in four bank signals /RAS0 - /RAS3.

The WR/W line is buffered by HC244 and latched by the rising edge of tap 3. Since this flip-flop is not otherwise set or reset, the latched read/write line LR/W is updated every 300nS. [The WR/W bus signal from the Waveform Processor is 300nS long and the open collector line is pulled up fast by a 220R resistor. The WS uses a tri-state line pulled up by 270R which may not be fast enough to avoid spurious write cycles when channels read immediately after a WS write. The WR/W pulse from the WS has been shortened to 100nS to solve this problem.]

/RA and /CA are the Row and Column address drive lines which control the address multiplexer (CMI-43-02). While these two signals are essentially the inverse of each other, the gating as arranged ensures that they are as close as possible to non-overlapping to prevent contention on the multiplexed RAM address lines. Thus the Column address is enabled when both taps 4 and 5 are high and the Row address is enabled on the opposite condition.

CAS (Column Address Strobe) is a timing signal which is generated continuously and later qualified by the data strobes to produce the actual /CAS signals to the RAM array. It is 100nS long, from the rising edge of tap 7 to the falling of tap 3.

The Output Enable signal /OE drives the data bus output latches. The timing of the /OE pulse is that it is clocked out on the rising edge of tap 7 and cleared when tap 3 is high but tap 5 is low. This results in a 200nS output drive pulse during valid read cycles. If READ is low, the latch will be held clear across the clock edge so no outputs will be enabled.

Address Decoding

(refer schematic CMI-43--02)

Card selection is performed by the HC85, comparing its A-side inputs to the pattern set up on the B-side by the DIP switch to generate the Card Select signal CSEL. A high on either BUDS or BLDS indicates a valid access cycle and is compared to a high. /WAS is, as described above, used as an additional address line by the WS to extend the address range beyond 32Mb. Cards 0-3 correspond to /BAS low, and cards 4-7 correspond to /BAS high. The address lines WA24 (which used to be the /8bit mode line in the Waveform Processor days) and WA23 constitute the other two card select bits.

The CMI-43 card has been designed to be compatible with future 4Mb RAM chips by the provision of an option block before the 1-of-4 block decoding. The default linking is for 1Mb chips, using /BA22 and /BA21 as the block select lines /BLK1 and /BLK0. If 4Mb chips are installed, /BA24 and /BA23 are used instead as block selects. Also, in the 4Mb case, the least significant DIP switches must be left open and links between pins 12 and 11, and 10 and 9 installed on the HC85. This makes /BAS the only card-select address line since each card is then 32Mb.

The block select lines /BLK0 and /BLK1 are latched by SCLKD125 (tap 5) rising edge, and decoded by HC139s to select one of four physical RAM blocks. The enabling of the decoders is qualified by the latched card select signal LCSEL, the latched upper and lower data strobes BUDS and BLDS respectively and the CAS signal, which controls the timing of the actual /CAS strobes to the RAM chips. BUDS and BLDS facilitate single byte accesses to the WRAM which is required if the WS wishes to run code in the WRAM. Indicator LEDs are provided driven by the latched card select signal and each of the four block select lines.

One upper and/or lower /CAS strobe are generated by active decoder outputs. A refresh cycle generates /CAS strobes to all blocks simultaneously through the HC00 gates at the outputs of the decoders. /BWREF is 300nS long, clocked out by the WS on the falling edge of SCLK. This results in a /CAS-before-/RAS refresh cycle, exploiting the on-chip refresh counters of the dynamic RAMs. Previous versions of the 2Mb and 4Mb WRAM card did not use /CAS-before-/RAS refresh but relied on an on-card refresh counter and /RAS-only refresh.

Address Multiplexer

(Refer schematic CMI-43-03)

The row address, constituted by WA1-WA10 plus WA21, is driven directly on to the RAM multiplexed address lines A0-A10 through an AC240 buffer and overshoot-limiting resistors during the low phase of /RA.

The channel cards only assert their addresses for 200nS which does not provide sufficient hold time after the /CAS strobe, so the column address must be latched. The column address is constituted by WA11-WA20 and WA22. The bottom 8 bits are latched and driven out to the RAMS by the transparent latch AC373 to maximise setup time, /WA19 and /WA20 are latched by two spare bits of the decoding HC374 (see CMI-43-02) and /WA22 is latched by a spare HC74 flip-flop.

The assignment of WA21 to the row address msb and WA22 to the column address msb is to enable compatibility between 1Mb and 4Mb RAMs without shuffling address lines. These bits multiplex to the A10 line which is ignored in the 1Mb case but WA21 and WA22 are then used as block selects instead.

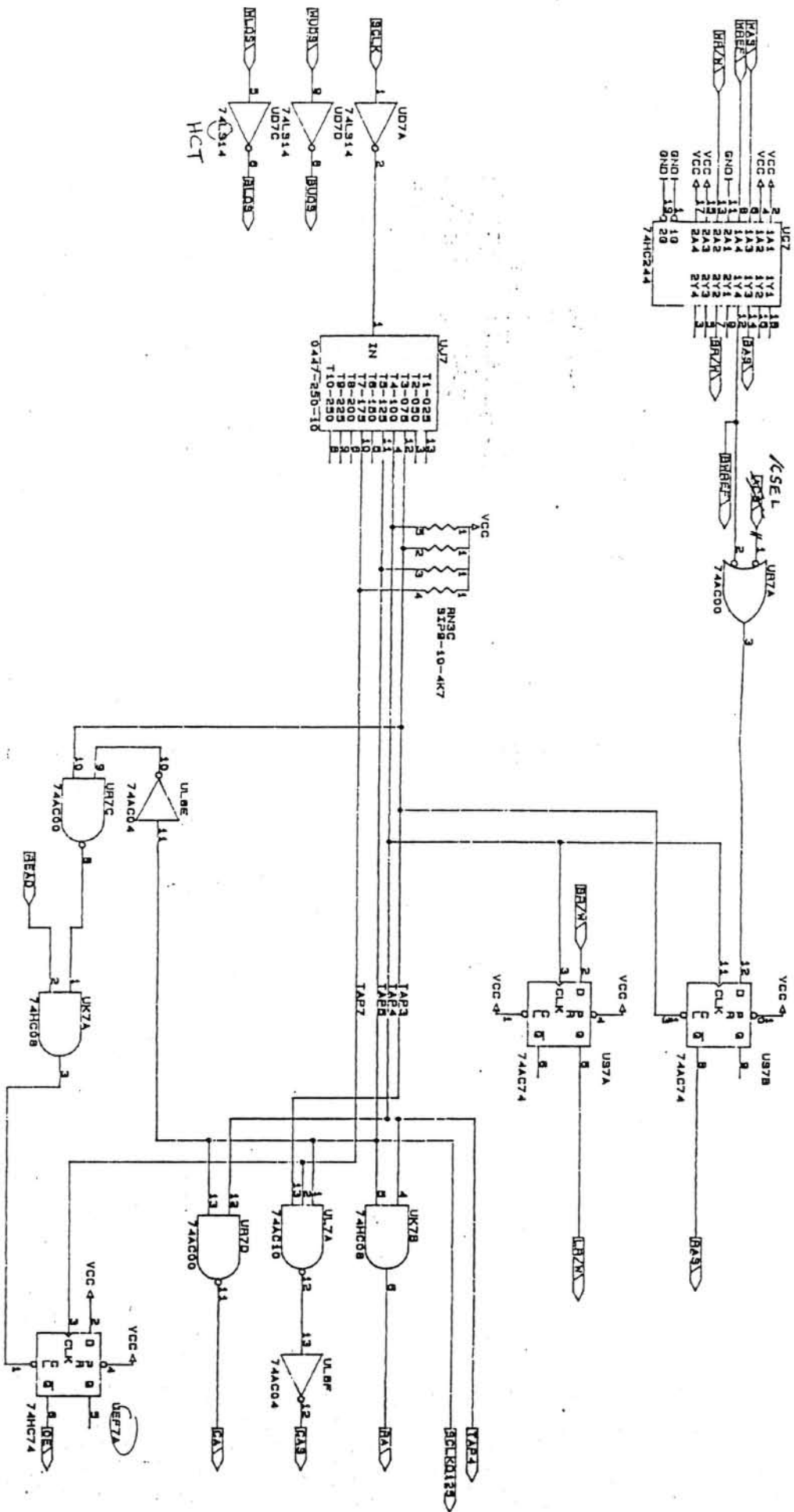
Data Bus Interface

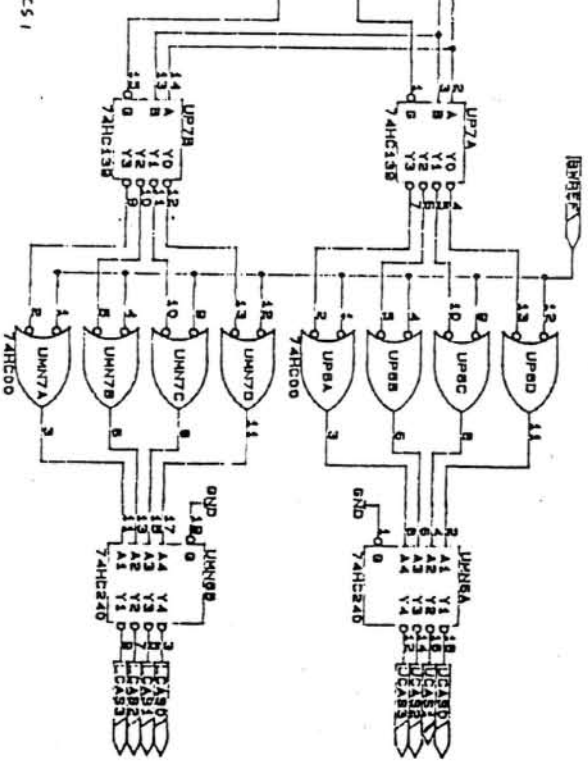
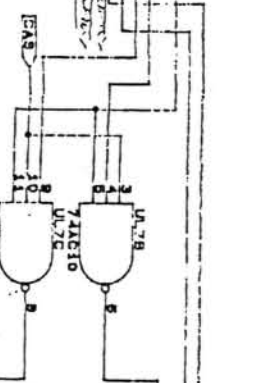
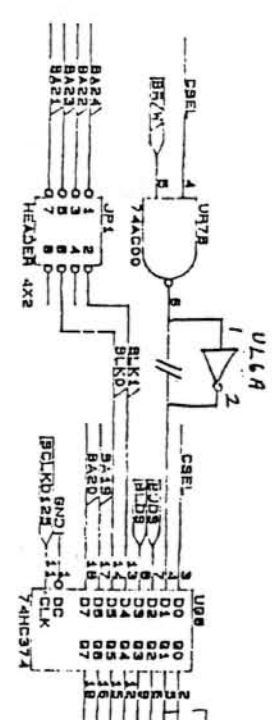
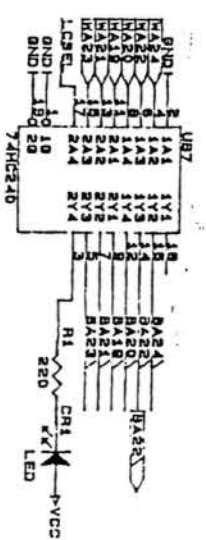
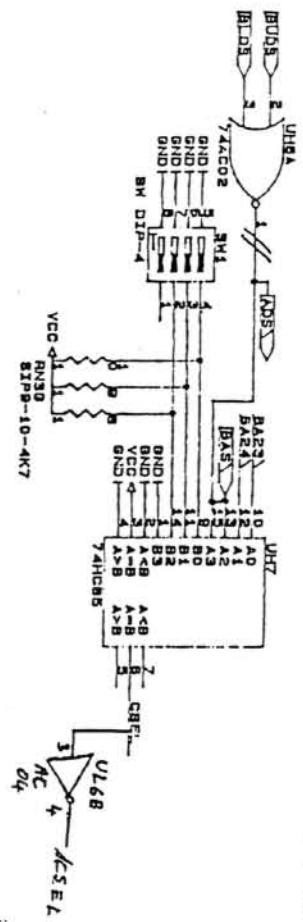
(Refer schematic CMI-43-04)

During read cycles the data from the RAM appears on lines Q0 to Q15 and is driven onto the waveform data bus by /OE for 200nS. The data is retained by the transparent latches on the falling edge of tap 4.

Data from the waveform bus is permanently enabled onto the D inputs of the RAM chips through HC244 buffers.

The latched write strobe LR/W and /RAS are each buffered into four drive signals, one for each RAM block and driven through current limiting resistors.



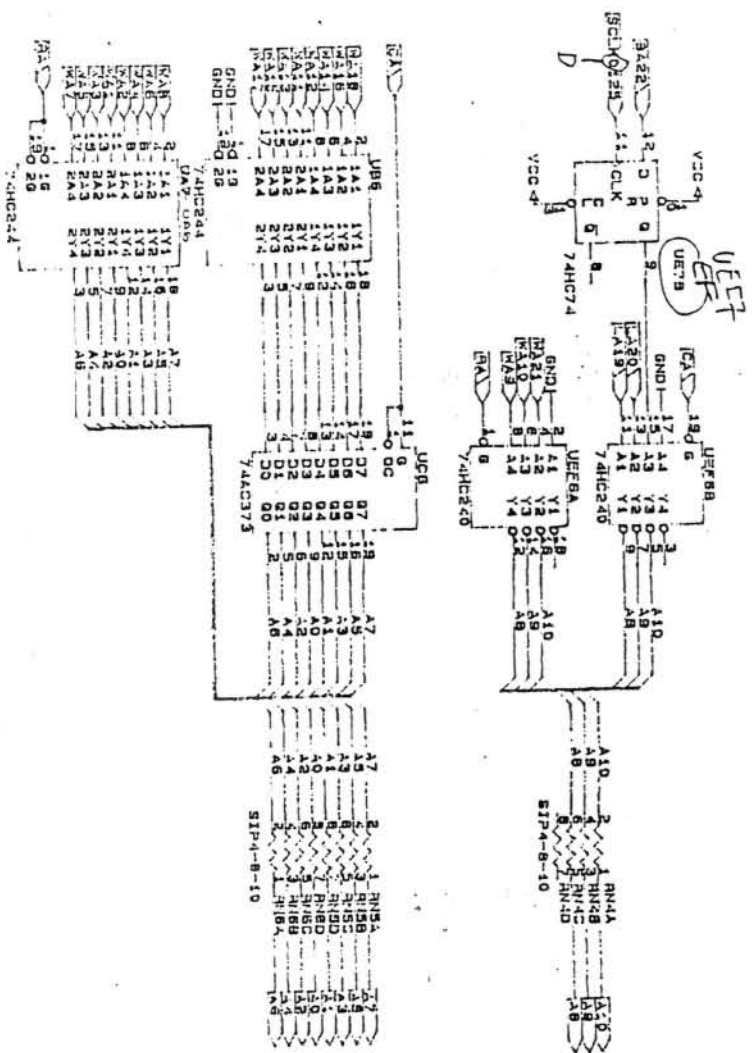


REV 1.1 Mods. (1) U16B inverted to correct logic error.

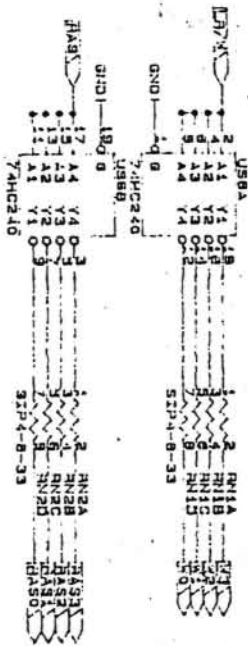
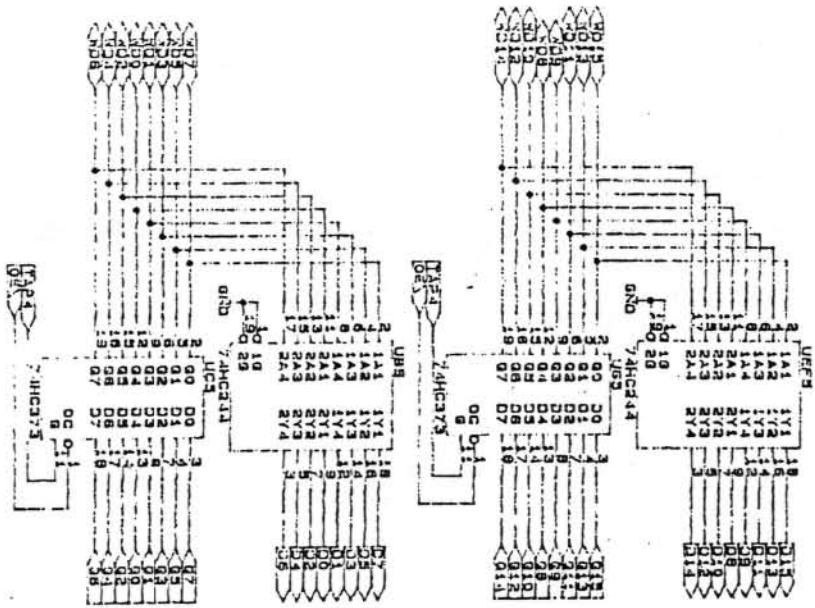
(2) $\overline{B\bar{A}S}$ used as address strobe instead of $\overline{BUD5} + \overline{BUD6}$ (i.e. revert to 2M/4M system). Cannot use $\overline{LD5}$, $\overline{UD5}$ since these are generated too late during 68k write cycles. This prevents use of RAM above 32Mk.

(3) $\overline{LCS\bar{E}L}$ used to generate \overline{RBS} instead of $\overline{B\bar{A}S}$ to fix "noise" problem. (Slot 1)

- D.C. 13/5/89.



FAIRLIGHT INSTRUMENTS
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 NAVFORD HAN 4M KORD
 Site Casson's Number 800KCS
 REV 11



PAIR LIGHT INSTRUMENTS

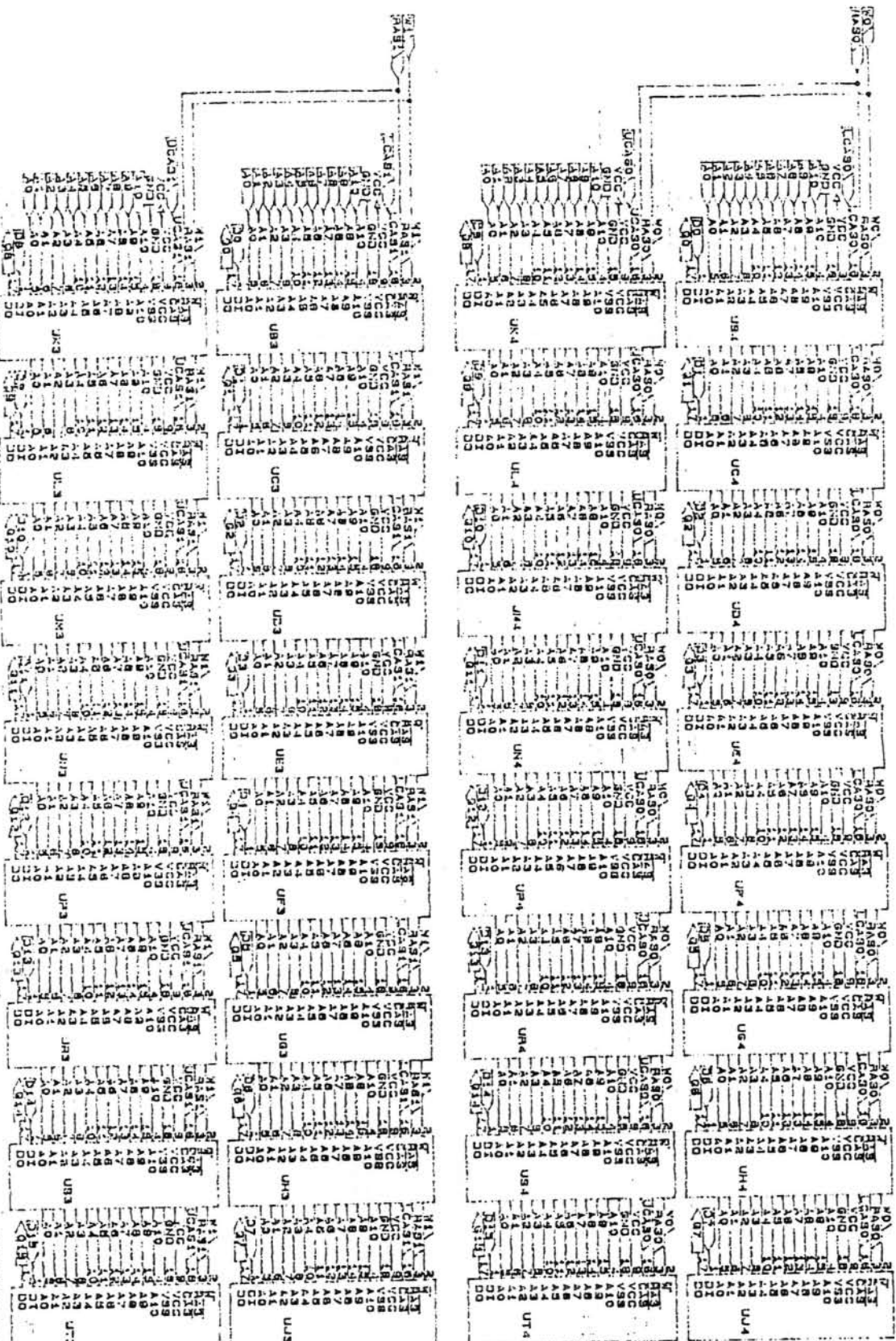
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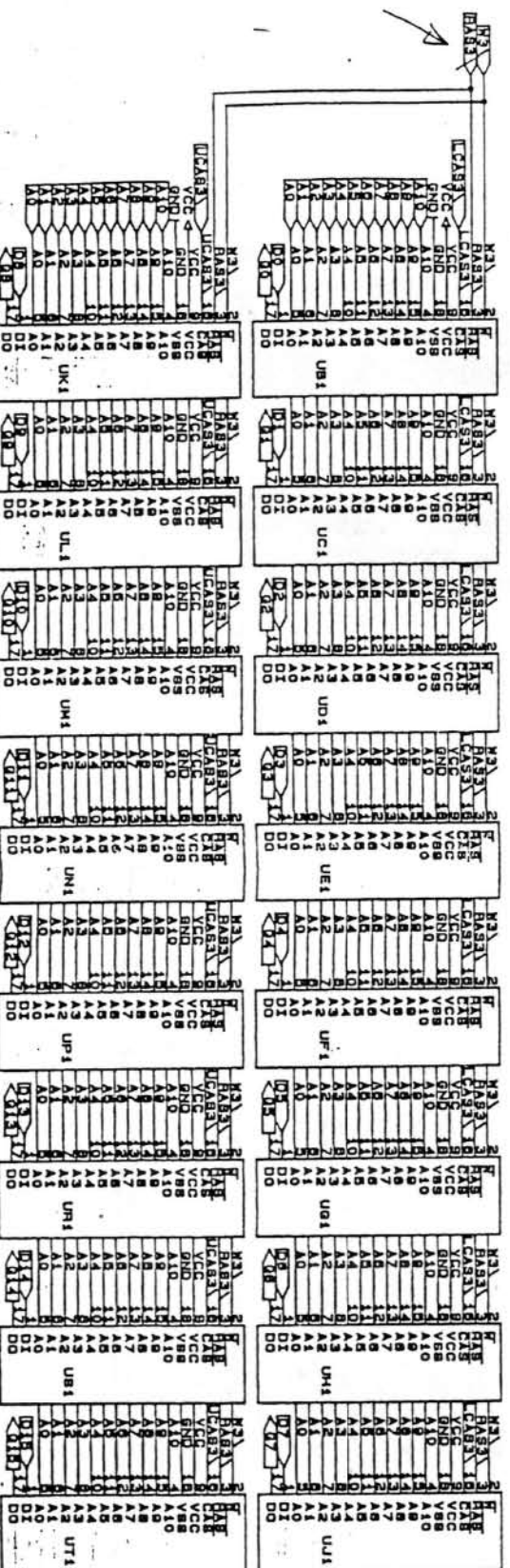
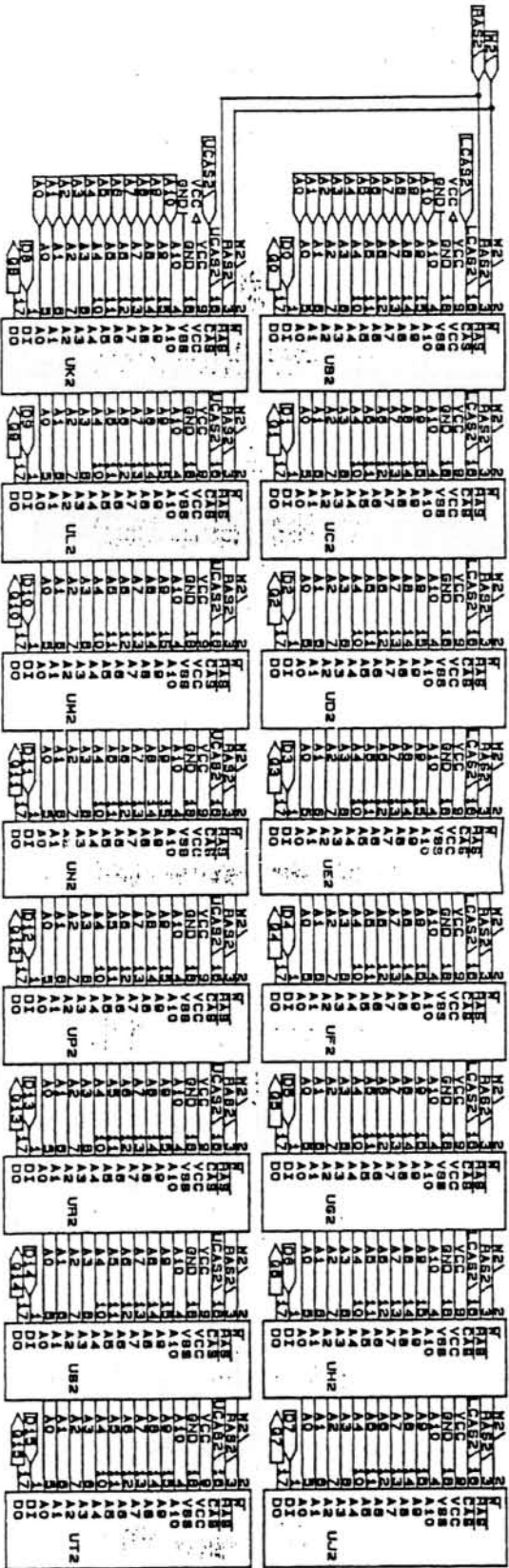
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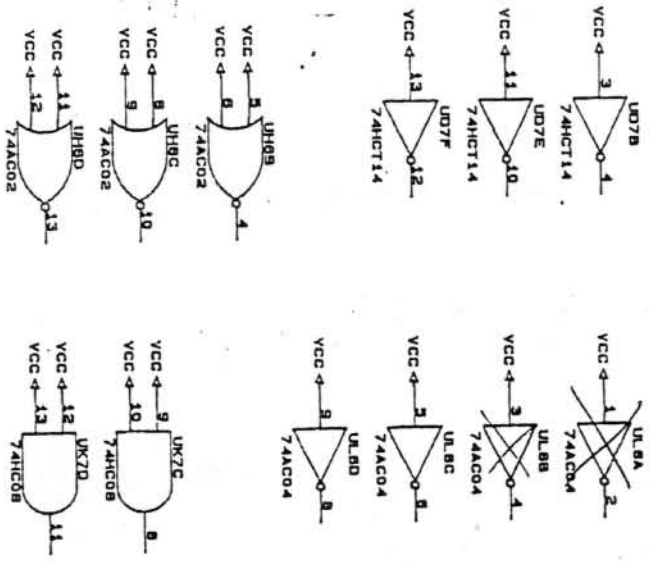
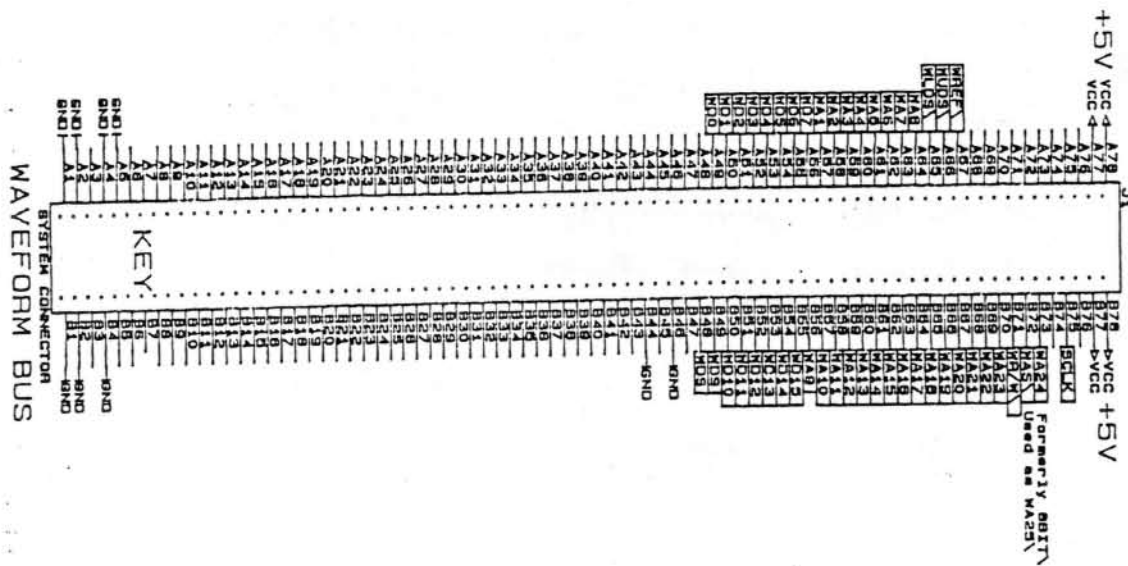
CNT-43 INT OFFICE

REV



AIRMAIL INSTRUMENTS
 TITLE
 DYNAMIC RANGE - KAYE/CPM RAN AN XORD
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 CH1-43





SYSTEM CONNECTOR
WAVEFORM BUS