CMI-39

2 MEG RAM

ESP

FIELD CHANGE NOTICE

Field Change Notice No 79

PRODUCT CMI [X] CVI [ ]

ORIGINATOR: Chris Alfred **DATE:** 28 / 8 / 90

ASSEMBLY No: CMI-39

DESCRIPTION: 2 Meg RAM card

This FCN applies to rev No: 4.4 **The New rev No is:** 4.5

REASONS FOR CHANGE:

Latching of *BRW at SCLKD75 did not allow adequte setup time causing data to be lost.
*BRW is now latched 25nS later at SCLKD100.

DETAILS OF CHANGE:

1. Carefully cut and lift out pin 3 of IcA4 (74ALS74).
2. Connect lifted IcA4 pin 3 to ICA9 (74ALS00) pin 5.

DEPT	SIGNATURE	DATE	COMMENTS
Project Manager			
Customer Service			

ESP

FIELD CHANGE NOTICE

Field Change Notice No 70

PRODUCT CMI [X] CVI [ ]

ORIGINATOR: Chris Alfred **DATE:** 17 / 6 / 91

ASSEMBLY No: CMI-39

DESCRIPTION: 2 Meg Ram Card

This FCN applies to rev No: 4.3 **The New rev No is:** 4.4

REASONS FOR CHANGE:
Corruption of DRAM address

The CMI-39 2Meg RAM cards latch the column address at the same time as the addresses to the DRAMs are changed. This can cause glitches caused by the multiplexing of addresses on the column address to be latched to the DRAM address lines.

DETAILS OF CHANGE:

Cut wiring side track to ICB13/11 (74HC373) at the pin.
Connect ICB13/11 to ICA6/6 (25nS delay line).

DEPT	SIGNATURE	DATE	COMMENTS
Project Manager	C E. Alfred	22/8/91	
Customer Service	M. Pardini	22/8/91	

ESP

FIELD CHANGE NOTICE

Field Change Notice No: 69

PRODUCT CMI [X] CVI [ ]

ORIGINATOR: Chris Alfred **DATE:** 17 / 6 / 91

ASSEMBLY No: CMI-39

DESCRIPTION: 2 Meg Ram Card

This FCN applies to rev No: 4.2 **The New rev No is:** 4.3

REASONS FOR CHANGE:

1. Corruption while Channel Cards running

When the channel cards assert their address onto the Waveform Buss, glitches are induced onto the *WUDS and *WLDS signals. These glitches are propagated to the CAS signals on the DRAMs. This modification latches *WUDS and *WLDS (similar to the 4Meg and 8Meg cards) so no glitches appear on CAS.

DETAILS OF CHANGE:

Cut wiring side track to Ic A5/2 (74ALS00) at the pin.
Cut wiring side track to Ic A5/12 (74ALS00) at the pin.
Bend out all pins except 1,8,9,16 on a 74LS175.
Piggy back the 74LS175 onto Ic B3 (74LS174) soldering pins 1,8,9,16 of 74LS175 to pins 1,8,9,16 of ICB3 respecively.
Connect 74LS175/5 to Ic A10/10 (74LS14).
Connect 74LS175/7 to Ic A5/2 (74ALS00).
Connect 74LS175/12 to Ic A10/8 (74LS14).
Connect 74LS175/10 to Ic A5/12 (74ALS00).

DEPT	SIGNATURE	DATE	COMMENTS
Project Manager	C L Alfred	22/8/91	
Customer Service	H. Paglini	22/8/91	

Introduction

The Waveform RAM (WRAM) provides the bulk fast memory required for storage of multi-sampled sounds, although it may be used for any purpose. It resides on a 24 bit address buss which is controlled by the Waveform Processor (WP) and Channel cards and the data path is 16 bits wide. When accessed by a Channel card, the data ouput from the WRAM is received not by the Channel card but the Channel Support Card, for transmission to the audio board DACs. Currently the only device which can write to the WRAM is the WP.

Memory Configuration

Each card contains 2M bytes of RAM using 256K x 1 bit chips. Up to and including Revision 2, 64K chips were supported using a PC link block to adjust the memory configuration and yielding 512K bytes per card. Revision 3 and above only accommodate 256K bit chips. Up to seven cards may be installed in the Series III motherboard, DIP-switched to different address ranges. 7 cards containing 256K chips will provide 14M bytes of RAM, filling the available address space (the bottom 2M is used by internal decoding on the WP).

The WP and Channel cards differ slightly in their respective "views" of WRAM:

Channel Card - generates the upper 23 address lines plus the mode bit. The bottom address line A0 does not exist physically but is constituted by the two buss lines Upper and Lower Data Strobes (UDS, LDS). When a Channel accesses WRAM the WP buss arbitration logic automatically asserts both strobes, since all channel accesses yield 16-bit outputs.

WP - also generates 23 address lines and the mode bit, plus either or both of UDS and LDS according to whether a byte or word access is required by the 68000. The operation of UDS and LDS is independent from and should not be confused with the mode bit explained below.

The main difference between the Channel and WP views of the WRAM is that the 68000 has an internal concept of bytes and words and generates, internally at least, A0. The address generated by the channel card has no internal A0 and an implicit zero is tacked on in the 16-bit mode. In the 8-bit case the address is shifted right to use A1 as the odd/even byte selector.

As indicated by the memory maps, the lowest number 2M card which can be installed is card 1. There is no memory mapping of WRAM contents.

8/16-bit Modes

The WRAM may be read in either full 16-bit or left-justified 8-bit mode. 16-bit mode gives optimum audio quality, while 8-bit mode doubles the length of sounds which can be stored, with reduced audio performance. Mode selection is on a cycle-by-cycle basis so mixed 8- and 16-bit sounds can be in WRAM simultaneously. The mode is selected by an auxiliary buss line which must be driven appropriately by the accessing device.

In the 8-bit case the data byte is output on the most significant data lines whether or not it was written at an odd or even address, and the least significant 8 data lines are driven with zero. As mentioned above the waveform address is shifted right once by the WRAM so a byte written at a given address in 16-bit mode will be read back at twice the address in 8-bit mode. This has the side effect of doubling the apparent size of each WRAM card to 1M or 4M bytes. The "shifted out" address line, A1, is used to select the odd or even byte and control the left-justification circuitry. See WRAM memory maps for further explanation.

The purpose of the 8-bit mode is for 8-bit sounds to be played by the channel cards. There is no need for the WP to access the WRAM in 8-bit mode except to test the WRAM. When the 16-bit mode is selected, WRAM appears as just normal memory which supports byte and word accesses by the 68000 as described in Section 1.2. Code can be executed in WRAM by the 68000 provided it accesses WRAM in 16-bit mode.

Timing Generation

(refer schematic CMI-39-00 and timing diagram)

All timing is generated from one bus signal SCLK, which originates from the Channel Support card, and control signals from the Waveform Bus arbitration logic on the Waveform Processor. The whole Waveform Bus is synchronous to this signal. SCLK has a 300nS period, which sets the bus cycle time at 300nS, and a 1:3 duty cycle. SCLK is inverter-buffered and fed into a ten tap, 25nS/tap digital delay line at A6. Four delayed versions of SCLK are then combined in various ways to produce the complex waveforms required to drive the RAM array at the highest possible speed.

A valid access cycle is indicated by a low on the control signal $\overline{\text{WAS}}$ (Waveform Address Strobe), and a refresh cycle by a low on $\overline{\text{WREF}}$ (Waveform Refresh). In either case, $\overline{\text{RAS}}$ (Row Address Strobe) is clocked on the rising edge of the 4th delay line tap and is cleared again by the next low on the 3rd tap. The $\overline{\text{RAS}}$ pulse is driven through the HC244 buffer C18 (CMI-39-01) to all RAM chips.

The WR/W line is buffered by A18 and latched at A4 by rising edge of tap 3. Since this flip-flop is not otherwise set or reset, LR/W (Latched Read/Write) is updated every 300nS.

RA and CA are the Row and Column Address drive lines which control the address multiplexor (CMI-39-02). While these two signals are essentially the inverse of each other, RA is generated by the LS00 at A9 and CA by the ALS08 at A7. This ensures that they are as close as possible to non-overlapping so that contention is not caused on the multiplexed address lines. CA and RA both are inverted to produce $\overline{\text{CA}}$ and $\overline{\text{RA}}$ which will be similarly non-overlapping. Thus the Column address is enabled when both taps 4 and 5 are high, and the Row address is enabled on the opposite condition.

CAS is just a timing signal generated continuously which is later qualified to produce the actual $\overline{\text{CAS}}$ (Column Address Strobe) signals to the RAM array. It is 100nS long, from the rising edge of tap 7 to the falling edge of tap 3.

The Output Enable signals $\overline{OE1}$ - $\overline{OE4}$ drive the latches and buffer on CMI-39-03. The logic preceding the data inputs to the LS175 at B9 will be explained along with output section. The timing of these signals are that they are clocked out on the rising edge of tap 7, and cleared when tap 3 is high but tap 5 is low. This results in a 200 output drive pulse during valid read cycles. If READ is low, the latch will be held cleared across the clock edge so no outputs will be enabled.

Address Decoding

refer schematic CMI-39-01)

As described in Sect. 1.2, 256K RAM chips yield 2M bytes on each card, and 7 cards can be plugged into the Series III system. Therefore the top 3 address lines are used as the card select bits. In 16-bit mode, B8BIT is low so WA23-WA21 are buffered through A17, through the link block at A15 to become CS2-CS0 and into the LS85 comparator at A14. If the data on these three lines agree with the setting of the DIP switch, a high is output from the LS85. If a low on $\overline{WAS}$ indicates a valid access cycle, a low is generated by A9 pin 8 and this is latched on the rising edge of tap 3 (SCLKD125 = SCLK inverted and delayed by 125nS) to produce the enable for the memory rank decoder A3.

In 8-bit mode the one-bit right shift of the address is effected by enabling buffer A16 instead of A17 when $\overline{B8BIT}$ is low. Then only WA23 and WA22 are used as card select lines because four cards fill up the address space (see memory maps).

The next two address bits (WA20 and 19 in 16-bit mode, WA21 and 20 in 8-bit mode) come out of the link block as BLK1 and BLK0. These are used as the block number, to determine which rank of RAM chips is accessed. BLK1 and BLK0 are again latched by SCLKD125 and input to the 1-of-4 decoder A3. The decoded rank select goes to both halves of A2. One of the Upper and/or Lower $\overline{CAS}$ outputs are then driven, depending on the CAS timing pulse and either or both buffered data strobes (BUDS and BLDS).

Being a TTL device, A2 has to drive the RAM array through series resistors. At the end of the CAS pulse both halves of A2 are desabled and the $\overline{CAS}$ lines are pulled up quickly by 330R pullups.

The valid card select signal (A9 pin 8) is also combined with the BR/W signal (Buffered read/write) and latched to produce the READ signal. READ feeds back to the logic on CMI-39-00 which inhibits the output enable signals if a cycle is not a valid read.

The next two address lines (WA18, 17 in 16-bit mode, WA19, 18 in 8-bit mode) are used by the top ninth of the address multiplexor formed by the LS125 B18. Either of these two gates are enabled by the active low Row and Column Address lines ($\overline{RA}$ and $\overline{CA}$) and drive A8 through the HC244 buffer. The lower of the two address lines is latched at B3 first.

Revision 2 and earlier cards support 64K RAM chips. If these are used each card only provides one quarter as much memory. To keep successive cards contiguous in the memory space, all the card select and rank select lines must be shifted down 2 bits with the respect to the address bus. This is performed by changing the link block A15 to connect pins 3-16, 4-15, 5-14, 6-13, 7-12 and 8-11. Then in 16-bit mode WA23 is ignored, WA22-WA19 become CS3-CS0, and WA18 & 17 become BLK1 & 0. 64K chips do not have an A8 address line so LS125 multiplexor inputs do not have to be adjusted. Again, 8-bit mode shifts the card and rank select bits along once.

The HC244 buffer C18 drives the write (/W) lines and the $\overline{RAS}$ lines of the four ranks of RAM.

Address/Refresh Multiplexor

(refer schematic CMI-39-02)

Dynamic RAMs have multiplexed address inputs which allow, in this case, 256K bits per chip to be addressed with only 9 address pins compared to 18 pins which would be required by a non-multiplexed addressing arrangement.

During a valid memory access the first half of the address is enabled by a high on RA and strobed into the RAMs on the falling edge of $\overline{RAS}$. In 16-bit mode ($\overline{B8BIT}$ high) this is WA1-WA8 through B14, and in 8-bit mode, WA2-WA9 are driven through B15. The waveform address buss is stable during the critical setup and hold times before and after $\overline{RAS}$ so the buffers can drive the RAMs directly.

It can be seen from the timing diagram that the channel card does not assert its address for very long after the falling edge of $\overline{CAS}$, so it is necessary to latch the column address. WA9-WA16 are enabled in 16-bit mode, and WA10-WA17 in 8-bit mode, onto the HC373 inputs at B13. These are both latched and driven to the RAMs by B13 when CA goes high. The falling edge of $\overline{CAS}$ clocks the column address into the RAM chips.

During a refresh cycle both the row address buffers and the column address latch are disabled by the low on $\overline{BWREF}$. The same signal increments the LS393 refresh counter and drives the refresh count onto the RAM address lines.

Data Bus Interface

(refer schematic CMI-39-03)

HC244s B1 and B17 are permanently enabled to buffer data off the waveform data bus to the RAM D inputs. During write cycles the data is written in to the RAM on the falling edge of $\overline{CAS}$. During read cycles, input data is ignored.

The remaining three latches and one buffer are used during read cycles to output 16-bit data and left-justified 8-bit data. Left-justified means that whether the data byte is in the low or high 8 bits of the addressed memory word, it appears on the upper 8 bits of the data buss and the lower 8 bits are driven to zero. All latches are clocked by the falling edge of the CAS timing signal which is near the end of the low-going $\overline{CAS}$ pulse on the RAM chips.

The latch outputs are enabled by the LS175 outputs $\overline{OE1}$-$\overline{OE4}$ on CMI-39-00. The three cases are: 16-bit read, 8-bit even read, and 8-bit odd read. The high RAM byte must drive the high buss lines in the 16-bit read case (B8BIT low) or in the 8-bit even case (ODD low). This gives the gating for $\overline{OE4}$.

The low RAM byte must drive the low buss lines only in the 16-bit case, so $\overline{B8BIT}$ high is the input for $\overline{OE3}$.

The low RAM byte must drive the high buss lines only in the 8-bit odd read case when B8BIT and ODD are both high. This gating produces $\overline{OE2}$.

$\overline{OE1}$ enables the buffer with all inputs to ground onto the low data lines, which is required for any 8-bit cycle (B8BIT low). The ODD signal is simply buffered WA1, which is ignored by the decoding and multiplexor during 8-bit cycles. To put it another way, WA1 is "shifted in" to the WA0 position which is the odd/even byte selector and does not explicitly exist on the buss.

RAM Array

(refer schematic CMI-39-04.05)

The CMI-39 memory is composed of 256K or 64K by 1-bit chips. The 64-chip ram array is divided into four columns, or ranks, of 256K or 64K by 16 bits each. Rank 0 which occupies the bottom quarter of the address space, is in F column nearest the front edge of the board. Each rank is divided into an upper and a lower byte distinguished by upper and lower $\overline{CAS}$ signals. It is the $\overline{CAS}$ signal alone which determines whether a given group of 8 chips are accessed: data in, $\overline{RAS}$ and $\overline{W}$ signals are distributed to all chips but it is the presence of $\overline{CAS}$ which determines whether data is written into or read out from a RAM chip.

Refresh cycles are performed by asserting $\overline{RAS}$ while the refresh count is driven on the address lines, without a subsequent $\overline{CAS}$ pulse. During an access cycle of one group with $\overline{CAS}$ asserted, the presence of $\overline{RAS}$ without $\overline{CAS}$ on another group will refresh the row of memory cells in the non-accessed group corresponding to the accessed row address. The accessed group is also refreshed in the process of reading or writing to it. It is for this reason that the Waveform Processor Bus Arbitration logic gives higher priority to channel card accesses than to refresh: if channel cards are hogging the buss to the extent that refresh cannot be serviced it can be guaranteed that the RAM array will be refreshed by the channel accesses alone. This is true providing at least one of the channels is playing a loop of 256 or more words, since an 8-bit refresh count must be fully cycled to refresh the whole of memory. This is also why the least significant 8 waveform address bits, which change the most rapidly when a channel is looping, are used as the row address.

Timing Tolerances

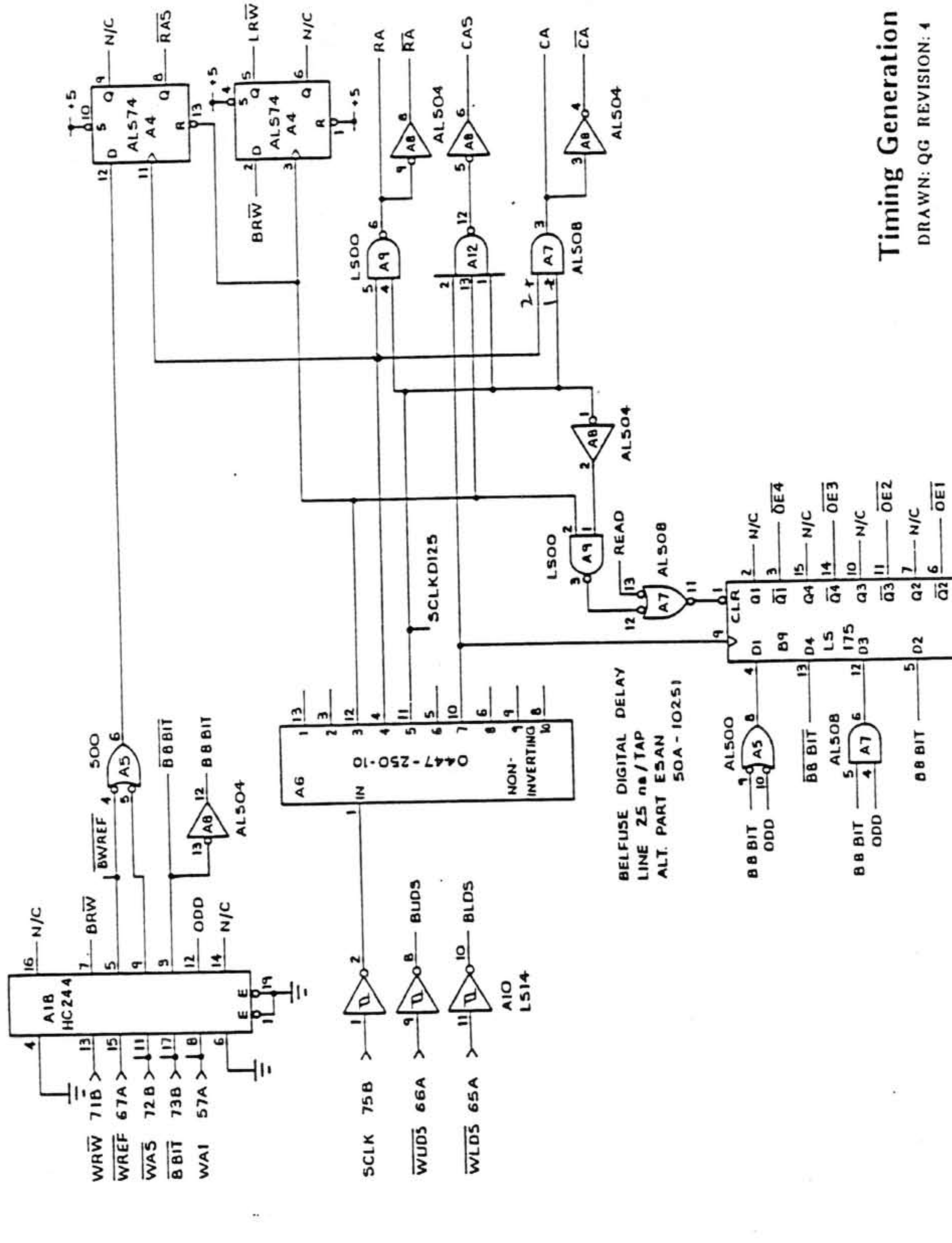
The CMI-39 Waveform RAM operates at a continuous cycle time of 300nS and is designed to use 150nS access time RAM chips which usually have a minimum cycle time of 300nS. As a result, some timing tolerances are extremely tight and it was not possible to design the board to cope with all components operating at their worst-case level. In practice this should not be a problem since RAM timing requirements such as the 300nS cycle time are specified for worst-case conditions of temperature, radiation level etc. and most RAMs will still work when being driven considerably out of spec. However, to provide a guide in case future component variations are suspected to be causing problems, the following is a list of tight parameter specs and actual measured timings from typical CMI-39 boards. Various RAMs have slightly different timing requirements: the list specifies the most difficult to meet of several brands analyzed. In most cases, 256K chips have easier specs than 64K chips.

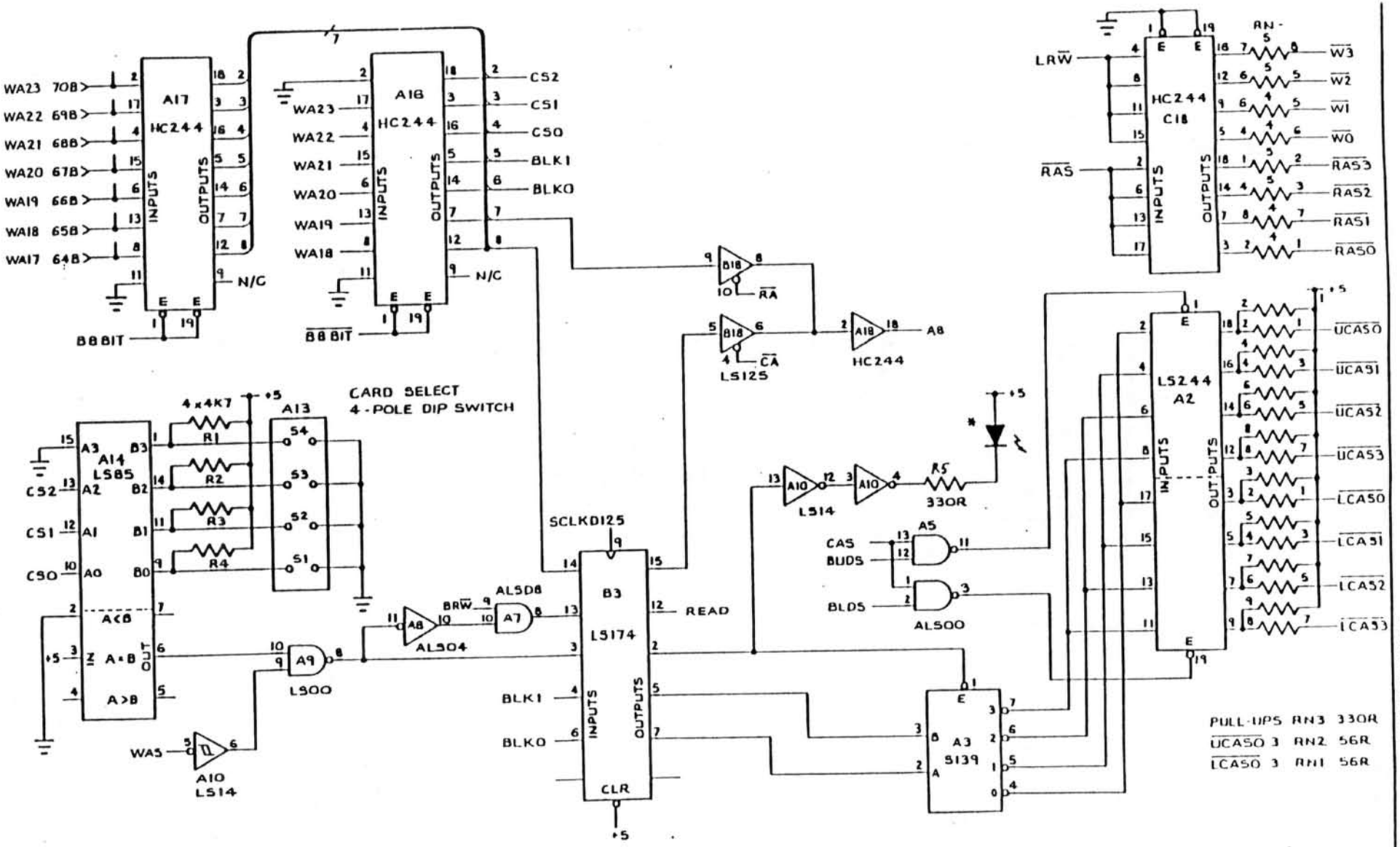
Symbol	Parameter	Spec.	Measured
t_{RC}	Cycle time	300	300
t_{RP}	RAS precharge	120	120
t_{RAS}	RAS width	150	150
t_{CAS}	CAS width	75	80
t_{RCD}	RAS to CAS lead time	75	75
t_{RSH}	RAS hold	75	80
t_{CSH}	CAS hold	150	150+
t_{ASR}	Row address set up	0	40
t_{RAH}	Row address hold	20	20
t_{ASC}	Column address set up	0	30
t_{CAH}	Column address hold	45	140
t_{DS}	Data in set up	0	50

The above specs are all minimum, and all entries are in nS. All measurements are made on the RAM chips themselves.

The following measurements may be of interest:-

Buffered $\overline{SCLK}$ rising edge to $\overline{RAS}$ falling edge	120
Buffered $\overline{WAS}$ falling edge to $\overline{RAS}$ falling edge	100

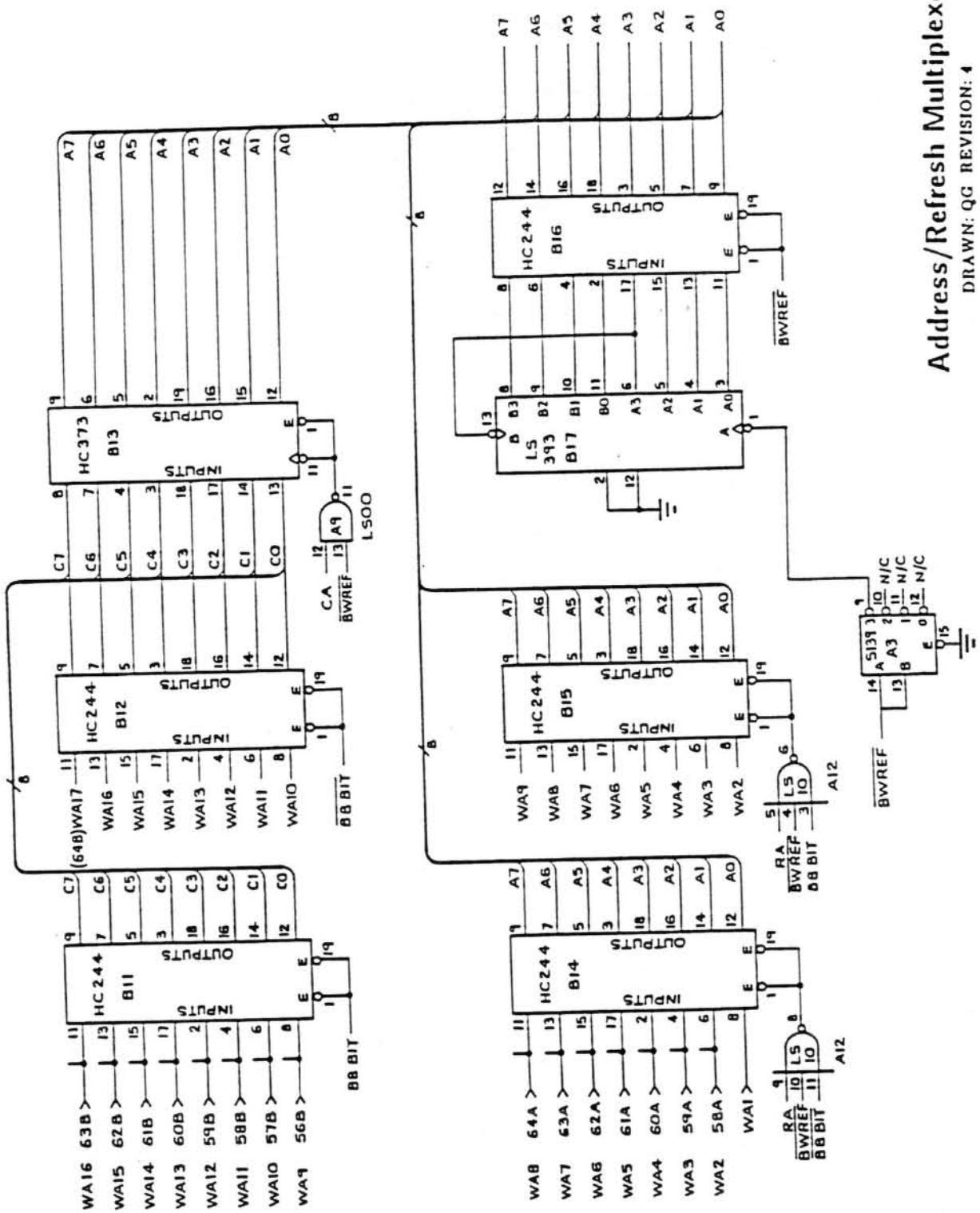

Timing Generation
DRAWN: QG REVISION: 4
BELFUSE DIGITAL DELAY
LINE 25 ns / TAP
ALT. PART ESAN
50A - 10251

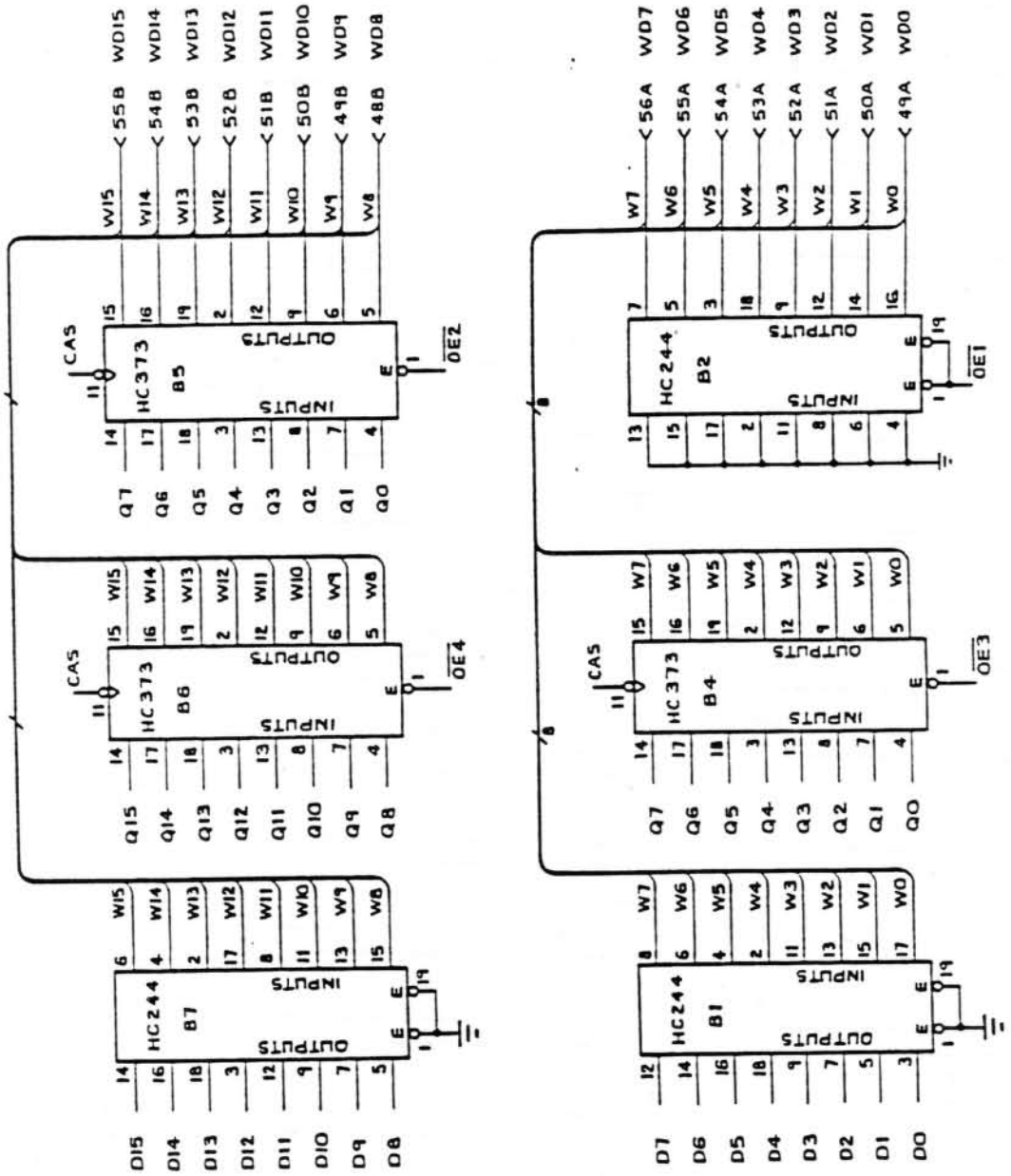


*LED: USE DIALITE 555-2401 WITH 330R RESISTOR (R5)
OR DIALITE 555-2403 WITH RESISTOR SHORTED OUT
OR STANDARD 3mm LED WITH 220R RESISTOR

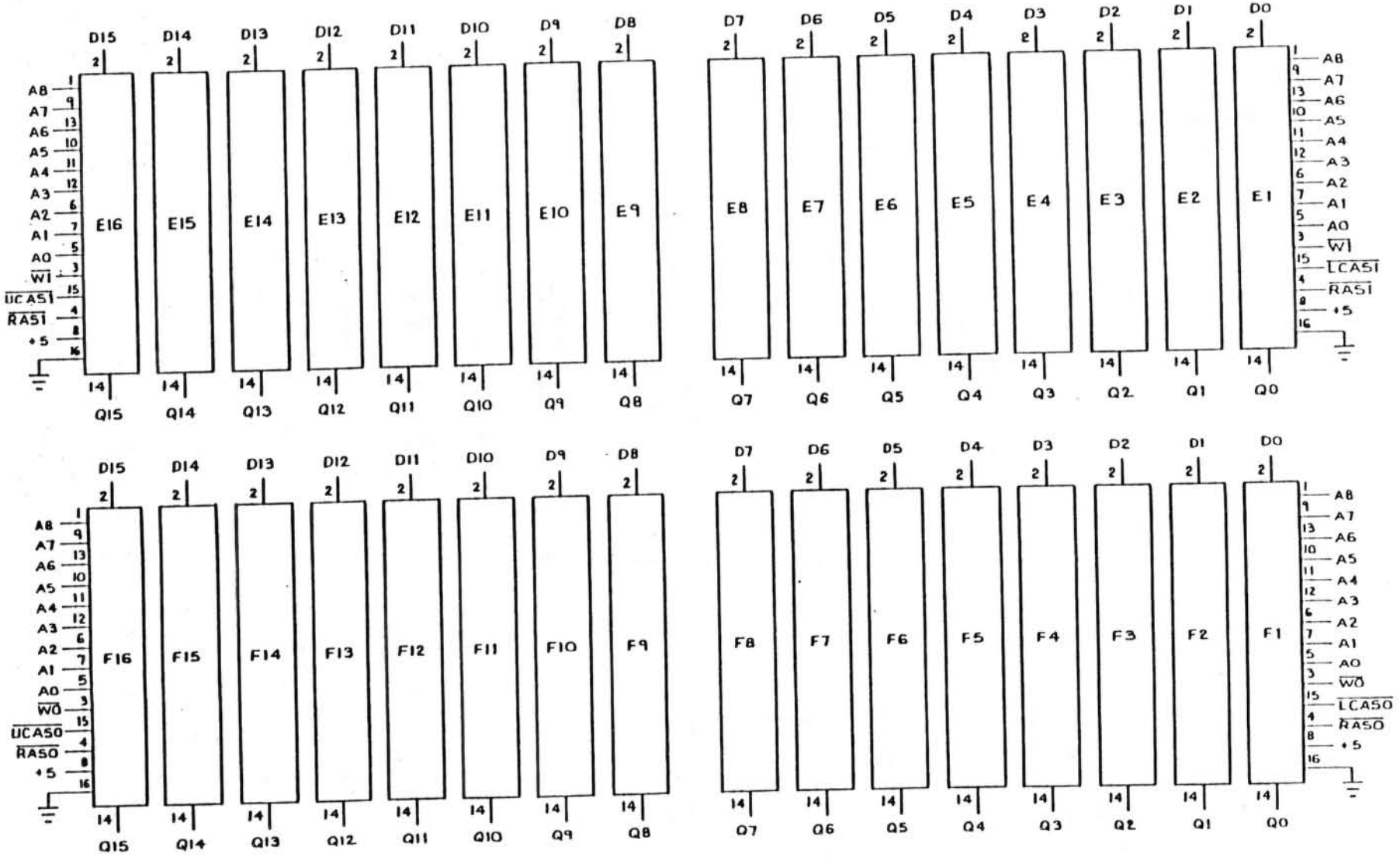
Decoding

DRAWN: QG REVISION: 4


Address/Refresh Multiplexor
DRAWN: QC REVISION: 4
HC373 B13
HC244 B12
HC244 B11
HC244 B16
LS 393 B17
HC244 B15
HC244 B14
5139 A3
LS00
LS10
INPUTS
OUTPUTS
BWREF
88 BIT
CA
RA
A12
N/C


Data Bus Interface
DRAWN: QG REVISION: 4
HC244
B1
B2
B7
B8
HC373
B4
B5
B6
INPUTS
OUTPUTS
CAS
OE1
OE2
OE3
OE4
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
WD0
WD1
WD2
WD3
WD4
WD5
WD6
WD7
WD8
WD9
WD10
WD11
WD12
WD13
WD14
WD15

fairlight

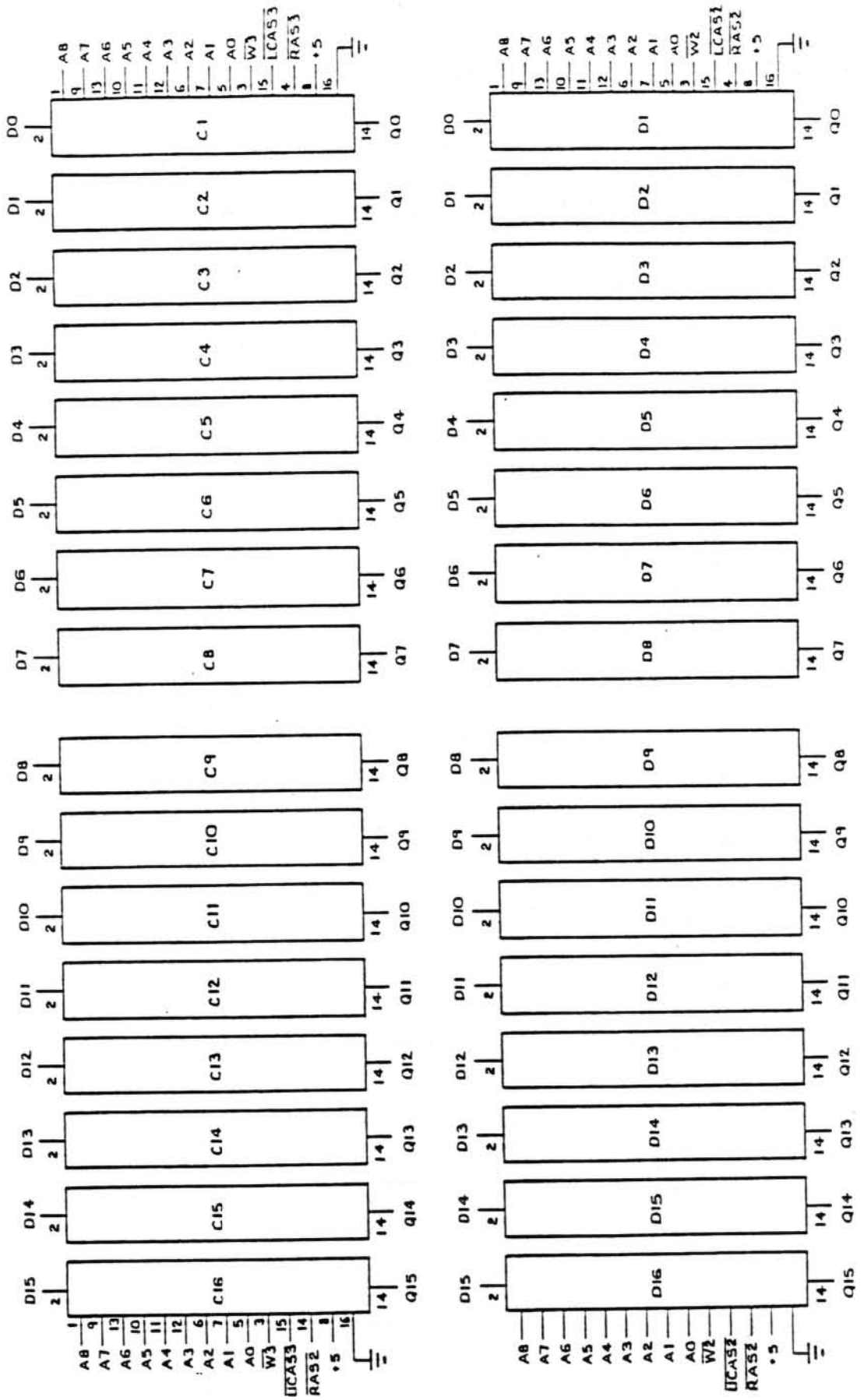


COMPATIBLE 256K RAMS:-
50256-15 (HITACHI)
MN41256 (MATSUSHITA)
6256-15 (MOT.)
41256-15 (NEC)

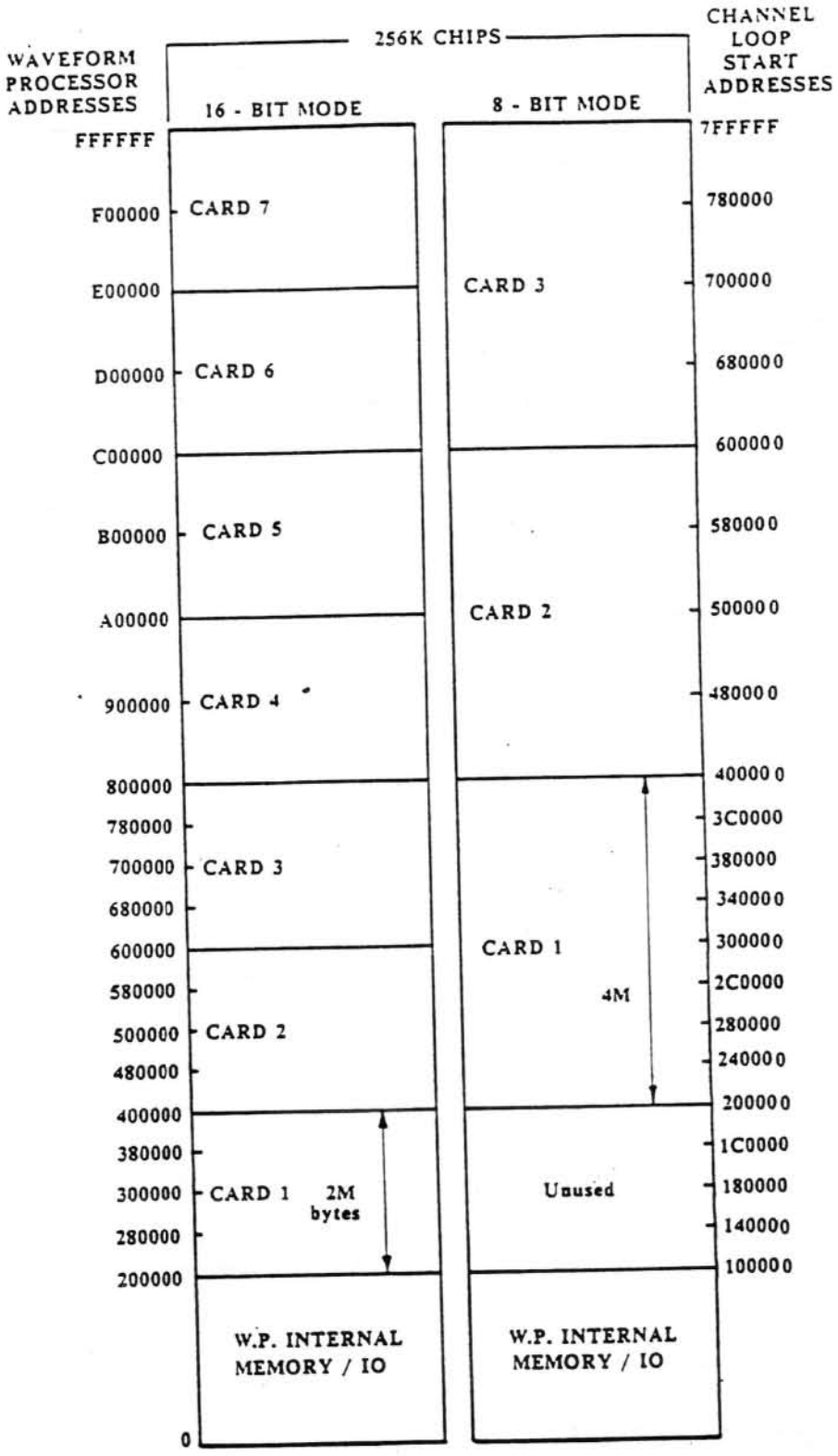
RAMS MUST BE 150 nS MAX.
ACCESS TIME OR FASTER

Dynamic RAMS

DRAWN: QG REVISION: 4


Dynamic RAMS
DRAWN: QG REVISION: 4
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
A8
A7
A6
A5
A4
A3
A2
A1
A0
W3
W2
CAS3
CAS2
RAS3
RAS2
+5
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15

CMI-39 Waveform Memory Map



Waveform Ram Timing

fairlight