DSP-96K

WAVEFORM PROCESSOR

DSP - 96k Boot Sequence

After executing 'debug96 -p' the following sequence of events should occur.

(1) The WS asserts reset by writting to the control latch in DSPCTRL (*WCTRL asserted).

(2) WS writes program into WRAM (at 4800400).
If this is successful you should be able to to see data as below:

4800400: 03003F00 00000EFE 00000000 00000000

4804000: 03803F51 03807F09 0380BF5D 0380BF5D

(note that the code at 4804000 is the code that appears on the **dsp-96k overlay handler/loader** listing)

(3) The WS writes to the control latch to clear reset (*WCTRL asserted)

(4) The DSP then reads 4096 bytes from address 0. This is the location of the DSPINIT boot prom. As the prom is only 32 bytes long, the data is aliased 128 times. The data read is placed into internal DSP program memory and then executed.

The data in the DSPINIT prom is:

FD397D00 00000000 803F0C03 00010082
00000101 00000002 00000000 626F6F74

You should be able to see this sequence being read after clear of reset by triggering a logic analyser on *ROMEN and monitoring DB0..7 data lines.

The code in DSPINIT is:

(1) Set wait states to 0 (no external accesses needed for this)
(2) Jump to $82000100

NOTE: (1) The WRAM is mapped at $82000000 for the DSP, and at $4800000 for the WS.

(2) All addresses seen by the WS are byte addresses, and addresses seen by the DSP are long (32 bits) addresses.

This means that the jump to $82000100 will be to the location $4800400 as seen by the WS - i.e. the location where the loader was placed by the WS. Thus the DSP jumps to the loader code to continue operation.

(5) Once the DSP has executed the DSPINIT boot code and jumps into the loader in WRAM, the *DACC signal will be asserted indicating access by the DSP to WRAM.

(6) Soon after this, the DSP will write twice to the DSPCTRL control latch (*DCTRL asserted).
[see the overlay code listing at lines 1526 and 1527].

(7) The DSP code then copies the contents of the DSPINIT boot prom to $82000000 ($4800000 for WS). There should be 4 reads from DSPINIT and a write to WRAM repeated

8 times.

(8) From this point, there should only be accesses to WRAM by the DSP as it polls for new commands written by the WS into WRAM.

Additional Notes

(1) To start OSK from K007 partition type:

osk k007

(2) To display a region of WS memory using OSK type:

debug

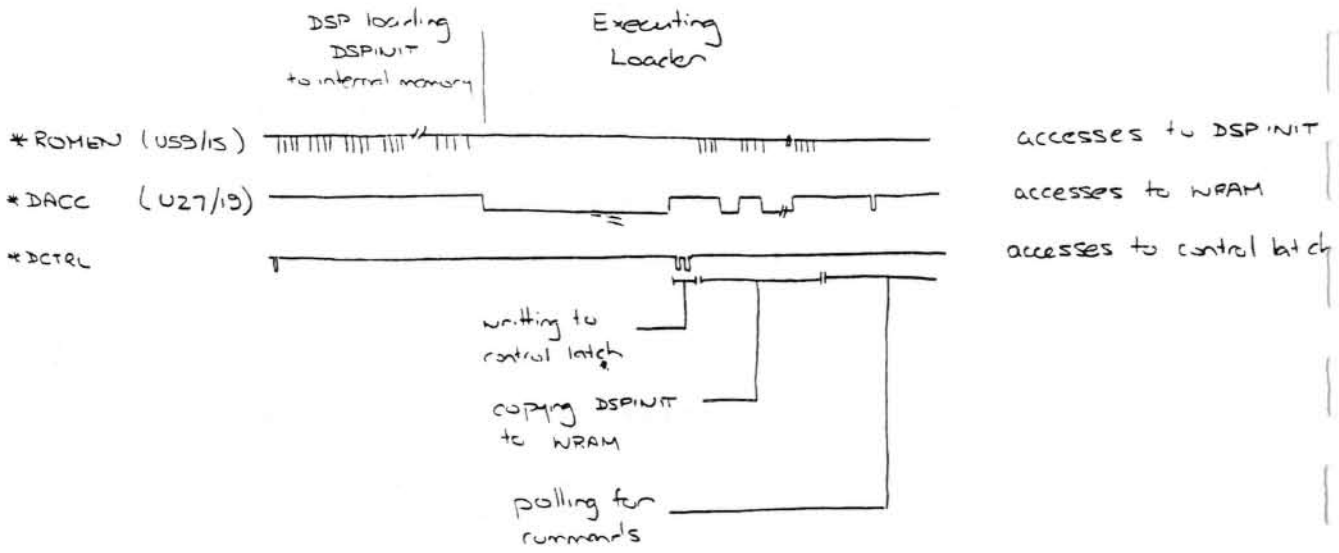
Then at dbg: prompt type:

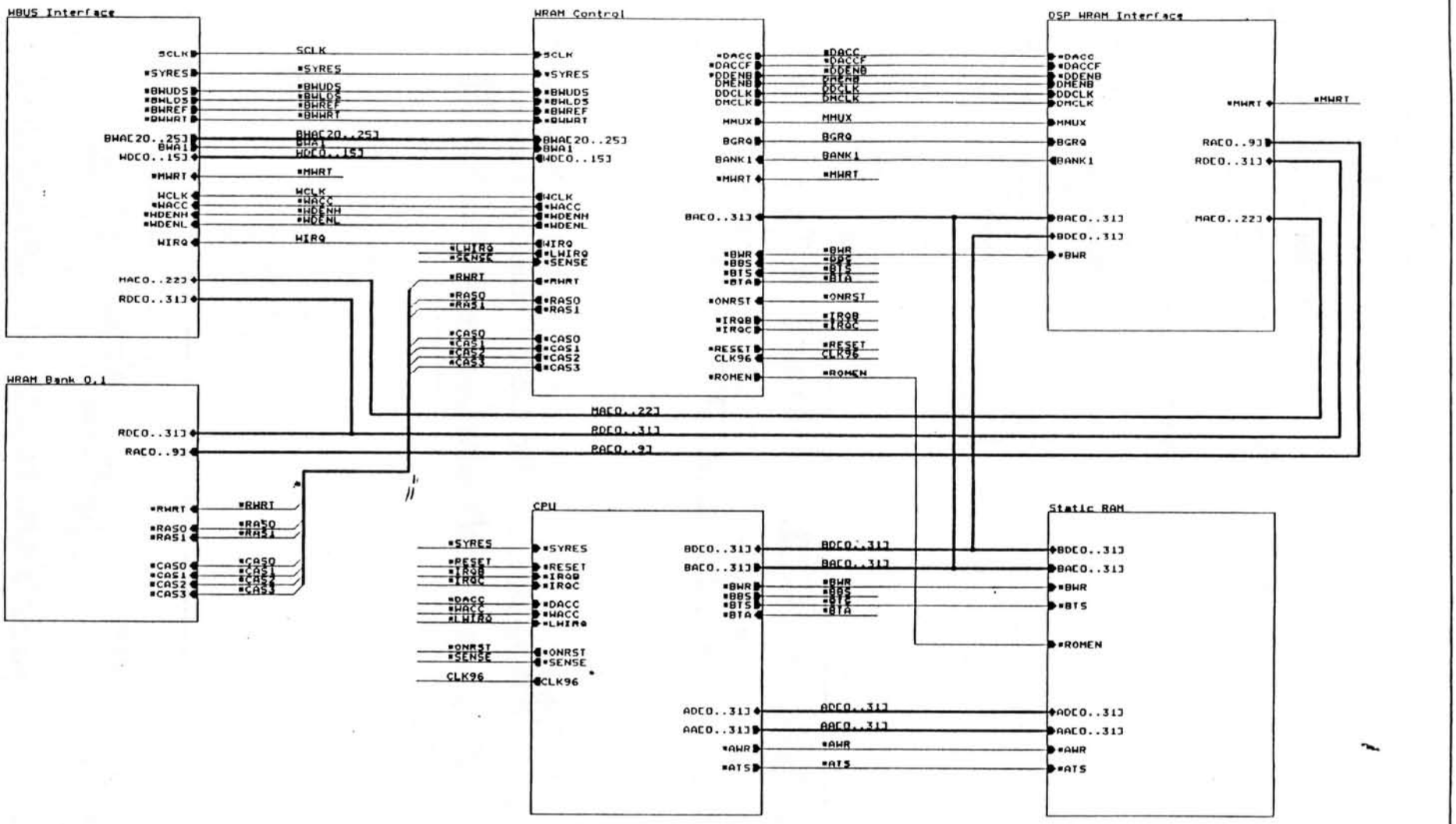
d <start address> <count>

To quit type 'q'

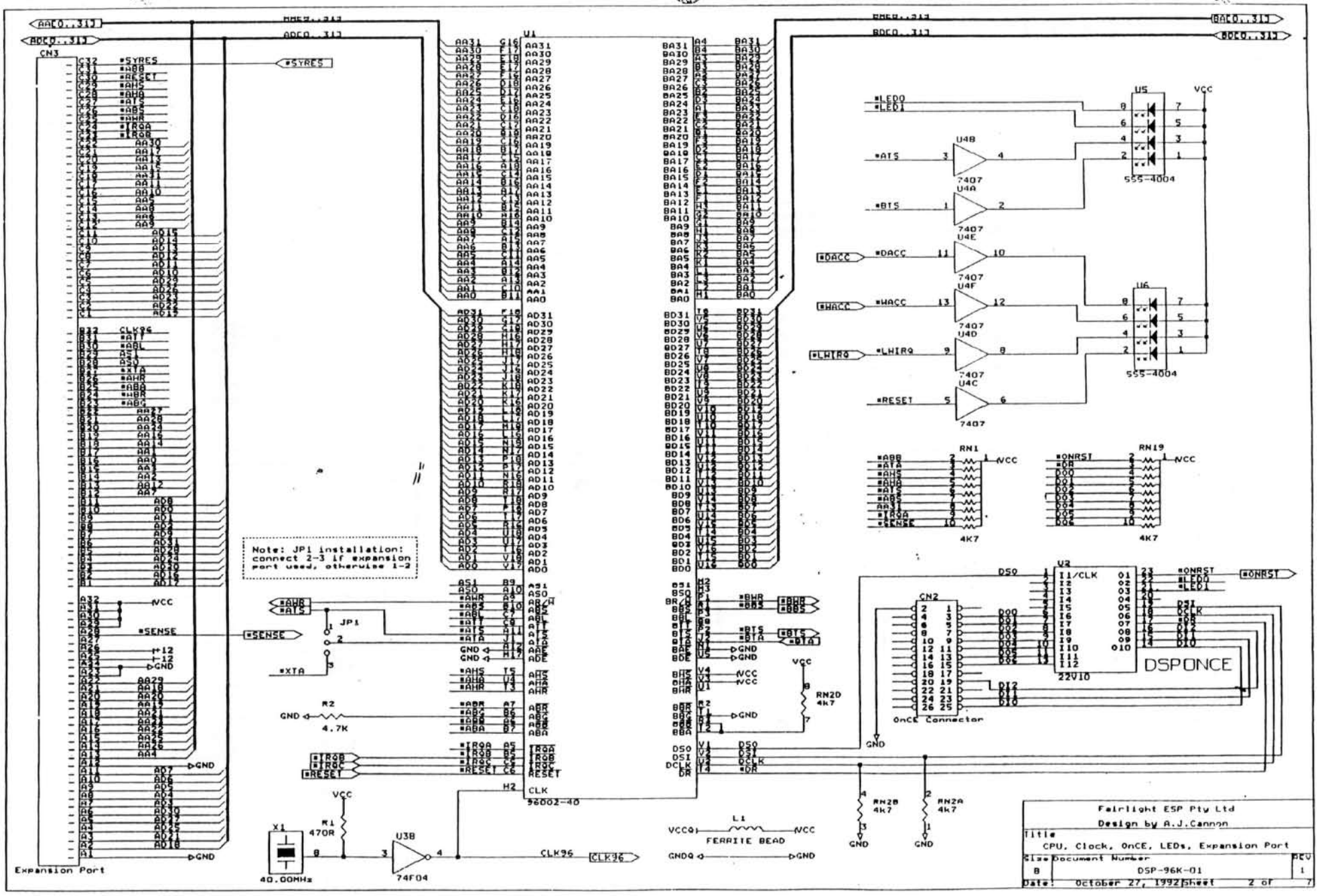
(3) The 96002 prefetches instructions. This means that even if the current instruction is a branch (bra in listing), then the next instruction is fetched and discarded.

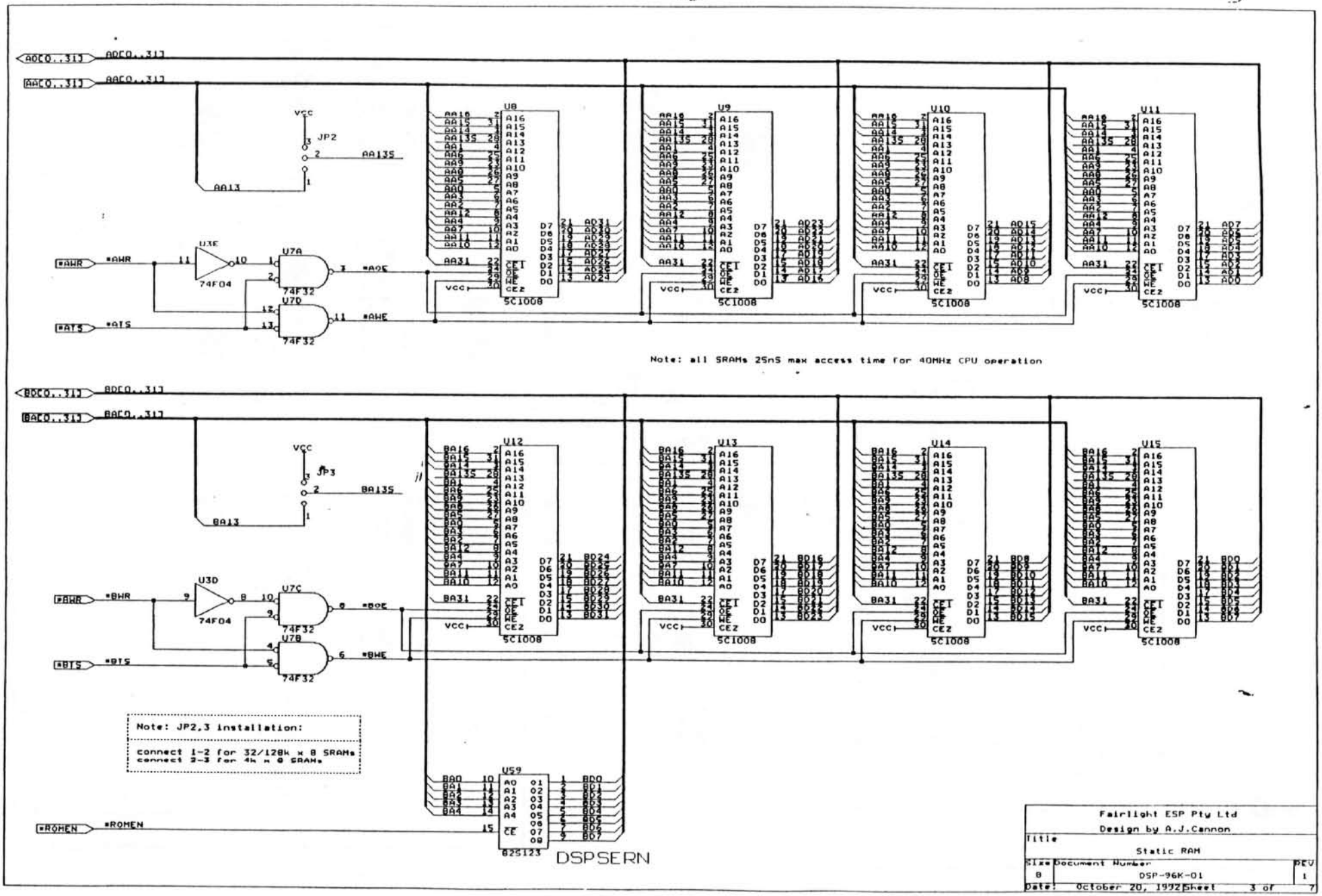
Simplified Sequence of events as seen on Logic Analyser

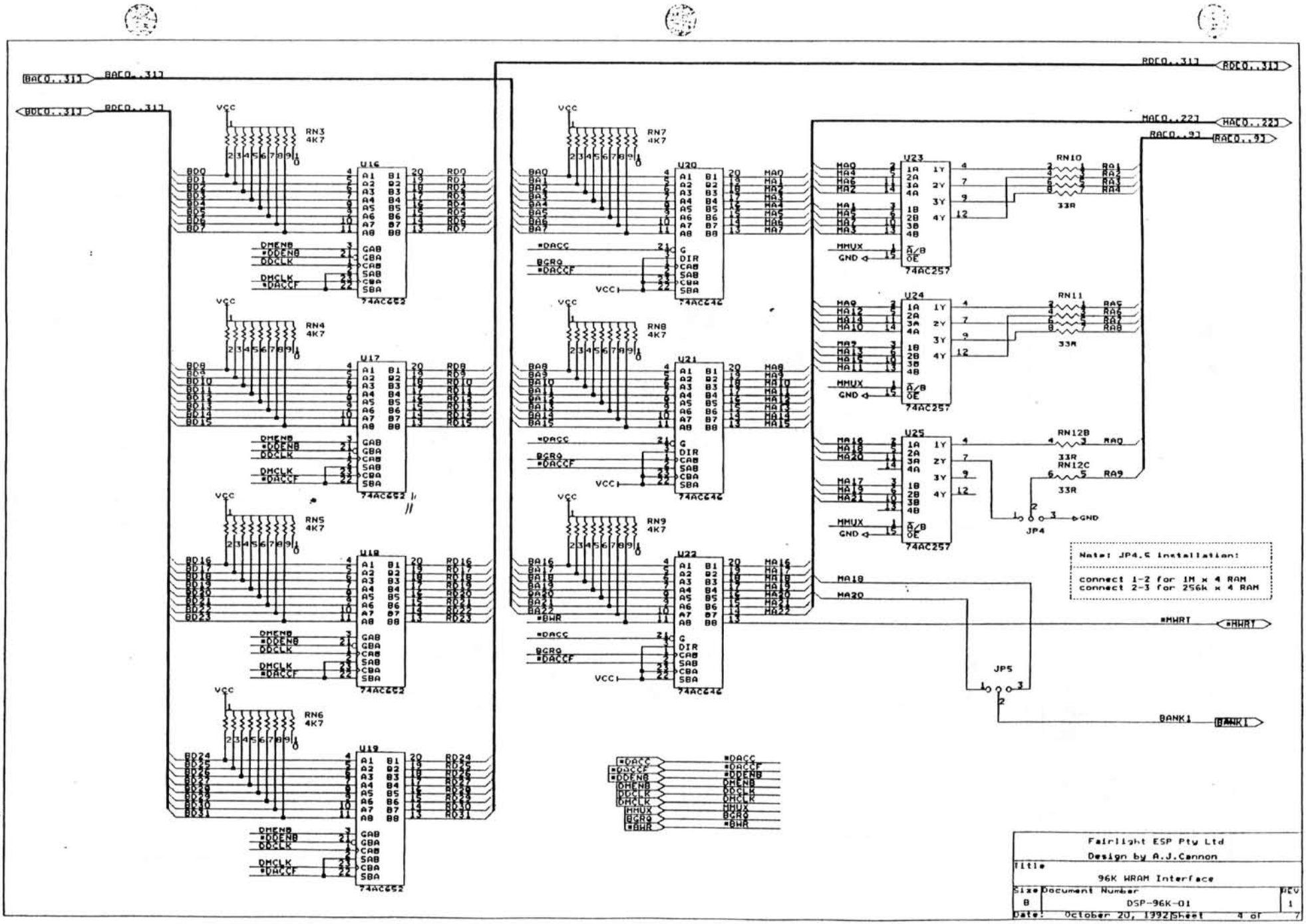


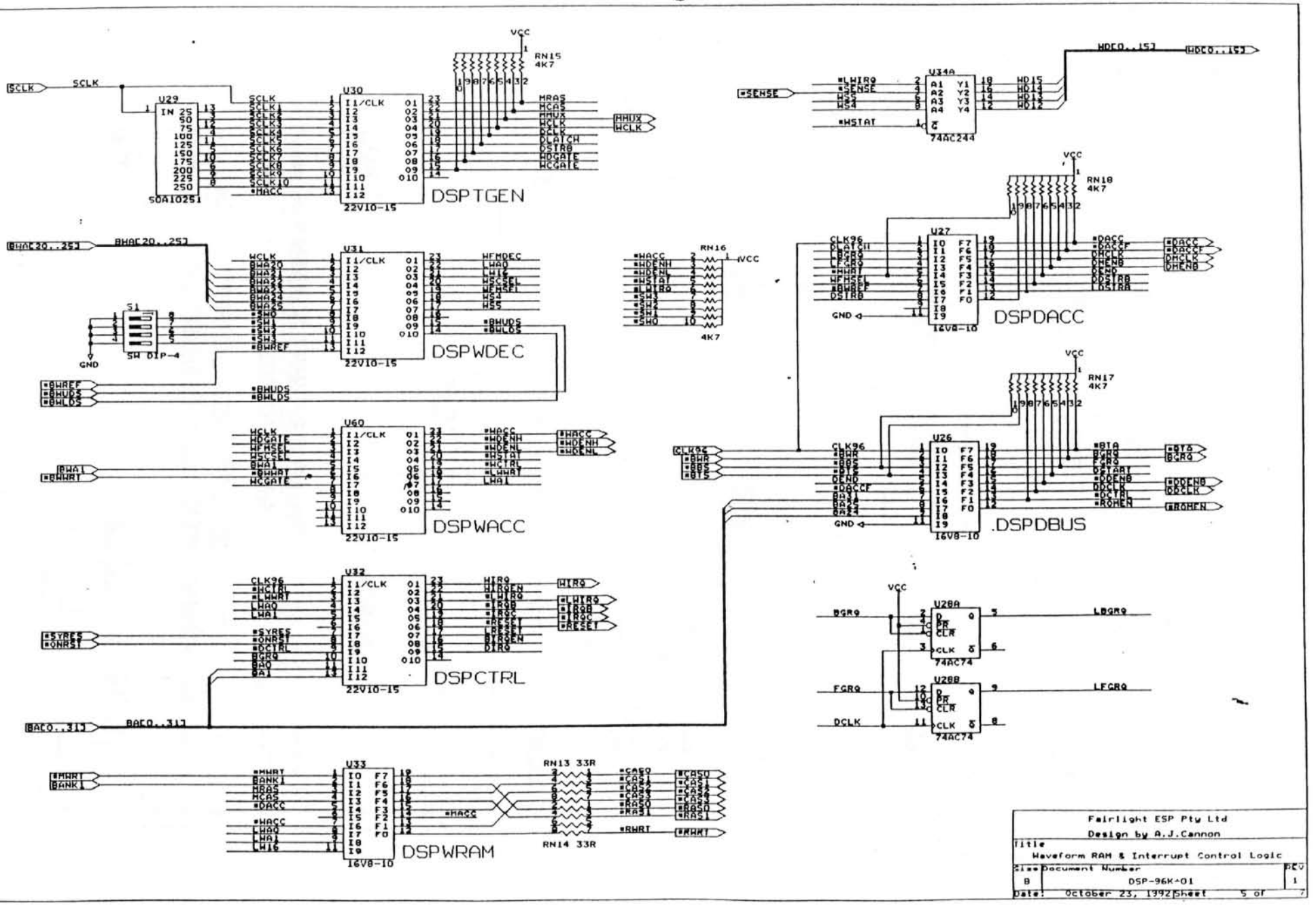


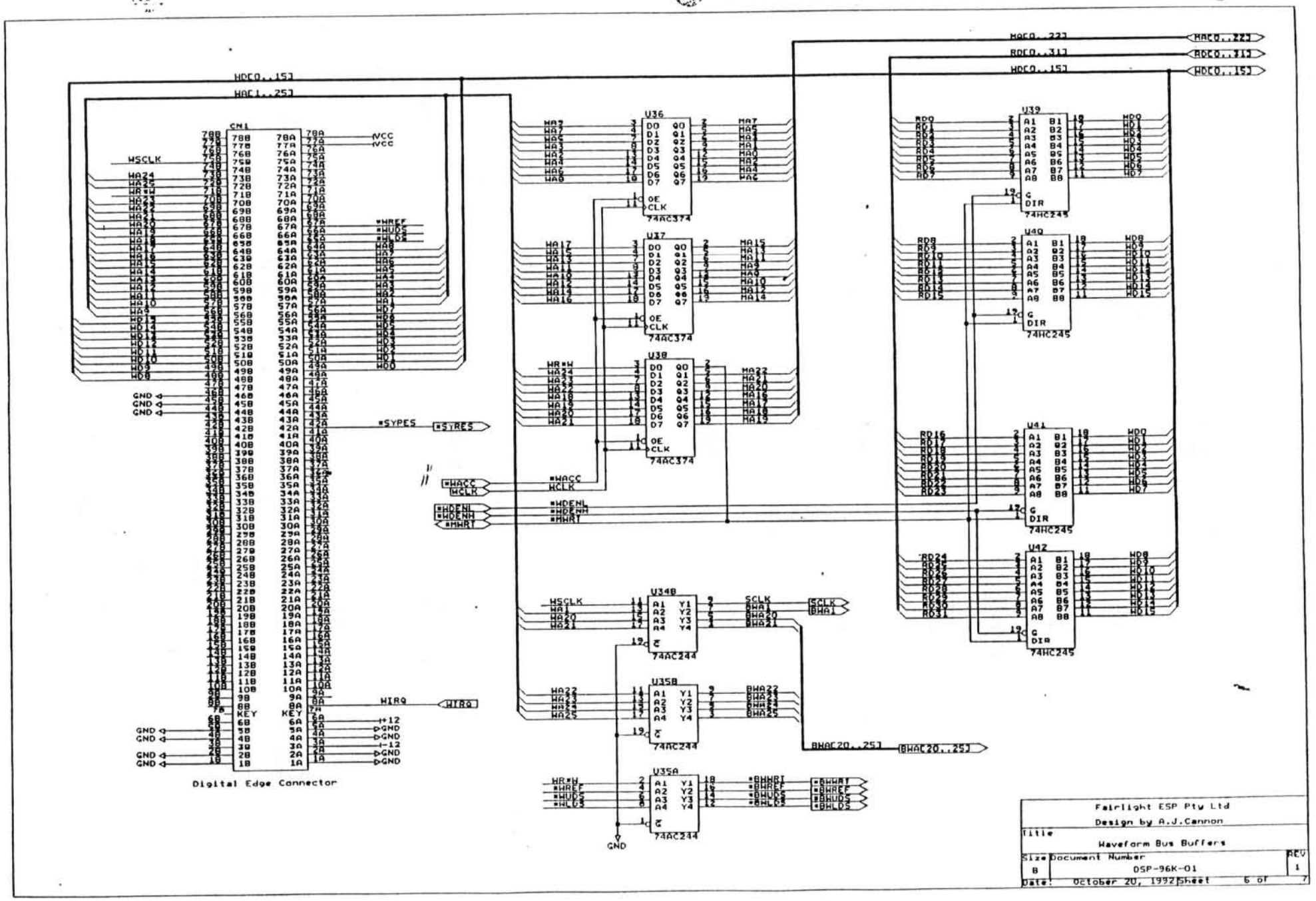
Fairlight ESP Pty Ltd		
Design by A.J.Cannon		
Title: 96002 DSP Accelerator Card		
Size: B	Document Number: DSP-96K-01	REV: 1
Date: October 23, 1992	Sheet 1 of 7	

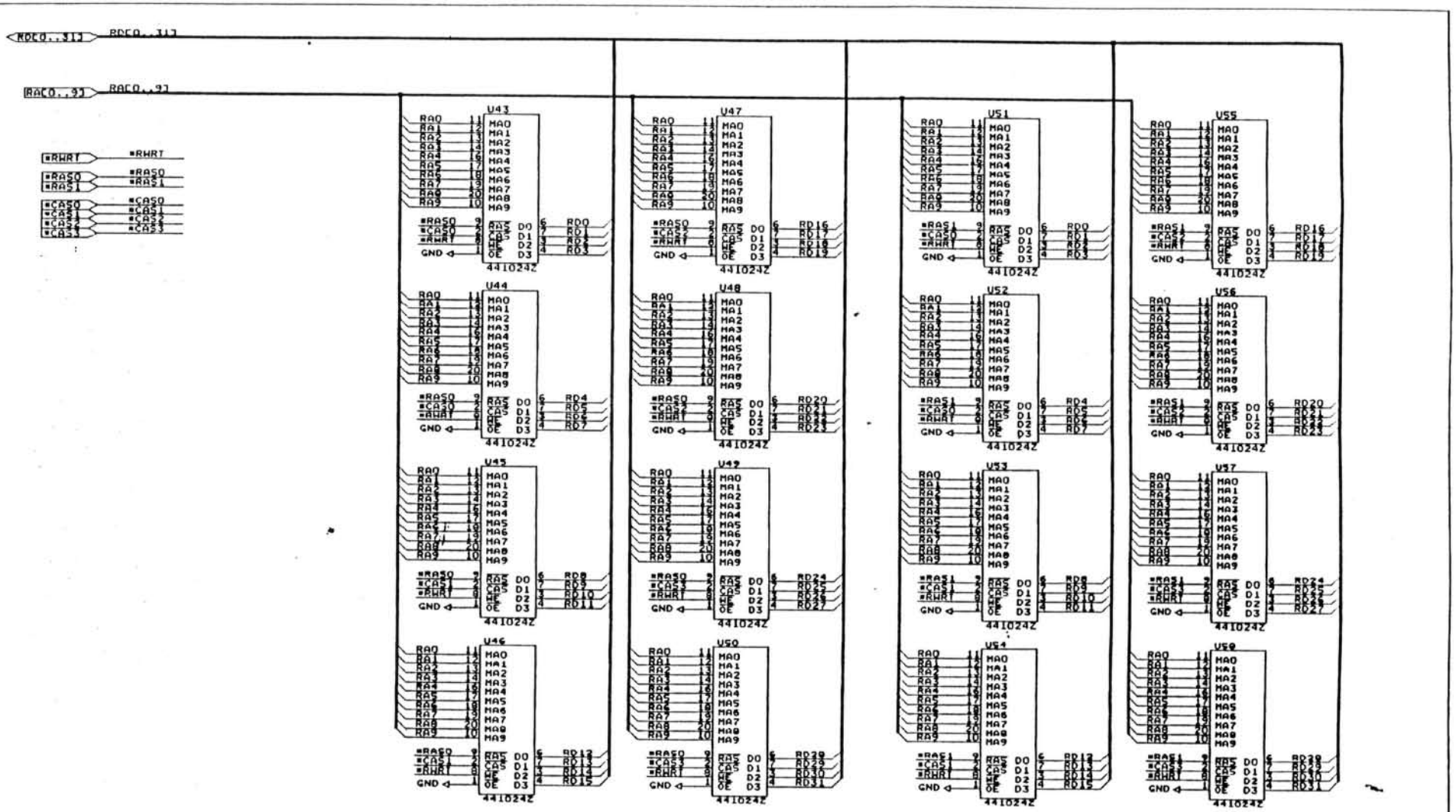

CN3
Expansion Port
U1
Note: JP1 installation:
connect 2-3 if expansion
port used, otherwise 1-2
JP1
R2
4.7K
X1
40.00MHz
R1
470R
U3B
74F04
56002-40
CLK
CLK96
L1
FERRITE BEAD
U5
555-4004
U6
555-4004
U4B
U4A
U4E
U4F
U4D
U4C
7407
RN1
RN19
4K7
RN2D
RN2B
RN2A
U2
22V10
DSPONCE
CN2
OnCE Connector
Fairlight ESP Pty Ltd
Design by A.J.Cannon
Title
CPU, Clock, OnCE, LEDs, Expansion Port
Size
B
Document Number
DSP-96K-01
REV
1
Date: October 27, 1992
Sheet 2 of 7


ADCO..31
AACO..31
VCC
JP2
AA13S
AA13
U8
U9
U10
U11
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
D7
D6
D5
D4
D3
D2
D1
D0
CE1
OE
WE
CE2
AA31
VCC
5C1008
*AWR
*AIS
U3E
74F04
U7A
U7D
74F32
*AOE
*AWE
Note: all SRAMs 25nS max access time for 40MHz CPU operation
BDCO..31
BACO..31
JP3
BA13S
BA13
U12
U13
U14
U15
*BWR
*BIS
U3D
U7C
U7B
*BOE
*BWE
Note: JP2,3 installation:
connect 1-2 for 32/128k x 8 SRAMs
connect 2-3 for 4k x 8 SRAMs
U59
BA0
BA1
BA2
BA3
BA4
CE
825123
*ROMEN
DSPSERN
Fairlight ESP Pty Ltd
Design by A.J.Cannon
Title
Static RAM
Size
B
Document Number
DSP-96K-01
REV
1
Date: October 20, 1992
Sheet 3 of 7


BACO..31]
BDCO..31]
RN3
4K7
U16
74AC652
RN4
U17
RN5
U18
RN6
U19
RN7
U20
74AC646
RN8
U21
RN9
U22
U23
74AC257
U24
U25
RN10
RN11
RN12B
RN12C
33R
JP4
JP5
GND
VCC
DMENB
*DDENB
DDCLK
DMCLK
*DACCF
BGRQ
*BWR
MMUX
*MWRT
BANK1
MA18
MA20
Note: JP4,5 installation:
connect 1-2 for 1M x 4 RAM
connect 2-3 for 256k x 4 RAM
Fairlight ESP Pty Ltd
Design by A.J.Cannon
Title
96K WRAM Interface
Size B
Document Number DSP-96K-01
REV 1
Date: October 20, 1992 Sheet 4 of 7


SCLK
U29
IN 25
50
75
100
125
150
175
200
225
250
S0A10251
SCLK
*MACC
U30
I1/CLK
22V10-15
DSPTGEN
VCC
RN15
4K7
MRAS
MCAS
MMUX
MCLK
DCLK
DLATCH
DSTRB
MDGATE
MCGATE
MMUX
MCLK
BWAC20..25]
U31
HCLK
*BWA20
*BWA21
*BWA22
*BWA23
*BWA24
*BWA25
*SW0
*SW1
*SW2
*SW3
*BWREF
HFMDEC
LWA0
LWA1
LWA2
LWA3
LWA4
LWA5
*BWUDS
*BWLDS
S1
SW DIP-4
GND
DSPWDEC
*BWREF
*BWUDS
*BWLDS
U60
HCLK
MDATE
MWRITE
MSTART
BWA1
*BWWRT
MCGATE
*MACC
*MDENH
*MDENL
*MSTAT
*MCTRL
*LWWRT
LWA1
DSPWACC
BWA1
*BWWRT
U32
CLK96
*MCTRL
*LWWRT
LWA0
LWA1
*SYNRES
*ONRST
*DCTRL
BGRQ
BA0
BA1
*LHIRQ
*IRQB
*IRQC
*RESET
HIRQ
DSPCTRL
BA0..31]
*SYNRES
*ONRST
BA0..31]
U33
*MWRT
BANK1
MRAS
MCAS
*DACC
*MACC
LWA0
LWA1
LWA10
I6V8-10
DSPWRAM
RN13 33R
RN14 33R
*CAS0
*CAS1
*RA0
*RA1
*RWRT
*MWRT
BANK1
RN16
4K7
VCC
*MACC
*MDENH
*MDENL
*MSTAT
*LWWRT
LWA1
*SENSE
U34A
*LHIRQ
*SENSE
*MSTAT
74AC244
HD15
HD14
HD13
HD12
HD0..15]
HD0..15]
U27
CLK96
DLATCH
DSTRB
*DACC
*DACCF
DMCLK
*DMEND
DDENB
DDCLK
DCTRL
*RQMEN
I2V8-10
DSPDACC
RN18
4K7
U26
*BTA
BGRQ
*DDENB
DDCLK
*RQMEN
.DSPDBUS
RN17
4K7
U28A
BGRQ
LBGRQ
74AC74
U28B
FGRQ
LFGRQ
DCLK
74AC74
Fairlight ESP Pty Ltd
Design by A.J.Cannon
Title
Waveform RAM & Interrupt Control Logic
Size
B
Document Number
DSP-96K-01
REV
1
Date: October 23, 1992
Sheet 5 of 7


HDC0..15]
HAC1..25]
CN1
Digital Edge Connector
HSCLK
HR*W
*HREF
*HVDS
*HLDS
*SYPES
*STRES
*WACC
WCLK
*WDENL
*WDENH
*WWRT
WIRQ
U36
U37
U38
74AC374
U34B
U35B
U35A
74AC244
U39
U40
U41
U42
74HC245
HAC0..22]
RDC0..31]
BHAC20..25]
Fairlight ESP Pty Ltd
Design by A.J.Cannon
Title
Waveform Bus Buffers
Size B
Document Number DSP-96K-01
REV 1
Date: October 20, 1992 Sheet 6 of 7



Fairlight ESP Pty Ltd		
Design by A.J.Cannon		
Title: Waveform RAM Bank 0,1		
Size: B	Document Number: DSP-96K-01	Rev: 1
Date: October 20, 1992	Sheet 7 of 7	