ESP-348

SAMPLER CARD

fairlight

FIELD CHANGE NOTICE

DATE 13/ 5 / 93

NUMBER 128

ORIGINATOR Chris Alfred **PRODUCT: CMI / MFX**

ASSEMBLY No. ESP-348 **DESCRIPTION** Sampler Card

This FCN applies to REV No: REV 1.7 **New REV No is:** REV 1.8

REASON FOR CHANGE:

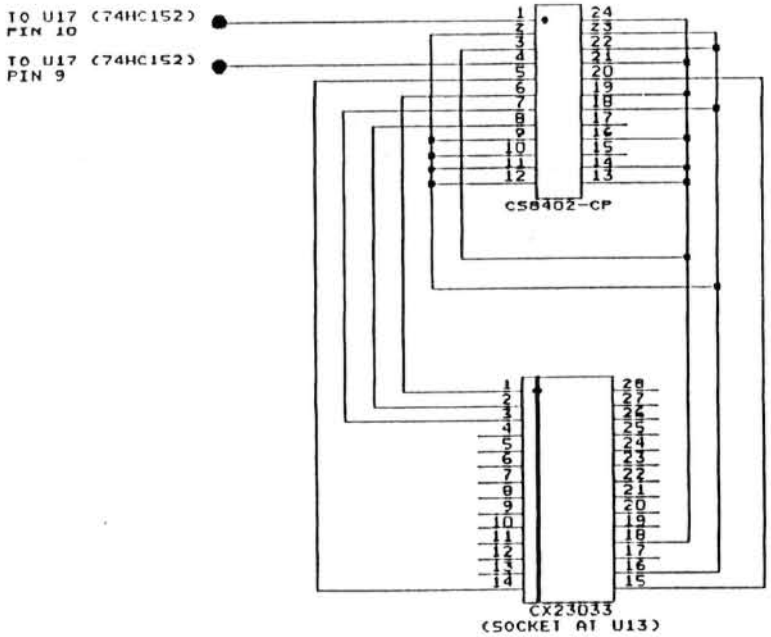
Due to the change in specifications of the AES / EBU standard the digital output chip used on the sampler is obsolete.

The addition of this new chip will output full AES with pro bit set and sample rate bit set.

DETAILS OF CHANGE:

1. Remove Sony chip from socket. (CX23033) at U13. Do not remove the socket.
2. Plug in ESP-350 AES adapter pcb assembly.
3. Wire pin 1 of the Crystal CS8402-CP to pin 10 U17 (74HC152).
4. Wire pin 4 of the Crystal CS8402-CP to pin 9 U17 (74HC152).
5. Cut track at U13 pin 3.
6. Wire U13 pin 3 to U6 pin 2.
7. Label board REV 1.8

ORIGINATOR:	DATE:	TEST:	DATE:
		PROD:	DATE:
SERVICE:	DATE:	KIT LIST CHANGE:	YES NO



Fairlight ESP 30 Bay St.,Broadway,2007 Designed:C.E.Alfred		
title AES REPLACEMENT WIRING DIAGRAM		
Size A	Document Number AESWIRE.SCH	REV 1
Date: April 7, 1993	Sheet 1 of 1	

fairlight

FIELD CHANGE NOTICE

DATE 3/ 5 / 93
NUMBER 125

ORIGINATOR Andrew Cannon **PRODUCT: CMI / MFX**

ASSEMBLY No. ESP-348 **DESCRIPTION** Sampler Card

This FCN applies to REV No: REV 1.6 **New REV No is:** REV 1.7

REASON FOR CHANGE:

1. To eliminate glitches when digital input is disconnected or not locked.

2. To allow up to 24dB gain on digital input.

3. Automatic sample rate conversion of 44K1 to 48K and vice versa on digital input.

NOTE that 2 and 3 require software revision 11.25 or higher with the "B" option on the Turbo SCSI card. For all previous revisions of software there is no operational change.

DETAILS OF CHANGE:

1. Remove ESP-348

2. Replace U24 (DSP 348 REV 3) with new EPROM, ESP-348 REV 6.

3. Relabel sampler for revision 1.7.

ORIGINATOR: AC DATE: 3-5-93	TEST: MP DATE: 13/5/93 PROD: DATE:
SERVICE: DATE:	KIT LIST CHANGE: YES NO

Fairlight ESP Pty Ltd
ESP-348 Sampler
Firmware Revision 6

30th April 1993
A.J.Cannon

Features

a) Audio Muting when digital input is not connected or not locked.
b) Up to +24dB gain on digital input.
c) Automatic conversion of 44k1 to 48k and vice versa on digital input.

Note that (b) and (c) require Rev 11.25B+ software.

Description

a) Whenever digital input is selected the "locked" status bit is continuously monitored. If the input becomes unlocked then the output is muted and remains so until the input has been locked for 200mS. If digital in is selected when no input is connected then the output remains muted until 200mS after a source is connected.

b) When digital input is selected the leftmost field of the input menu becomes a "gain" field, allowing up to 24dB of gain (in 1dB steps) to be applied to the digital input. This is useful when a digital source (eg DAT) has been recorded at a very low level throughout.
This feature should not be relied upon to compensate for over-conservative recording practices (ie leaving too much headroom) since the signal-to-noise ratio of the resulting audio will be degraded.
Digital input gain is only available with rev 11.25 or higher software with the "B" option installed.

c) When rev 11.25B or higher software is installed the sampler will detect the sample rate of the incoming digital source and automatically convert it to the sample rate of the MDR project. Thus 44k1 material from CD can be recorded directly into a 48k project, or a CD mastering project at 44k1 can include material from a 48k DAT recording.

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FIELD CHANGE NOTICE

DATE 26/ 10/ 92
NUMBER 111

ORIGINATOR Shane Morris **PRODUCT: CMI / MFX**

ASSEMBLY No. ESP-348 **DESCRIPTION** Sampler

This FCN applies to REV No: Rev 1.5 **The New REV No is:** Rev 1.6

REASON FOR CHANGE:

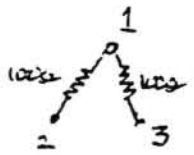
In some cases FCN -92 has caused poor digital lock for both input and output of the AES signal. Some cross talk to the audio inputs has also been noted.

DETAILS OF CHANGE:

1. Connect pin one of both the digital AES signal input and output connectors to the O volt of the PCB . CN 1 and at CN 2.

2. Leave the pin one of the XLR audio connectors attached to the frame of the module.

3. CONNECT 100Ω RESISTORS BETWEEN PIN 1 AND PIN 3, PIN 1 AND PIN 2 ON DIGITAL IN XLR ONLY.



ORIGINATOR: [signature]	DATE: 26/10/92	PROD: [signature]	DATE: 26/10/92
SERVICE:	DATE:	KIT LIST CHANGE: YES NO	

ESP

FIELD CHANGE NOTICE

Field Change Notice No 92

PRODUCT CMI Series III

ORIGINATOR: Shane Morris **DATE:** 10/ 6 / 92

ASSEMBLY No: ESP - 348

DESCRIPTION: Sampler module

This FCN applies to rev No: .4 / 1.4 **The New rev No is:** .5 / 1.5

REASONS FOR CHANGE:

It has been noted that outside ground glitches effect the correct performance of the sampler module. Symptoms include loosing lock and playing "phantom" sounds.

DETAILS OF CHANGE:

1. Remove wires connected to the XLR pin 1's. Also remove these wires from the P.C.B. For the AES input the 100 ohm resistors must remain connected to the XLR pin 1.
2. Connect AES input XLR pin 1 to AES output pin 1 and then to the module chassis via a solder lug.
3. Connect the audio input XLR pin 1's to each other and then to the module chassis via a solder lug.
4. Make sure that no connection is made from anywhere on the pcb to the chassis of the module use thin plastic washers.

Colour code is: Pin 1 green, Pin 2 red, Pin 3 black. CN1 [1 2 3] PCB.

Make sure, **very important,** that the module chassis / frame is connected to the frame of the machine when the module is inserted into it's slot.

USER NOTE: When using SPDIF signals in or out of this module connect pins 1 & 3 together in the XLR cable connector and use pin 2 for signal and pin 1 for the shield connection.

SPDIF and AES signals are different both in level and impedances. SPDIF will not run with long cables so caution is advised.

DEPT	SIGNATURE	DATE	COMMENTS
Project Manager			
Customer Service			

ESP

FIELD CHANGE NOTICE

Field Change Notice No 90

PRODUCT CMI Series III

ORIGINATOR: Chris Alfred **DATE:** 3 / 6 / 92

ASSEMBLY No: ESP348

DESCRIPTION: Digital Sampling Card

This FCN applies to rev No: 0.3 / 1.3 **The New rev No is:** 0.4 / 1.4

REASONS FOR CHANGE:

Terminate sampler interface to remove glitches.
This stops clicks during sampling.

DETAILS OF CHANGE:

1. Connect a 470R resistor between Q2 emitter and Q2 collector.
2. Connect a 470R resistor between Q4 emitter and Q4 collector.
3. Connect a 470R resistor between Q6 emitter and Q6 collector.
4. Mark the PCB as Rev 0.4 or Rev 1.4.

NOTE: to be done in conjunction with FCN91

DEPT	SIGNATURE	DATE	COMMENTS
Project Manager			
Customer Service			

ESP

FIELD CHANGE NOTICE

Field Change Notice No 84

PRODUCT CMI Series III

ORIGINATOR: Andrew Cannon **DATE:** 5 / 3 / 92

ASSEMBLY No: ESP-348

DESCRIPTION: Digital Sampling Card

This FCN applies to rev No: 1.2 **The New rev No is:** 1.3

REASONS FOR CHANGE:

To improve operation of current loop from sampler to WS by increasing the driving current. This removes clicks during recording caused by false detection of the rising edge of the EOC signal on the WS.

DETAILS OF CHANGE:

Change the three 680R resistors added in FCN 75 from the 7407 to the edge connector to 330R.

DEPT	SIGNATURE	DATE	COMMENTS
Project Manager			
Customer Service			

ESP

FIELD CHANGE NOTICE

Field Change Notice No 83

PRODUCT CMI Series III

ORIGINATOR: Andrew Cannon **DATE:** 5 / 4 / 92

ASSEMBLY No: ESP-348 rev 0 (with gold overlay)

DESCRIPTION: Digital Sampling Card

This FCN applies to rev No: 0.1 **The New rev No is:** 0.2

REASONS FOR CHANGE:

To allow the old revision sample card to be used with a Waveform Supervisor (CMI-41) which has been modified according to FCN 77. This also results in improved operation of the link between the sampler and WS.
Note that this FCN does not bring the rev 0 sampler up to the same level as the ESP-348 rev 1.x.

*** this FCN is to be done in conjunction with FCN 77 ***

DETAILS OF CHANGE:

1. Remove BC558 transistors Q1, Q2, Q3, Q4, Q5 and Q6.
2. On the wiring side, cut wide track to pins A9 & A10 of the edge connector.
3. Add a 7407 IC as follows: Bend all pins except 7 and 14 out and cut short. Solder pins 7 and 14 to pins 7 and 14 respectively of U6 (74HC04).
4. Connect pin 9 of the 7407 to pin 7 of U23 (74HC244)
5. Connect pin 11 of the 7407 to pin 5 of U23
6. Connect pin 13 of the 7407 to pin 3 of U23
7. Connect pins B9,B10 (component side) of the edge connector to Q6 emitter (this track goes to emitters of Q1-Q6 & +ve terminal of 47uF electro cap, and is the output of the 7805)
8. Solder a 330R resistor to pin 8 of the 7407 and connect the other end to pin A11 of the edge connector (collector of Q2).
9. Solder a 330R resistor to pin 10 of the 7407 and connect the other end to pin A12 of the edge connector (collector of Q4).
10. Solder a 330R resistor to pin 12 of the 7407 and connect the other end to pin A13 of the edge connector (collector of Q6).

DEPT	SIGNATURE	DATE	COMMENTS
Project Manager			
Customer Service			

ESP

FIELD CHANGE NOTICE

Field Change Notice No 82

PRODUCT CMI [X] CVI [ ]

ORIGINATOR: Chris Alfred **DATE:** 20 / 2 / 92

ASSEMBLY No: ESP 349

DESCRIPTION: Sampler Analog Card

This FCN applies to rev No: 1.2 **The New rev No is:** 1.3

REASONS FOR CHANGE:
Correct input gain to ensure +4dBu (1.228Vrms sinewave at 1kHz) displays -10dB on the level meters.

DETAILS OF CHANGE:
Replace the 14k2 1% resistors at locations R23,R24,R34,R35 with 7k5 1% resistors

DEPT	SIGNATURE	DATE	COMMENTS
Project Manager	C Alfred	24-2-92	
Customer Service		24.2.92	

ESP

FIELD CHANGE NOTICE

Field Change Notice No 81

PRODUCT CMI [X] CVI [ ]

ORIGINATOR: Mario Paolino **DATE:** 12 / 11 / 91

ASSEMBLY No: ESP 349

DESCRIPTION: Analog Sampling Card (top board)

This FCN applies to rev No: 1.1 **The New rev No is:** 1.2

REASONS FOR CHANGE:

To increase the analog input sensitivity such that a signal of +4dbm corresponds to a reading of 10dbm on the sample page meters.

DETAILS OF CHANGE:

1) For Sample cards which have the Digital and Analog boards joined by a ribbon cable.
Resistors R23 & R24 and R34 & R35 original value was 2k new value is 14.3k 1%
See attached overlay.

2) For Sample cards which have the Digital and Analog boards joined by a connector set.
Resistors R24 & R25 and R34 & R35 original value was 2k new value is 14.3k 1%
See attached overlay.

DEPT	SIGNATURE	DATE	COMMENTS
Project Manager			
Customer Service			

ESP

FIELD CHANGE NOTICE

Field Change Notice No 76A

PRODUCT CMI [X] CVI [ ]

ORIGINATOR: Robert Stapldon **DATE:** 24 / 12 / 91

ASSEMBLY No: ESP349

DESCRIPTION: Sampler Analog

This FCN applies to rev No: 1 **The New rev No is:** 1.1

REASONS FOR CHANGE:

To eliminate VCO cross talk into the analog sampling circuit, the VCO is shut down when sampling in analog.

** This FCN is to be done in conjunction with FCN 75 **

DETAILS OF CHANGE:

1. Remove Relay RL2
2. Link the pins of RL2 (as shown)
3. Remove diode D2 and replace it with a wire link.
4. Desolder the collector of transistor Q3 & lift this leg out of the hole.
5. Join the lifted collector of Q3 to Ic U1 (74HC04) Pin 1.

DEPT	SIGNATURE	DATE	COMMENTS
Project Manager			
Customer Service			

ESP

FIELD CHANGE NOTICE

Field Change Notice No 75

PRODUCT CMI Series III

ORIGINATOR: Chris Alfred **DATE:** 9 / 7 / 91

ASSEMBLY No: ESP348

DESCRIPTION: Digital Sampling Card

For rev Ø sampler (with Gold Overlay) refer FCN 83.

This FCN applies to rev No: 1.1 **The New rev No is:** 1.2

REASONS FOR CHANGE:

Sampler signals to the WS are now driven by open collector buffers instead of the current mirrors. To achieve a smoother switching in the HP2631 opto isolators. on the WS card.

* refer FCN 84.

** This FCN is to be done in conjunction with FCN 76 ** & 77

DETAILS OF CHANGE:

Modifications to ESP-348 Sampler

1. Remove transistors Q1, Q2, Q3, Q4, Q5,Q6.
2. On the component side - cut track going to edge connector fingers B9,B10.
3. On the wiring side - cut track going to edge connector fingers A9,A10.
4. Obtain an Ic 7407 & bend out all pins except 7 and 14.
5. Solder the 7407 on top of U37 (74HC04) soldering 7407/7 to U37/7; and 7407/14 to U37/14.
6. On the component side - Connect 7407/13 to U23/3 (74HC244).
7. On the component side - Connect 7407/11 to U23/5 (74HC244).
8. On the component side - Connect 7407/9 to U23/7 (74HC244).
9. On the component side - Connect 680R resistor from Ic 7407/12 to the collector of Q6. } *
10. On the component side - Connect 680R resistor from Ic 407/10 to the collector of Q4. } *
11. On the component side - Connect 680R resistor from Ic 7407/8 to the collector of Q2. } *
12. On the wiring side - Connect Q2 emitter (BC558) to edge connecter fingers A9 and A10. (Q2 emitter is the pin connected to U33-7805).

DEPT	SIGNATURE	DATE	COMMENTS
Project Manager			
Customer Service			

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FIELD CHANGE NOTICE

DATE 14/ 2 /91
NUMBER 68

ORIGINATOR Mario Paolino **PRODUCT: CMI / MFX**

ASSEMBLY No. ESP-348 **DESCRIPTION** Digital Sampler

This FCN applies to REV No: REV 1 **The New REV No is:** REV 1.1

REASON FOR CHANGE:
To enable digital out.

The watchdog IC DS1232 is currently connected directly to the DSP monitoring the signal SDATAO. The change is to monitor the signal 17 clocks.
There is also a ROM and PAL update which can be obtained from FAIRLIGHT.

DETAILS OF CHANGE:

1) on component side - Cut track going to IC U12 (DS1232) pin 7.

2) Join U12 pin 7 to the nearby feed through hole as shown on overlay.

ORIGINATOR: **DATE:**

SERVICE MANAGER: **DATE:**

fairlight ORIGINAL

FIELD CHANGE NOTICE

DATE 14/ 2 /91
NUMBER 67

ORIGINATOR Mario Paolino **PRODUCT: CMI / MFX**

ASSEMBLY No. ESP-348 **DESCRIPTION** Digital Sampler

This FCN applies to REV No: Unmarked **The New REV No is:** .1

REASON FOR CHANGE:
To enable digital out.

The watchdog IC DS 1232 is currently connected directly to the DSP monitoring the signal SDATAO. The change is to monitor the signal 17 clocks.
There is also a ROM and PAL update which can be obtained from FAIRLIGHT.

DETAILS OF CHANGE:

1) Locate & remove the mod wire connected to IC U12 (DS1232) pin 7- going to the DSP.
2) Join U12 pin 7 (the IC pin itself) to U5 (74HC02) pin 1.
3) The ROM should be changed to DSP 348 REV 2
4) The PAL at U9 should be changed to ESP 348-2
5) Mark this board REV0.1

ORIGINATOR: **DATE:**

SERVICE MANAGER: **DATE:**

ESP

FIELD CHANGE NOTICE

Field Change Notice No: 63

PRODUCT CMI [X] CVI [ ]

ORIGINATOR: Mario Paolino **DATE:** 27 / 11 / 90

ASSEMBLY No: ESP 349

DESCRIPTION: Analog Sampling Card (top board)

This FCN applies to rev No: 1 **The New rev No is:** 1.1

REASONS FOR CHANGE:

To increase the analog input sensitivity such that a signal of +4dbm corresponds to a full scale reading on the sample page meters.

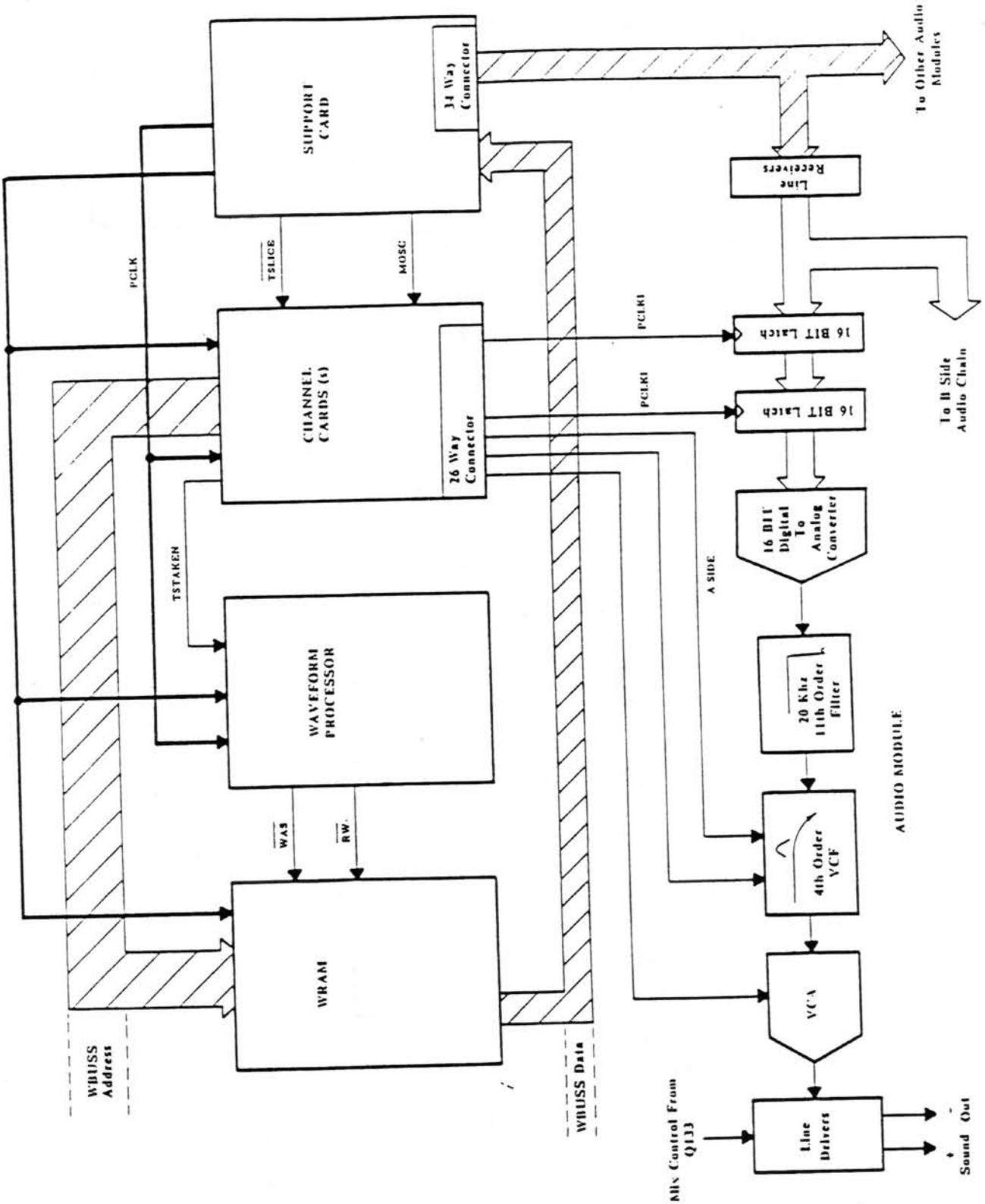
DETAILS OF CHANGE:

1) For Sample cards which have the Digital and Analog boards joined by a ribbon cable.
Resistors R23 & R24 and R34 & R35 original value was 10k new value is 2.0k 1%
See attached overlay.

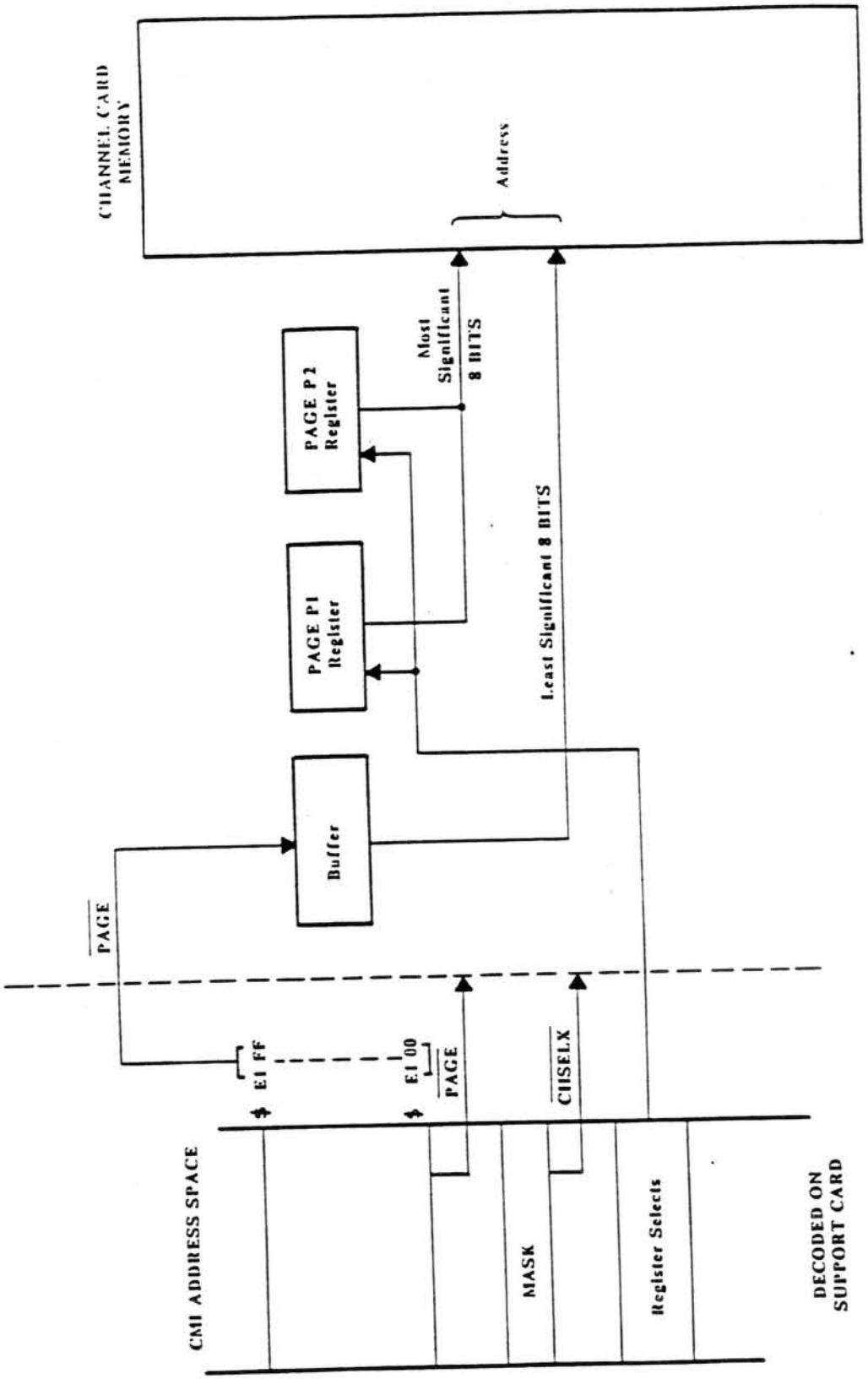
2) For Sample cards which have the Digital and Analog boards joined by a connector set.
Resistors R24 & R25 and R34 & R35 original value was 10k new value is 2.0k 1%
See attached overlay.

DEPT	SIGNATURE	DATE	COMMENTS
Project Manager	Mario Paolino	27/11/90	
Customer Service	Mario Paolino		

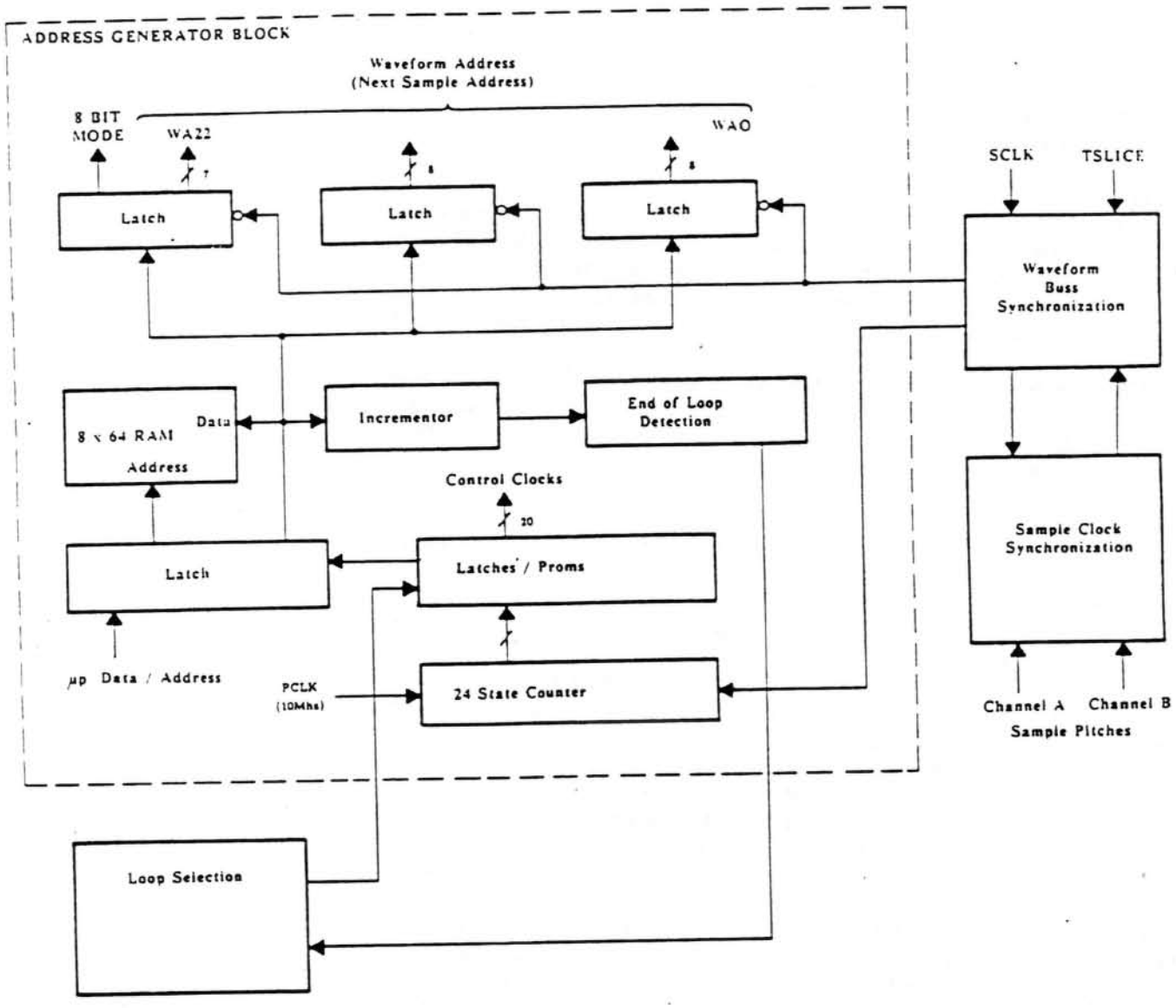
Important Modules during Sound Playing



Memory Access Block Diagram



Address Generator Block Diagram



Terminology
WP: Waveform Processor
GIC: General Interface Card
WBuss: Waveform Buss
WRAM: Waveform RAM (2M - 14Mbytes)
CC: Channel Card
CCP: Channel Card Processor
CSC: Channel Support Card
CPU: Dual 6809 processor system running OS9.
Hexidecimal numbers are in the form nnnnnnH.
Active low signal names are preceded by a "/" character

Introduction

The Channel Card (CC) provides the sample addresses, sample clocks and control voltages used in outputing data to the Audio Modules and controlling the resulting audio waveforms amplitude and high frequency content. It carries on these functions as a self contained computer, once instructed what functions to perform by the WP, GIC or CPU.

The CC can be divided into 2 main sections. The control of the 6809 and its memory by the main CPUs through the CPU buss interface, and the on board 6809s I/O, which generates signals for the WBUSS and the Audio Rack.

Channel Control

The CC contains a 2MHz 68B09E and 64K of dynamic ram. To the main CPUs it looks like a block of 16 registers and two pages of 256 bytes of memory, mapped into its peripheral space.

The generation of the CC select signals occurs on the CMI-32, Channel Support Card (CSC).

The CCs registers allow the main CPUs to reset and interrupt the on board 68B09E and select which two pages of memory are mapped into the main CPUs address space.

All accesses to the CCs registers and memory are made transparently to the Channel Card Processor (CCP) by cycle stealing. This allows the fastest update of control parameters with the minimum overhead.

Refresh also steals one cycle every 16 microseconds from the CCP.

Channel Card Peripherals

The CCP initializes and controls the sample address and clock generating hardware collectively referred to as the Address Generator (ADDGEN). It also addresses 6 DACs used to generate control voltages used in the control of the Voltage Controlled Filters (VCF) and the Voltage Controlled Amplifiers (VCA) on the Audio Modules.

Waveform Buss Interface.

CCs are allowed access to the WBUSS in a "round robin" buss sharing scheme. The CCs internally share their WBUSS grant between the two audio channels contained on each CC.

The ADDGEN is granted access to the WBUSS via the CSCs buss arbitration signal, $\overline{\text{TSLICE}}$. During active CC WBUSS cycles, the WP is informed via $\overline{\text{TSTAKEN}}$ that it or refresh cannot access the WBUSS.

Processor, Address Registers and Multipexers

(refer schematic CMI-31-01)

The CPU's data buss is buffered at A6 to form the internal Memory Data Buss (MDB). The CCPs data buss is connected to the MDB via bidirectional buffer B8. All onboard RAM access occurs via the MDB. B8 is only disabled during CC access by external CPUs, during ram refresh and when the CCP accesses the ADDGEN and DACs. The buss between B8 and the CCP is the peripheral buss (PB) and is where the DACs and ADDGEN are connected. External CPU data cannot get onto the PB from the MDB, and hence control the ADDGEN.

The MDB also connects to the octal latches at A8 and A7 which are the PAGE registers used in external access to the CC's RAM. Latch A7 contains the page address for P1, A8 for P2.

The addresses from the CCP, via buffers B6 and B7, the page registers, and buffer B5 (connected to the least significant 8 bits of the dual CPU buss) all connect together to form the 8 bit address buss for the dynamic RAMs.

During refresh cycles, the least significant 7 bits of the CPU address buss contain the contents of the refresh counter from the CMI-133. During CC memory accesses by external CPUs, the least significant 8 bits of the CMI address buss contains the address within the page to be accessed. The Buffer B5 is enabled during these memory cycles to form the row address for the RAMs.

When the CC is accessed, the two card select control signals, $\overline{\text{CHSEL}}$ and $\overline{\text{PAGE}}$ become active. The channel select is buffered and ANDed with the refresh signal in D9, which in turn is ANDed with the externally generated E and Q to feed the CCP. During refresh and external accesses, the CCP has its clock stopped (D9 pin 11 low), allowing a memory cycle for refreshing and updating of memory or registers.

Address Decoding

(refer schematic CMI-31-02)

The CCs control registers are decoded from the CPU buss by 1 of 8 decoder C3. It is enabled when the channels $\overline{\text{CHSEL}}$ is low and $\overline{\text{PAGE}}$ is high. From this decoder the external CPU can read the channels run status, reset the CCP, write to the PAGE registers and interrupt the CCP. The CCP loses one cycle for each access.

The LS133 at C6 decodes the CCP address buss to define the ADDGEN and DAC I/O locations.

The CCPs I/O is decoded in 2 64 byte blocks starting at FE80H. The first block contains the control latch, pitch registers, CCPs interupt status register, real time clock acknowledge and DACs. The second decodes the ADDGEN registers.

Whenever these I/O loactions are accessed, pin 9 of C6 will go low and disable the CCP's MDB transiever.

Channel B Pitch and Card Status Register

(refer schematic CMI-31-03)

The latches at E5 and E6 contain the pitch for the B audio channel. There are 3 bits to select which octave and 12 bits to select the pitch within the octave. The pitch within the octave bits feed Rate Multipliers at F6 and F5.

The Rate multipliers are clocked at 17.14 MHz. The output of this chain is pin 6 of F6. This is a train of pulses with an average frequency of the required pitch, but in a much higher octave. This clock has considerable jitter as the rate multipliers effectively drop clock pulses from the 17.14 MHz stream to change frequency.

This clock feeds a binary counter E3 that generates the clocks for 8 octaves, at 16 times the required sample rate. The 1 of 8 selector E4 uses the octave select bits to select the appropriate output of E3.

The selector feeds a divide by 16 counter which acts as a jitter filter, to average out the periods of the sample clock, to reduce distortion in the output waveform.

The output of the jitter filter, E9, is ANDed with the RUNB control signal to generate the sample clock for channel B.

The 4 bit latch and buffer at B11 and A11, are used by the external CPUs to determine the current status of the channel card. The upper 4 bits of this register allow the external CPUs to determine if an interrupt came from this channel card, that the CCP is reset, and if either of the two audio channels controlled by this card are currently being used.

The least significant 4 bits allow the CCP to send 4 bit status codes to the external CPUs.

Channel A Pitch and the control registers

(refer schematic CMI-31-04)

The pitch generation for channel A is identical to Channel B but uses the components at E8, E7, F8, F7, D6, D5 and E9.
The main pitch oscillator is bussed from the CSC as a differenti-al line. This is received at A9 by a 26LS32. This receiver then drives the two channels of pitch generating ratemultipliers.

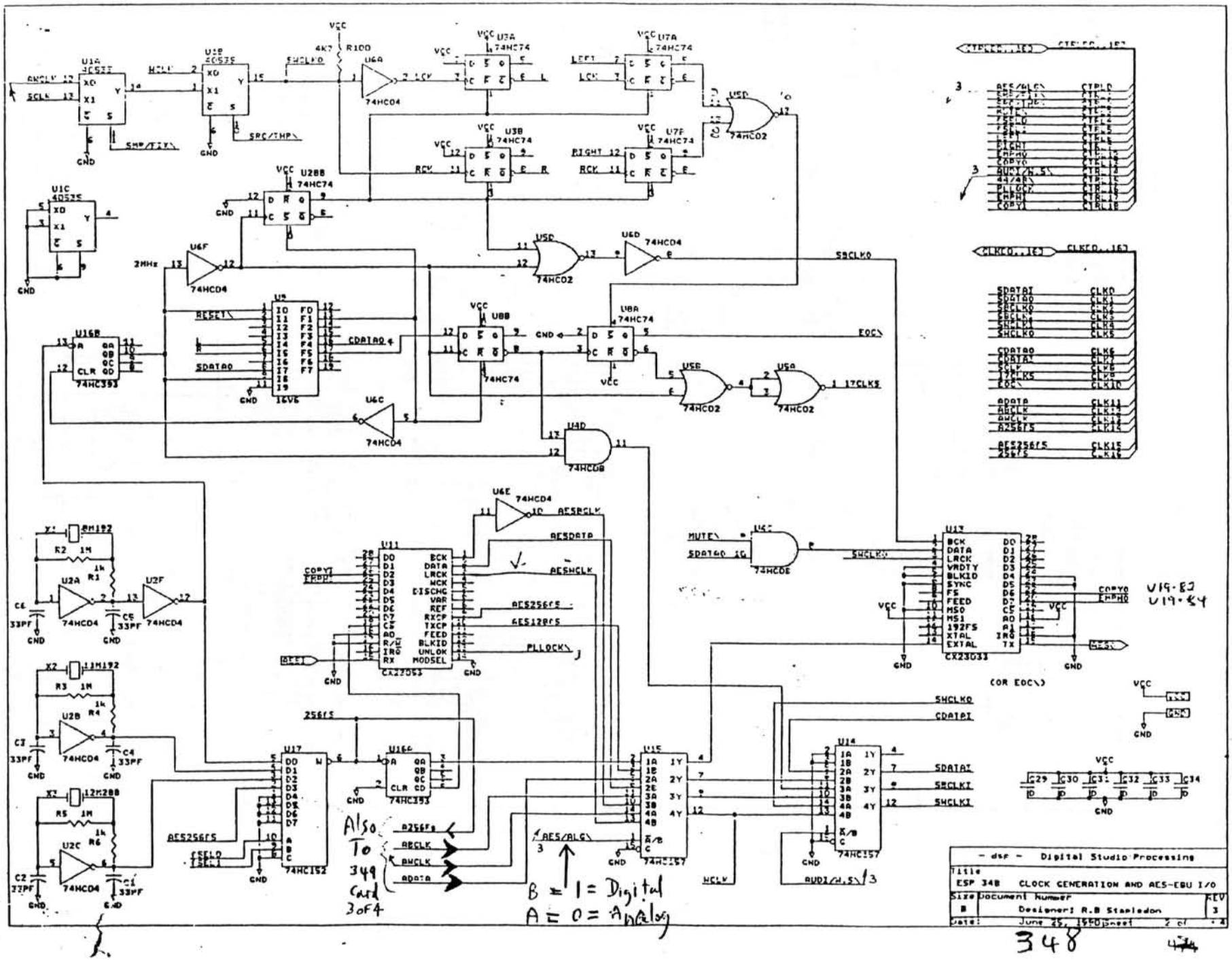
The control latch is located at C10. This octal latch outputs all the control lines to control, channel running, zippa filter time constant, enabling of end of loop interupts and selection of the ADDGENs loops. It is reset when the CMI is turned on to stop the channels running, and making any sound before they are initialized.

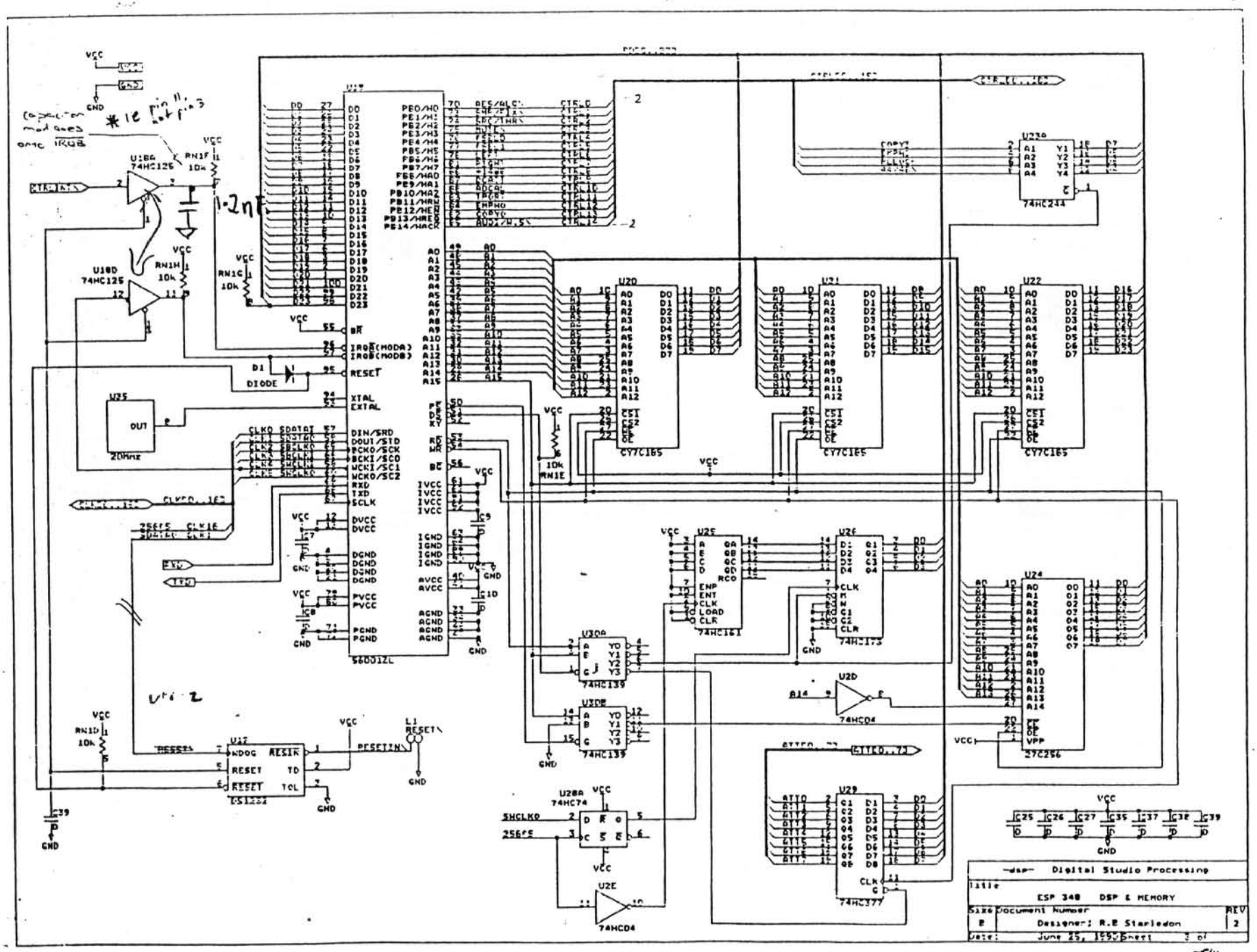
The F/F at D2 is used to control the $\overline{\text{RESET}}$ input of the CCP. It can only be written to by external CPUs and is reset, the CCP stopped, at power on.

Control Voltage Generation

(refer schematic CMI-31-05)

The Control Voltage DACs all use a precision 10.000V source as their voltage reference. The +15V, -15V and analog ground (AGND) are cabled to the CCs via 26 way flat cables. There is no connection between the CCs digital ground DGND and AGND on the CC. They are connected together in the Audio Rack. The back to back diodes


- dsp - Digital Studio Processing
Title
ESP 348 CLOCK GENERATION AND AES-EBU I/O
Size B
Document Number
REV 3
Designer: R.B Stapledon
Date: June 25, 1990
Sheet 2 of 4
Also To 349 Card 3 of 4
B = 1 = Digital
A = 0 = Analog
(OR EOC\)
348


Digital Studio Processing
ESP 348 DSP & MEMORY
Designer: R.B Stapledon
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74HC244
CY7C185
74HC161
74HC173
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74HC74
74HC377
27C256
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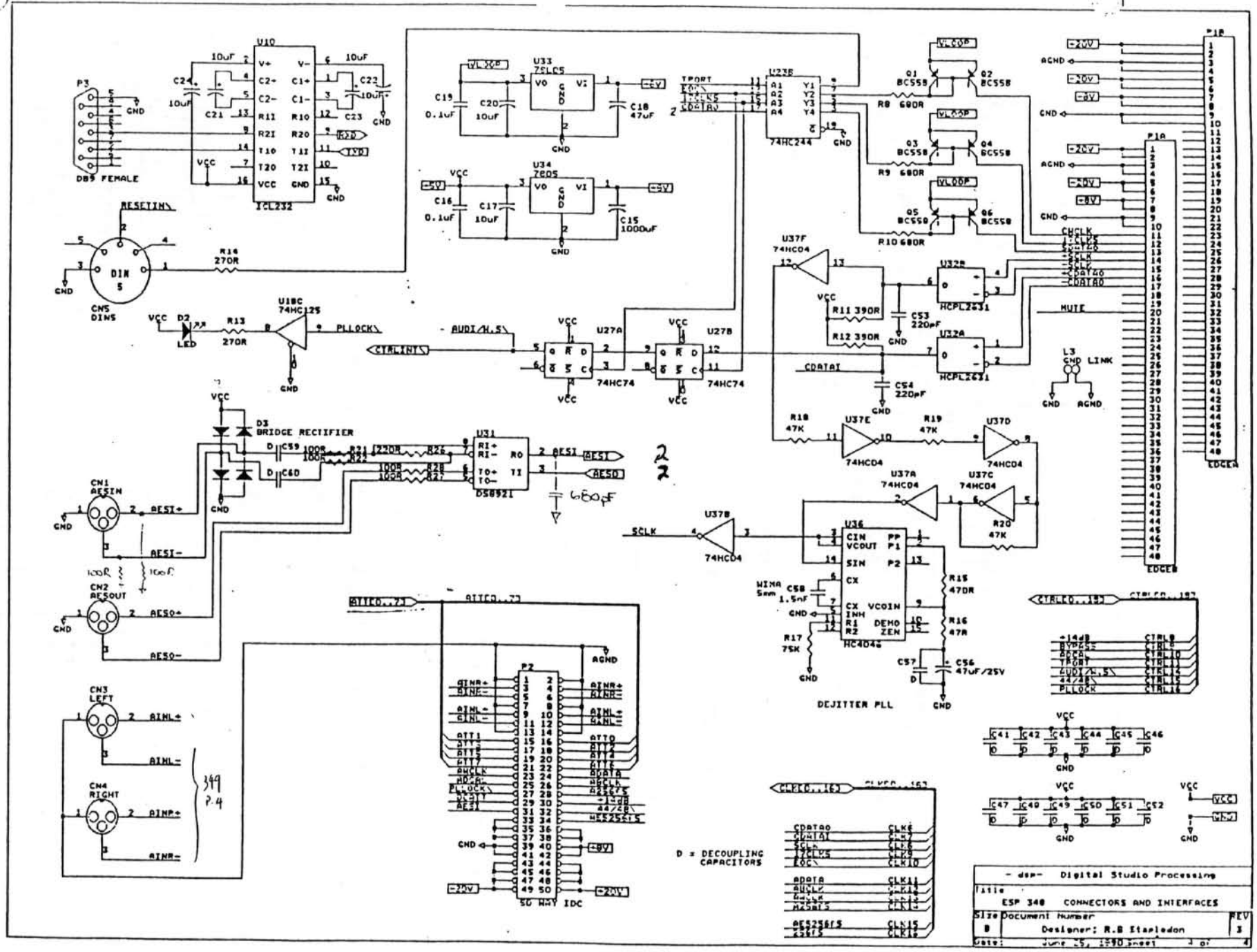
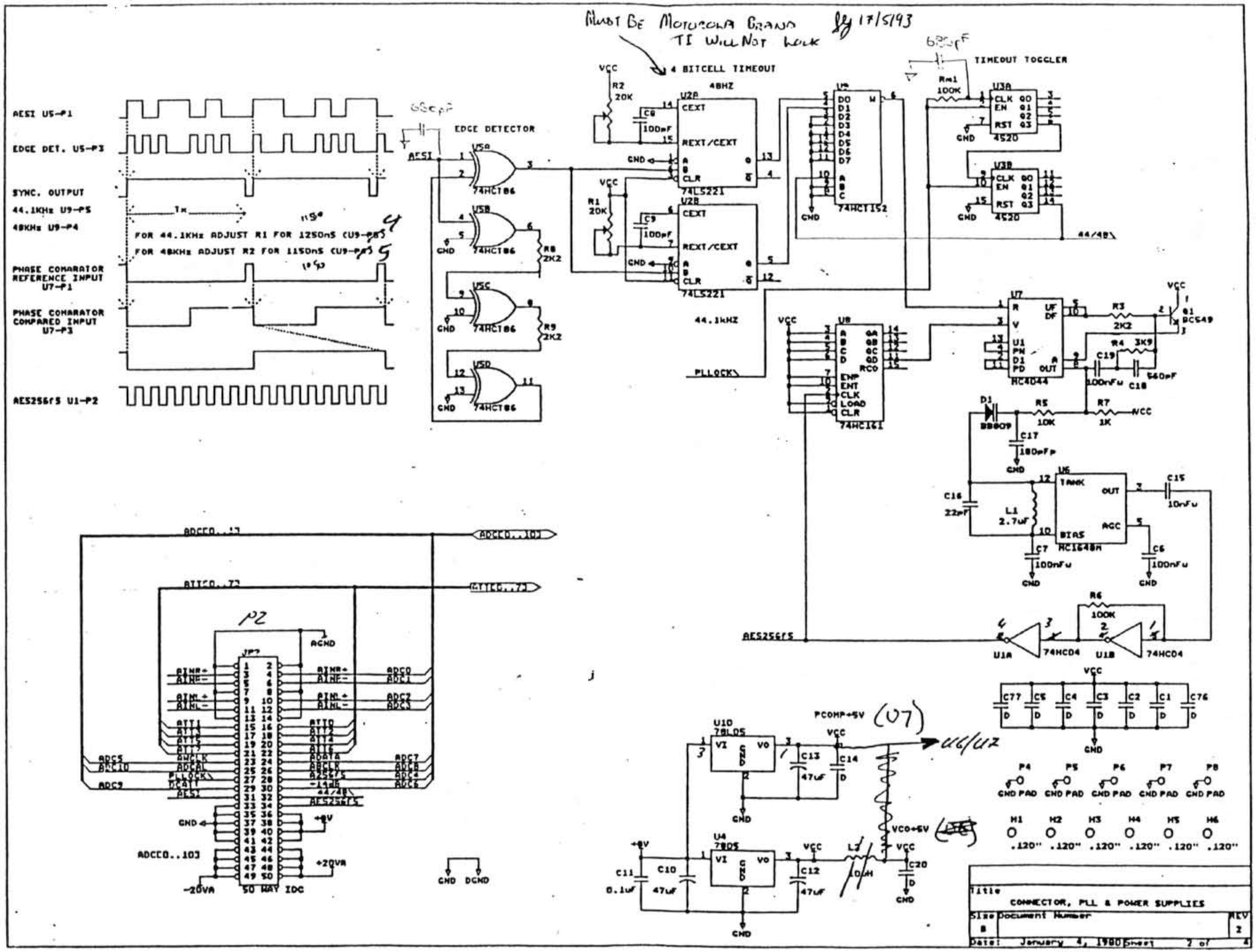
1.2nF
10k
DIODE
RESET
VCC
GND

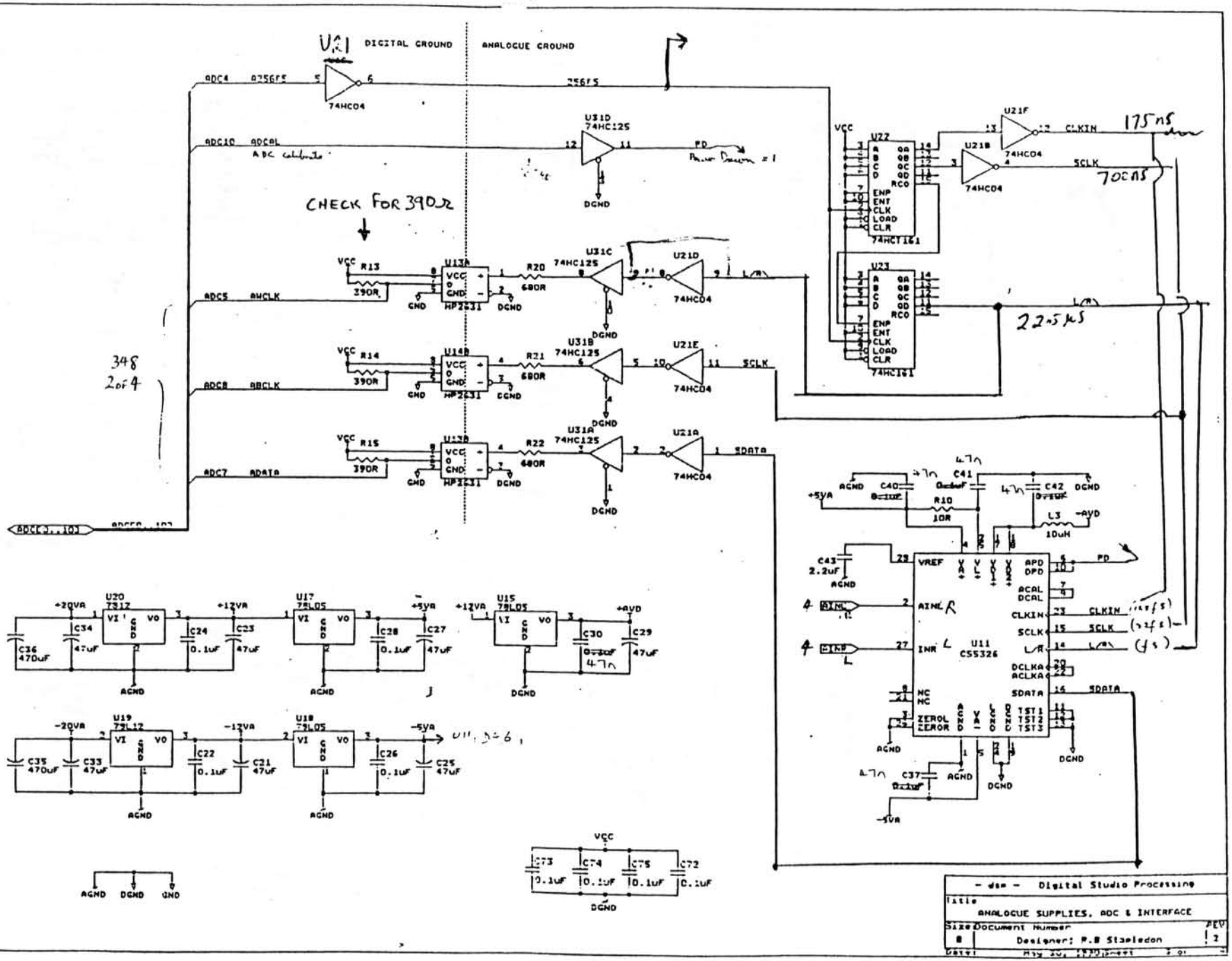

DB9 FEMALE
ICL232
DIN 5
CN5 DIN5
LED
BRIDGE RECTIFIER
DS8921
CN1 AESIN
CN2 AESOUT
CN3 LEFT
CN4 RIGHT
50 WAY IDC
74HC74
74HC244
74HCO4
HCPL2631
HC4046
DEJITTER PLL
D = DECOUPLING CAPACITORS
- dsp- Digital Studio Processing
ESP 348 CONNECTORS AND INTERFACES
Designer: R.B Stapledon

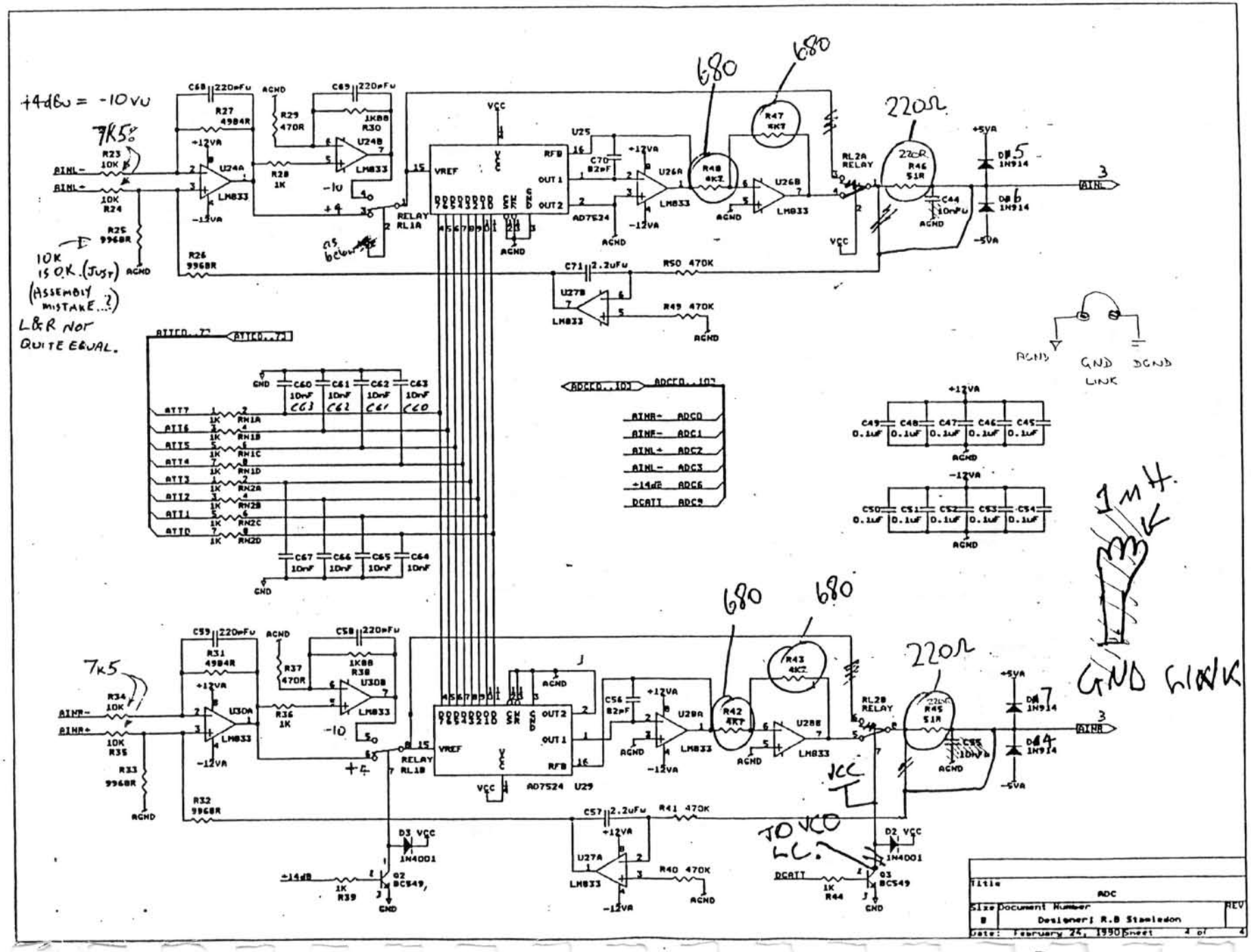
348



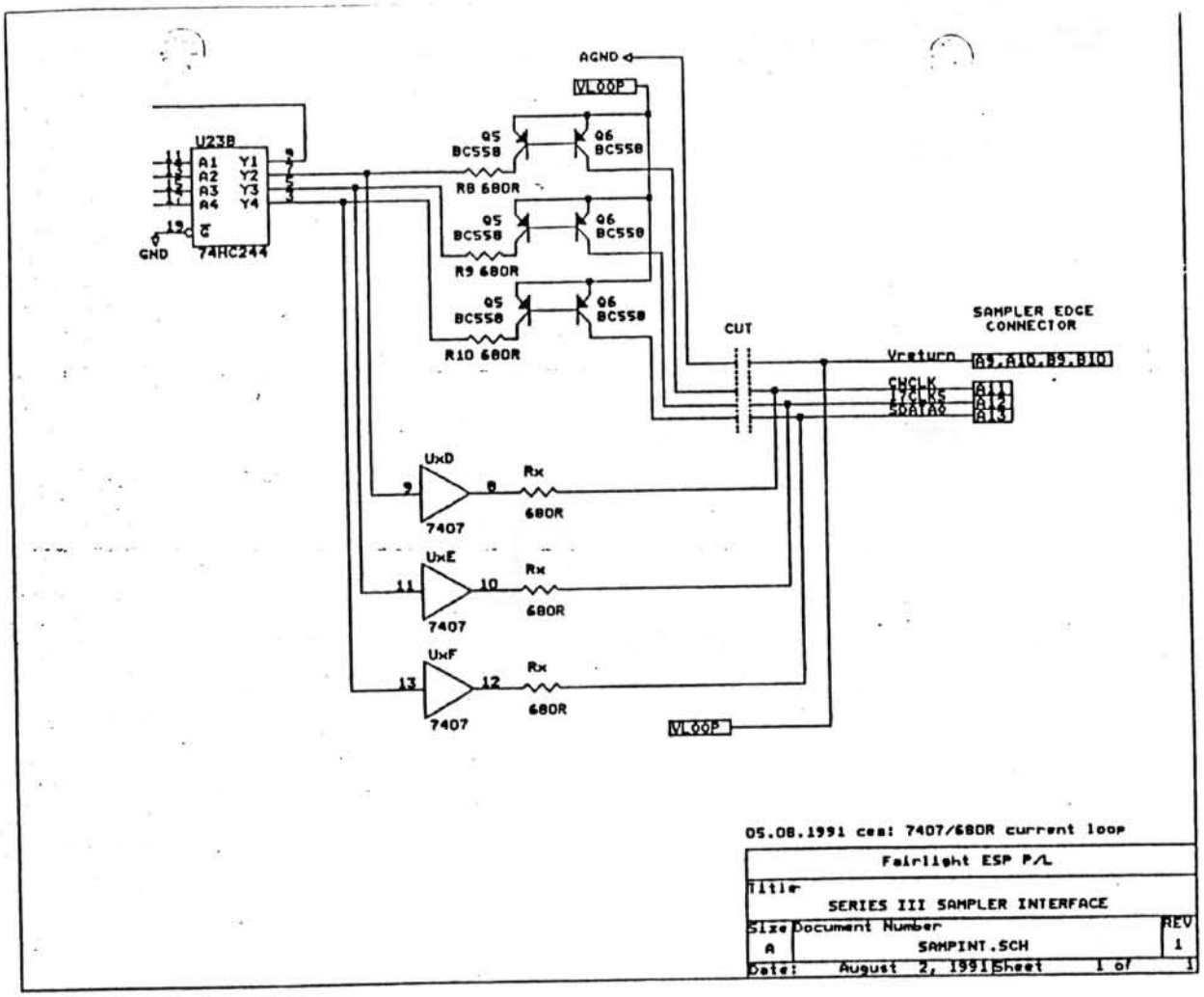
Must Be Motorola Brand TI Will Not Lock
17/5/93
4 BITCELL TIMEOUT
TIMEOUT TOGGLER
EDGE DETECTOR
AESI U5-P1
EDGE DET. U5-P3
SYNC. OUTPUT
44.1KHz U9-P5
48KHz U9-P4
FOR 44.1KHz ADJUST R1 FOR 1250nS (U9-P5)
FOR 48KHz ADJUST R2 FOR 1150nS (U9-P4)
PHASE COMARATOR REFERENCE INPUT U7-P1
PHASE COMARATOR COMPARED INPUT U7-P3
AES256fS U1-P2
74HCT86
74LS221
74HCT152
4520
74HC161
MC4044
MC1648M
74HC04
BC549
BB809
78LDS
78DS
48KHZ
44.1kHZ
PLLOCK
AES256fS
44/48
ADCD0..103
ATTD0..7
P2
50 WAY IDC
PCOMP+5V
(U7)
U6/U2
VCO+5V
GND PAD
.120"
Title
CONNECTOR, PLL & POWER SUPPLIES
Size B
Document Number
REV 2
Date: January 4, 1980
Sheet 2 of 4

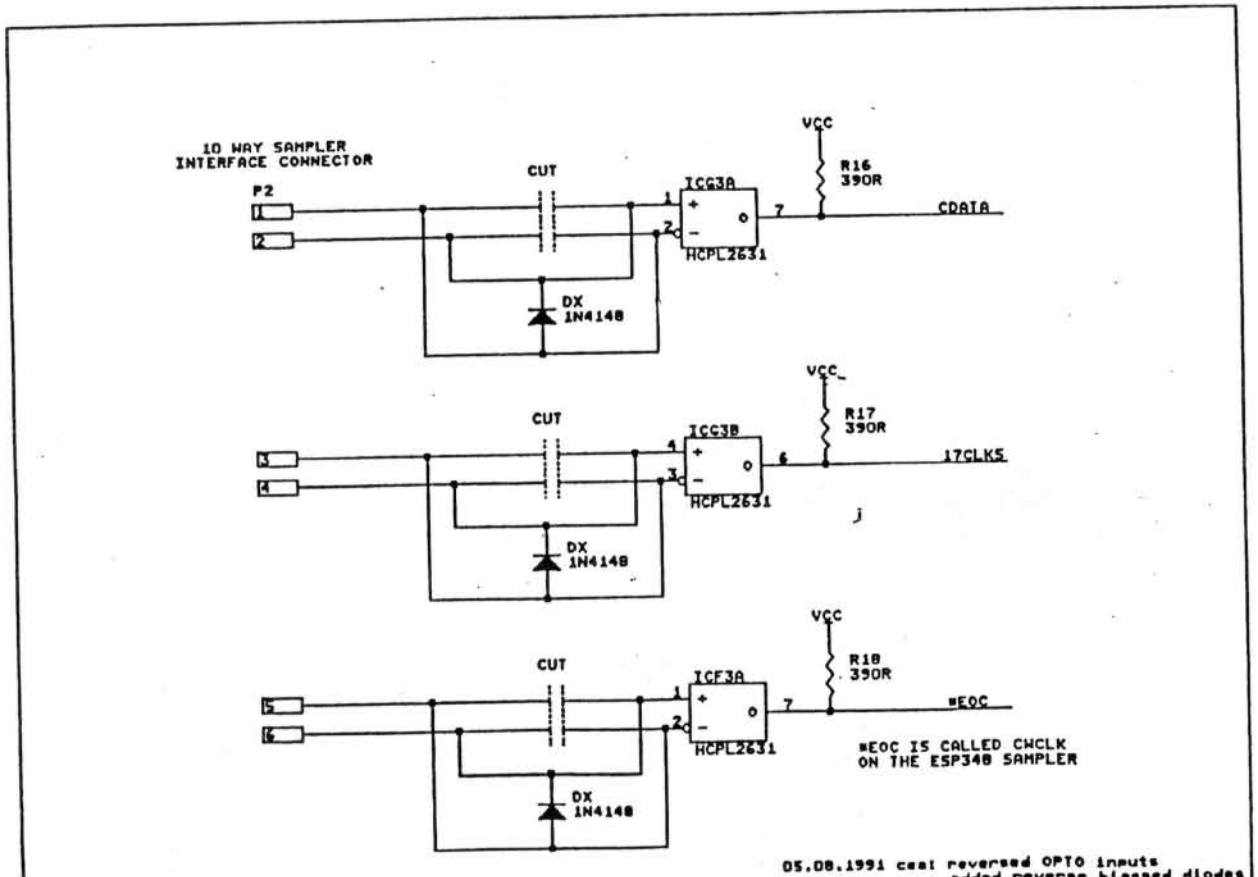
21-9 2 of 4


DIGITAL GROUND
ANALOGUE GROUND
74HC04
74HC125
74HCT161
HP2631
CHECK FOR 390Ω
390R
680R
10R
10uH
2.2uF
47uF
470uF
0.1uF
CS5326
AGND
DGND
SCLK
SDATA
CLKIN
175nS
70nS
22.5µS
348
2 of 4
349
3 of 4
- dsm - Digital Studio Processing
ANALOGUE SUPPLIES, ADC & INTERFACE



Title	ADC	
Size: B	Document Number	REV
Date: February 24, 1990	Designer: R.B Stapleton Sheet 4 of 4	


AGND
VLOOP
U23B
A1
A2
A3
A4
Y1
Y2
Y3
Y4
GND
74HC244
Q5
BC558
Q6
BC558
R8 680R
R9 680R
R10 680R
CUT
SAMPLER EDGE
CONNECTOR
Vreturn
A9,A10,B9,B10
CHCLK
17CLKS
SDATAO
A11
A12
A13
UxD
UxE
UxF
Rx
680R
7407
VLOOP
05.08.1991 ces: 7407/680R current loop
Fairlight ESP P/L
Title
SERIES III SAMPLER INTERFACE
Size
A
Document Number
SAMPINT.SCH
REV
1
Date: August 2, 1991
Sheet 1 of 1


10 WAY SAMPLER
INTERFACE CONNECTOR
P2
CUT
ICG3A
HCPL2631
VCC
R16
390R
CDATA
DX
1N4148
ICG3B
HCPL2631
R17
390R
17CLK5
ICF3A
HCPL2631
R18
390R
*EOC
*EOC IS CALLED CHCLK
ON THE ESP348 SAMPLER
05.08.1991 ceal reversed OPTO inputs
added reverse biassed diodes
Fairlight ESP P/L
Title