

CMI-35

DIGITAL MOTHER BOARD



StarNight

Page 1 of 1

FIELD CHANGE NOTICE

DATE 16/ 7 / 92
NUMBER 96

ORIGINATOR Chris Alfred

PRODUCT: CMI / MFX

ASSEMBLY No. CMI-35

DESCRIPTION DIGITAL MOTHER BOARD

This FCN applies to REV No: REV -1

The New REV No is: REV-1.1

REASON FOR CHANGE:

It has been noted that channel cards crashing is caused by crosstalk along the mother board. The channel refresh line is induced with signals from the data bus.

The inside of the front panel and or rear of digital rack should be marked indicating this change.

DETAILS OF CHANGE:

Add 1 X 180pF capacitor to CMI-35 SLOT 8 between pins B47 and B46.

Alternatively do FCN 95.

This is an important point as only 1 X 180pF capacitor should be installed !

DO NOT MODIFY BOTH THE 8th CHANNEL CARD AND THE DIGITAL MOTHER BOARD.

ORIGINATOR: *C. Alfred*

DATE: 16-7-1992

SERVICE MANAGER:

DATE:

CMI-35 Digital Mother Board

Terminology

VP - Waveform Processor CMI-33
CS - Channel Support Card CMI-32
VRAM - Waveform RAM CMI-39
RAM - System RAM Q256

Introduction

All of the digital CMI modules described in chapters 2.2 to 2.13 of this manual, plug directly into 78 pin edge connectors mounted on the CMI digital motherboard CMI-35. This is in turn mounted on the rear of the CMI card cage. The motherboard is the means by which all logic signals and power supplies are routed between the plug-in modules. This section specifies each of these signals for each module, starting from the left.

All modules are "double sided" so require two columns of pins on each connector. "Side A" refers to the wiring side of a plug-in module which corresponds to the left hand column of pins on the motherboard when viewed from the front of the card cage. Conversely, "Side B" refers to the component side of the module and connects to the right hand column of pins on the edge connector.

Pin numbers not included in the following lists are not used, and have no connection on the motherboard. Signals which are listed but have "N/C" entered as the source or destination are those which have been connected to edge connector fingers but have no connections leading to or from the corresponding pins on the motherboard.

A pin specified as an input ("I/P") will have the Source module which drives that input entered in the Source/Destinations column. Conversely an output ("O/P") will have the Destination or driven module entered in the Source/Destinations column.

Active-low signals are indicated by overlining. All other signals are active-high. Where different names have been used for one signal going between various modules, the Signal Name column contains the name for the module of the current section, and the alternative name is enclosed in brackets in the Source/Destination column.

This document refers to the CMI-35 Rev. 3 motherboard.

General Description

The Series III CMI contains two entirely independent busses, and this is reflected in the layout of the CMI-35 motherboard. The first buss is the 2MHz dual-6809 processor buss, or CPU buss. It extends from the slot-27 end of the board on which the Q-777 SCSI controller resides up to slot 16, the Channel Support slot. Part of the CPU buss then extends further to slot 8 which is occupied by Channel 8. The only cards which have no connections at all to the CPU buss are the Waveform RAM cards. The CPU buss comprises 16 bits of address, 8 bits of data plus the system reset signal, CPU timing signals, DMA arbitration, daisy chain, and mapping signals, Peripheral Enable, Interrupts, and a few control signals.

The second buss in the system is the 3.3MHz Waveform Bus which extends from the slot-1 end of the CMI-35 board up to the Waveform Processor on slot 17. It comprises 23 address bits, 16 data bits, two data strobes, Channel card timing signals, a 17-MHz Master Oscillator differential pair, a 10MHz Processor Clock differential pair, a 3.3MHz buss clock, Channel Select lines, refresh controls, and Channel arbitration signals.

CPU Bus Signals

The following connections are common to all slots on the CPU buss and travel from slot 27 to slot 8, except that the signals on pins 9A to 17A stop at slot 15. The buss lines are arranged in a ground shield interleave pattern which provides protection against electromagnetic noise pickup and cross-talk between adjacent signal tracks. Not all modules use all the bussed signals.

Side A

| Pin | Signal Name | Function | Source |
|-------|-------------|---------------------------------------|---------|
| 42 | SYRES | System reset | Q133 |
| 41 | ADD2 | P2 address on buss ¹ | Q209 |
| 40 | ADD1 | P1 address on buss ¹ | Q209 |
| 39 | P2 ϕ 2 | P2 phase 2 reference | Q209 |
| 38 | P1 ϕ 2 | P1 phase 1 reference | Q209 |
| 37 | <u>RA</u> | Row address mux signal | Q209 |
| 36 | <u>CA</u> | Column address mux sig. | Q209 |
| 35 | <u>RAS</u> | Row address strobe | Q209 |
| 34 | <u>CAS</u> | Column address strobe | Q209 |
| 33-26 | D0-D7 | Data Buss | Various |
| 25-18 | MA0-MA7 | Address Buss, upper half | Various |
| 17-10 | MA8-MA15 | Address Buss, lower half ² | Various |
| 17 | ADD2 | P2 address on buss ¹ | Q209 |
| 16 | ADD1 | P1 address on buss ¹ | Q209 |
| 9 | VMA | Valid Memory Address ² | Various |
| 8 | R/W | Read/write | Various |
| 7 | Key | Socket index key | |
| 6 | +12V | +12V supply rail | |
| 3 | -12V | -12V supply rail | |
| 2,1 | GND | Ground rail | |

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Side B

| Pin | Signal Name | Function | Source |
|---------|-------------|--------------------------|--------|
| 44-46 | GND | Ground rail | |
| 42-1 | GND | Ground shielding pattern | |
| 5,4,2,1 | GND | Ground rail | |

Notes

1. The P2 ϕ 2 and P1 ϕ 2 signals are on pins 39A and 38A respectively of slots 27 to 16, then pins 17A and 16A of slots 15 to 8.
2. The lower half of the address bus and the VMA signal only go from slots 26 to 16, and do not go to the Channels card slots.

Waveform Bus Signals

The following signals are common to all slots on the Waveform Bus and travel from slot 1 to slot 15. The Channel Support Card on slot 16 also connects to the Waveform Bus but some connections are different. Not all the modules use all the signals.

Side A

| Pin | Signal Name | Function | Source |
|-------|-----------------|--|---------|
| 67 | <u>BLOCKSEL</u> | All-channel select ¹ | CS |
| 66 | <u>WUDS</u> | Waveform Upper Data Strobe | WP |
| 65 | <u>WLDS</u> | Waveform Lower Data Strobe | WP |
| 64-57 | <u>WA8-WA1</u> | Waveform Address lower byte | Various |
| 56-49 | <u>WD7-WD0</u> | Waveform Data lower byte | Various |
| 48 | <u>CHANTICK</u> | Chan. processor interrupt clock ¹ | CS |
| 47 | <u>DRAS</u> | Delayed RAS for channel RAM ¹ | CS |
| 46 | <u>2E</u> | 2MHz E clock for chan. proc. ¹ | CS |
| 45 | <u>2Q</u> | 2MHz Q clock for chan. proc. ¹ | CS |
| 44 | <u>PCLK</u> | 10MHz clock for WP and chans ² | CS |
| 43 | <u>PCLK</u> | 10MHz clock for WP and chans ² | CS |
| 42 | <u>SYRES</u> | System Reset from CPU ³ | CCC |
| 39 | <u>MOSC</u> | Master Oscillator ³ | CS |
| 38 | <u>MOSC</u> | Master Oscillator ³ | CS |

Side B

| Signal Pin | Name | Function | Source |
|------------|----------------|--|--------------|
| 75 | <u>SCLK</u> | 3.3MHz Waveform Bus clock ⁴ | CS |
| 74 | <u>TSTAKEN</u> | Time Slice Taken | Channels |
| 73 | <u>8BIT</u> | 8-bit mode select | Channels, WP |
| 72 | <u>WAS</u> | Waveform Address Strobe | WP |
| 71 | <u>WRW</u> | Waveform Read/Write | WP |
| 70-56 | WA23-WA9 | Waveform Address high bits | Channels, WP |
| 55-48 | WD15-WD8 | Waveform Data high byte | WP, WRAM |
| 47 | REFRESH | Channel refresh strobe | CS |
| 46-44 | GND | Ground Rail | |
| 5,4,2,1 | GND | Ground Rail | |

Notes

1. Slots 16 to 8 only
2. Differential pair, slots 17 to 8 only
3. MOSC and MOSC are the differential pair which drive the 17Mhz Master Oscillator used as the pitch reference by all channel cards. It is generated on the Channel Support Card, slot 16 onto pins 78B and 77B. These pins connect to link connector holes "A" and "B" near the top of slot 16 the pair of signals then goes via a twisted pair flying connection to another two link connector holes marked "A" and "B" near the middle of slot 15. The latter holes connect to pins 39A and 38A of slot 15 and the MOSC signal are then bussed along all channel card slots.
4. SCLK is a rectangular wave clock: 100nS high, 200nS low.

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Slots 1 to 7: Waveform RAM

Side A

| Pin | Signal Name | Function | Input or Output | Source/Destination |
|-------------|----------------------|------------------|-----------------|--------------------|
| 67 66-49 | WREF see Sec. X.3 | Waveform Refresh | I/P | WP |

Side B

| Pin | Signal Name | Function | Input or Output | Source/Destination |
|-------------|------------------------|---------------------|-----------------|--------------------|
| 76 75-48 | TSLICE see Sec. X.3 | Last Time Slice out | I/P | Ch. 7- |

Slot 8: Channel 8

Side A

| Pin | Signal Name | Function | Input or Output | Source/Destination |
|-----|-------------|------------------|-----------------|--------------------|
| 76 | SO | Time Slice Out | O/P | WRAMs (TSLICE) |
| 68 | CHSEL8 | Channel 8 select | I/P | CS |

Side B

| Pin | Signal Name | Function | Input or Output | Source/Destination |
|-----|-------------|-------------------|-----------------|--------------------|
| 76 | TSLICE | Time Slice In | I/P | Ch. 7 (SO) |
| 17 | CHINT | Channel interrupt | O/P | Q133 (IL21) |

Slot 9: Channel 7

Side A

| Pin | Signal Name | Function | Input or Output | Source/Destination |
|-----|-------------|------------------|-----------------|--------------------|
| 76 | SO | Time Slice Out | O/P | Ch. 8 (TSLICE) |
| 69 | CHSEL7 | Channel 7 select | I/P | CS |

Side B

| Pin | Signal Name | Function | Input or Output | Source/Destination |
|-----|-------------|-------------------|-----------------|--------------------|
| 76 | TSLICE | Time Slice In | I/P | Ch. 6 (SO) |
| 17 | CHINT | Channel interrupt | O/P | Q133 (IL21) |

Slot 10: Channel 6
Side A

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|-----|---------------|------------------|-----------------|---------------------|
| 76 | <u>SO</u> | Time Slice Out | O/P | Ch. 7 (TSLICE) |
| 68 | <u>CHSEL6</u> | Channel 6 select | I/P | CS |

Side B

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|-----|---------------|-------------------|-----------------|---------------------|
| 76 | <u>TSLICE</u> | Time Slice In | I/P | Ch. 5 (SO) |
| 17 | <u>CHINT</u> | Channel interrupt | O/P | Q133 (IL21) |

Slot 11: Channel 5
Side A

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|-----|---------------|------------------|-----------------|---------------------|
| 76 | <u>SO</u> | Time Slice Out | O/P | Ch. 6 (TSLICE) |
| 68 | <u>CHSEL5</u> | Channel 5 select | I/P | CS |

Side B

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|-----|---------------|-------------------|-----------------|---------------------|
| 76 | <u>TSLICE</u> | Time Slice In | I/P | Ch. 4 (SO) |
| 17 | <u>CHINT</u> | Channel interrupt | O/P | Q133 (IL21) |

Slot 12: Channel 4
Side A

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|-----|---------------|------------------|-----------------|---------------------|
| 76 | <u>SO</u> | Time Slice Out | O/P | Ch. 5 (TSLICE) |
| 68 | <u>CHSEL4</u> | Channel 4 select | I/P | CS |

Side B

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|-----|---------------|-------------------|-----------------|---------------------|
| 76 | <u>TSLICE</u> | Time Slice In | I/P | Ch. 3 (SO) |
| 17 | <u>CHINT</u> | Channel interrupt | O/P | Q133 (IL21) |

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Slot 13: Channel 3 Side A

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|-----|---------------|------------------|-----------------|---------------------|
| 76 | <u>SO</u> | Time Slice Out | O/P | Ch. 4 (TSLICE) |
| 68 | <u>CHSEL3</u> | Channel 3 select | I/P | CS |

Side B

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|-----|---------------|-------------------|-----------------|---------------------|
| 76 | <u>TSLICE</u> | Time Slice In | I/P | Ch. 2 (SO) |
| 17 | <u>CHINT</u> | Channel interrupt | O/P | Q133 (IL21) |

Slot 14: Channel 2 Side A

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|-----|---------------|------------------|-----------------|---------------------|
| 76 | <u>SO</u> | Time Slice Out | O/P | Ch. 3 (TSLICE) |
| 68 | <u>CHSEL2</u> | Channel 2 select | I/P | CS |

Side B

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|-----|---------------|-------------------|-----------------|---------------------|
| 76 | <u>TSLICE</u> | Time Slice In | I/P | Ch. 1 (SO) |
| 17 | <u>CHINT</u> | Channel interrupt | O/P | Q133 (IL21) |

Slot 15: Channel 1 Side A

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|-----|---------------|------------------|-----------------|---------------------|
| 76 | <u>SO</u> | Time Slice Out | O/P | Ch. 2 (TSLICE) |
| 68 | <u>CHSEL1</u> | Channel 1 select | I/P | CS |

Side B

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|-----|---------------|---------------------|-----------------|---------------------|
| 77 | <u>ADCLK</u> | A/D Converter clock | O/P | WP |
| 76 | <u>TSLICE</u> | Time Slice In | I/P | CS |
| 17 | <u>CHINT</u> | Channel interrupt | O/P | Q133 (IL21) |

Slot 16: Channel Support Card
Side A

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|-----|---------------|--------------------|-----------------|---------------------|
| 76 | <u>TSLICE</u> | First Time Slice | O/P | Ch. 1 |
| 75 | <u>CHSEL1</u> | Channel 1 select | O/P | Ch. 1 |
| 74 | <u>CHSEL2</u> | Channel 2 select | O/P | Ch. 2 |
| 73 | <u>CHSEL3</u> | Channel 3 select | O/P | Ch. 3 |
| 72 | <u>CHSEL4</u> | Channel 4 select | O/P | Ch. 4 |
| 71 | <u>CHSEL5</u> | Channel 5 select | O/P | Ch. 5 |
| 70 | <u>CHSEL6</u> | Channel 6 select | O/P | Ch. 6 |
| 69 | <u>CHSEL7</u> | Channel 7 select | O/P | Ch. 7 |
| 68 | <u>CHSEL8</u> | Channel 8 select | O/P | Ch. 8 |
| 66 | REFEN | Refresh enable | I/P | Q133 (ENL1) |
| 65 | ACK1 | P1 DMA Acknowledge | I/P | Q209 |

Side B

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|-----|---------------|--------------------------------|-----------------|---------------------|
| 78 | <u>MOSC</u> | Master Oscillator ¹ | O/P | Channels |
| 77 | <u>MOSC</u> | Master Oscillator ¹ | O/P | Channels |
| 76 | <u>TIMINT</u> | Timer Interrupt | O/P | Q133 (IL11) |
| 43 | PENB | Peripheral Enable | I/P | RAM, Card 0 |

Notes

1. MOSC and MOSC are the differential pair which drive the 17MHz Master Oscillator used as the pitch reference by all channel cards. It is generated on the Channel Support Card, slot 16 onto pins 78B and 77B. These pins connect to link connector holes "A" and "B" near the top of slot 16 the pair of signals then goes via a twisted pair flying connection to another two link connector holes marked "A" and "B" near the middle of slot 15. The latter holes connect to pins 39A and 38A of slot 15 and the MOSC signal are then bussed along all channel card slots.

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Slot 17: Waveform Processor

Side A

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|-----|---------------|----------------------|-----------------|-----------------------|
| 76 | <u>P2DMAC</u> | P2 DMA Claim | O/P | RAMs (DMAC24) |
| 75 | <u>P1DMAC</u> | P1 DMA Claim | O/P | RAMs (DMAC12) |
| 71 | <u>WREF</u> | Waveform Refresh | O/P | WRAMs |
| 70 | <u>ETL2</u> | P2 Enable This Level | I/P | SMIDI (<u>ENL2</u>) |
| 69 | <u>ENL2</u> | P2 Enable Next Level | O/P | SCSI (ETL) |
| 68 | ETL1 | P1 Enable This Level | I/P | SMIDI (<u>ENL1</u>) |
| 67 | ENL1 | P1 Enable Next Level | O/P | N/C |
| 48 | <u>ACK2</u> | P2 DMA Acknowledge | I/P | Q209 |
| 47 | <u>RDMA2</u> | P2 Request DMA | O/P | Q209 |
| 46 | <u>ACK1</u> | P1 DMA Acknowledge | I/P | Q209 |
| 45 | <u>RDMA1</u> | P1 Request DMA | O/P | Q209 |

Side B

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|-----|--------------|----------------------|-----------------|---------------------|
| 76 | <u>ADCLK</u> | AD Convertor Clock | I/P | Ch. 1 |
| 43 | <u>FCXX</u> | Control latch select | I/P | Q133 |

Slot 18: General Interface Card CMI-28

Side A

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|-------|-----------------|--------------------------|-----------------|---------------------|
| 78,77 | +5V | +5V Logic supply | | |
| 76 | <u>P2DMAC</u> | P2 DMA claim | O/P | RAMs (DMAC24) |
| 75 | <u>P1DMAC</u> | P1 DMA claim | O/P | RAMs (DMAC11) |
| 70 | <u>ETL2</u> | P2 DMA Enable This Level | I/P | QFC9 (ENL) |
| 69 | <u>ENL2</u> | P2 DMA Enable Next Level | O/P | WP (ETL2) |
| 68 | <u>ETL1</u> | P1 DMA Enable This Level | I/P | Q133 (ENL1) |
| 67 | <u>ENL1</u> | P1 DMA Enable Next Level | O/P | WP (ETL1) |
| 66 | <u>MIDINT</u> | MIDI IRQ | O/P | Q133 (IL01) |
| 65 | <u>SMPTEINT</u> | SMPTE IRQ | O/P | Q133 (IL31) |
| 64 | <u>FCXX</u> | Control latch select | I/P | Q133 |
| 48 | <u>ACK2</u> | P2 DMA Acknowledge | I/P | Q209 |
| 47 | <u>RDMA2</u> | P2 DMA Request | O/P | Q209 |
| 46 | <u>ACK1</u> | P1 DMA Acknowledge | I/P | Q209 |
| 45 | <u>RDMA1</u> | P1 DMA Request | O/P | Q209 |

Side B

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|-----|----------------|-------------|-----------------|---------------------|
| 69 | <u>MIDINT</u> | MIDI IRQ | O/P | N/C |
| 68 | <u>SMIDINT</u> | SMPTE IRQ | O/P | N/C |
| 67 | <u>FCXX</u> | Port select | I/P | N/C |

The B-side signals on pins 67-69 are duplicates of the corresponding signals on side A, and are only used when a CMI-28 module is installed in a Series I machine upgraded to Series IIX.

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Slot 19: Spare

Side A

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|-------|-------------|------------------|-----------------|---------------------|
| 78,77 | +5V | +5V Logic supply | | |
| 54 | FCXX | Port select | I/P | Q133 |
| 46 | IRQ | Interrupt | O/P | Q133(IL41) |

Slots 20,21: System RAM Q256

One Q256 module must be installed in slot 21. This is referred to as Card 0 and must have zero set up on the card select DIP switch on the board (see Q256 description). A second Q256 module may be installed in slot 20, and should be switched as Card 1.

Side A

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|-------|-------------|------------------------------------|-----------------|--------------------------|
| 78-77 | +5V | Logic power supply | I/P | |
| 76 | BE1 | P1 E signal (unused) | I/P | Q209 |
| 75 | DMAC11 | P1 DMA claim level 1 | I/P | Gen. I/F (PIDMAC) |
| 74 | DMAC12 | P1 DMA claim level 2 | I/P | WP (PIDMAC) |
| 73 | DMAC13 | P1 DMA claim level 3 | I/P | N/C |
| 72 | DMAC14 | P1 DMA claim level 4 | I/P | N/C |
| 71 | DMAC21 | P2 DMA claim level 1 | I/P | Floppy (DMACLM) |
| 70 | DMAC22 | P2 DMA claim level 2 | I/P | H. Disk (DMACLM) |
| 69 | DMAC23 | P2 DMA claim level 3 | I/P | WP (P2DMAC) |
| 68 | DMAC24 | P2 DMA claim level 4 | I/P | Gen. I/F (P2DMAC) |
| 65 | RAMINH | System RAM Inhibit | I/P | Graphics (VRAMSEL) |
| 64 | FCXX | Port select (Mapsel RAM) | I/P | Q133 |
| 63 | A/B2 | P2 System/User State | I/P | Q209 |
| 62 | A/B1 | P1 System/User State | I/P | Q209 |
| 52 | PENBIN | Peripheral Enable In ¹ | I/P | RAM, Card 0 (PENBOUT) |
| 51 | PENBOUT | Peripheral Enable Out ¹ | O/P | Various |
| 50 | VRAMEN | Video RAM Enable ² | O/P | Graphics |
| 48 | REF | Refresh cycle | I/P | Q133 |
| 46 | PERRINT | Parity Error IRQ | O/P | Q133 (IL02) |

Notes

1. The PENB (Peripheral Enable) signal is driven by the PENBOUT pin 52A of RAM card 0 only, in slot 21. PENB goes to all cards which act as peripherals on the CPU bus, including PENBIN of both RAM cards on pin 51A. The main RAM is not a peripheral, but the MAPSEL and MAPRAM are (see Q256 documentation). PENBOUT of card 1 is N/C.

2. The VRAMEN output from RAM card 0 only goes to the Graphics card. VRAMEN of card 1 is N/C.

Slot 22: Q014 4-Port ACIA Module (Optional)

Side A

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|-------|-------------|----------------------|-----------------|---------------------|
| 78-77 | +5V | Logic power supply | I/P | |
| 66 | ENB | Peripheral Enable | I/P | RAM (PENBOUT) |
| 65-58 | IRQ0-7 | Individual ACIA IRQs | O/P | N/C |
| 57 | IRQ8 | Combined IRQ | O/P | Q133 (IL62) |
| 56-53 | AS6-AS9 | Address select | I/P | N/C |

Slot 23: Processor Control Module Q133

Side A

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|-------|-------------|------------------------|-----------------|----------------------------------|
| 78-77 | +5V | Logic power supply | I/P | |
| 76 | IL32 | P2 level 3 IRQ | I/P | Q209 (IPI2) |
| 75 | IL22 | P2 level 2 IRQ | I/P | N/C |
| 74 | IL12 | P2 level 1 IRQ | I/P | Graphics (RINT) |
| 73 | IL02 | P2 level 0 IRQ | I/P | Q133 (RTCINT) & RAM (PERRINT) |
| 72 | IL31 | P1 level 3 IRQ | I/P | Q209 (IPI1) & GIF (SMPTEINT) |
| 71 | IL21 | P1 level 2 IRQ | I/P | All Chs (CHINTX) |
| 70 | IL11 | P1 level 1 IRQ | I/P | Ch. Supp (TIMINT) |
| 69 | IL01 | P1 level 0 IRQ | I/P | GIF (MIDINT) |
| 68 | ILS2 | P2 PICU latch strobe | I/P | Q209 |
| 67-64 | IA42-IA12 | P2 intrpt vector addr. | O/P | Q209 |
| 63 | IRQ2 | P2 interrupt request | O/P | Q209 |
| 62 | ILS1 | P1 PICU latch strobe | I/P | Q209 |
| 61-58 | IA41-IA11 | P1 intrpt vector addr. | O/P | Q209 |
| 57 | IRQ1 | P1 interrupt request | O/P | Q209 |
| 56 | NMI2 | P2 NMI request | O/P | Q209 |
| 55 | NMI1 | P1 NMI request | O/P | Q209 |
| 54 | RES2 | P2 restart | O/P | Q209 |
| 53 | HLT2 | P2 HALT | O/P | Q209 |
| 52 | RES1 | P1 restart | O/P | Q209 |
| 51 | HLT1 | P1 HALT | O/P | Q209 |
| 50 | W2 | P2 halt acknowledge | I/P | Q209 |
| 49 | W1 | P1 halt acknowledge | I/P | Q209 |
| 48 | REF | Refresh cycle | O/P | RAM |
| 47 | PENB | Peripheral enable | I/P | RAM (PENBOUT) |
| 46 | ACK1 | Refresh acknowledge | I/P | Q209 |
| 45 | REQ1 | Refresh cycle request | O/P | Q209 |
| 44 | ROMEN | Restart ROM enable | I/P | Q209 |

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Side B

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|-------|----------------------------|---------------------------|-----------------|---|
| 76 | IL72 | P2 level 7 IRQ | I/P | QFC9, SCSI ($\overline{\text{IRQD}}$) |
| 75 | IL62 | P2 level 6 IRQ | I/P | Q133 ($\overline{\text{ACINT}}$) & Q014 ($\overline{\text{IRQ8}}$) |
| 74 | IL52 | P2 level 5 IRQ | I/P | Graphics ($\overline{\text{PENINT}}$) |
| 73 | IL42 | P2 level 4 IRQ | I/P | Graphics ($\overline{\text{TOUCHINT}}$) |
| 72 | IL71 | P1 level 7 IRQ | I/P | N/C |
| 71 | IL61 | P1 level 6 IRQ | I/P | N/C |
| 70 | IL51 | P1 level 5 IRQ | I/P | N/C |
| 69 | IL41 | P1 level 4 IRQ | I/P | Spare ($\overline{\text{IRQ}}$) |
| 68 | $\overline{\text{ACINT}}$ | Keyboard ACIA IRQ | O/P | Q133 (IL62) |
| 67 | $\overline{\text{IROPA}}$ | User PIA IRQ A | O/P | N/C |
| 66 | $\overline{\text{IROPB}}$ | User PIA IRQ B | O/P | N/C |
| 65 | $\overline{\text{ENLI}}$ | P1 DMA Enable Next Level | O/P | GIF ($\overline{\text{ETL1}}$) & Ch Supp (REFEN) |
| 64 | $\overline{\text{FCXX}}$ | Ports access | O/P | Various |
| 63 | $\overline{\text{RTCINT}}$ | Real time clock intrpt | O/P | Q133 (IL02) |
| 62,61 | | Current loop TX | O/P | N/C |
| 60 | $\overline{\text{FXXX}}$ | FXXX address range decode | O/P | N/C |

Slot 24: Central Processor Module Q209

Side A

| Pin | Signal Name | Function | Input or Output | Source/ Destination |
|-------|--------------|--------------------------|-----------------|---------------------|
| 78-77 | +5V | Logic power supply | I/P | |
| 76 | BE1 | P1 "E" signal | O/P | RAM, Spare |
| 75 | <u>FIRQ2</u> | P2 Fast IRQ | I/P | N/C |
| 74 | <u>FIRQ1</u> | P1 Fast IRQ | I/P | N/C |
| 73 | <u>IPI2</u> | P2 Interprocessor Intrpt | O/P | Q133 (IL32) |
| 72 | <u>IPI1</u> | P1 Interprocessor Intrpt | O/P | Q133 (IL31) |
| 71 | <u>FCXX</u> | Port select | I/P | Q133 |
| 70 | A/ <u>B2</u> | P2 System/User state | O/P | RAM |
| 69 | A/ <u>B1</u> | P1 System/User state | O/P | RAM |
| 68 | ILS2 | P2 PICU latch strobe | O/P | Q133 |
| 67-64 | IA42-IA12 | P2 intrpt vector addr. | I/P | Q133 |
| 63 | <u>IRQ2</u> | P2 interrupt request | I/P | Q133 |
| 62 | ILS1 | P1 PICU latch strobe | O/P | Q133 |
| 61-58 | IA41-IA11 | P1 intrpt vector addr. | I/P | Q133 |
| 57 | <u>IRQ1</u> | P1 interrupt request | I/P | Q133 |
| 56 | <u>NMI2</u> | P2 NMI request | I/P | Q133 |
| 55 | <u>NMI1</u> | P1 NMI request | I/P | Q133 |
| 54 | <u>RES2</u> | P2 restart | I/P | Q133 |
| 53 | <u>HLT2</u> | P2 HALT | I/P | Q133 |
| 52 | <u>RES1</u> | P1 restart | I/P | Q133 |
| 51 | <u>HLT1</u> | P1 HALT | I/P | Q133 |
| 50 | W2 | P2 in wait state (BA) | O/P | Q133 |
| 49 | W1 | P1 in wait state (BA) | O/P | Q133 |
| 48 | ACK2 | P2 DMA acknowledge | O/P | QFC9, SCSI, WP, |
| GIF | | | | |
| 47 | <u>REQ2</u> | P2 DMA request | I/P | QFC9, SCSI, WP, GIF |
| 46 | <u>ACK1</u> | Refresh cycle grant | O/P | Q133, WP, GIF, CS |
| 45 | <u>REQ1</u> | Refresh cycle request | I/P | Q133, WP, GIF |
| 44 | ROMEN | Restart ROM enable | O/P | Q133 |
| 43 | OSC | Master proc. clock | O/P | N/C |

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Slot 25: Lightpen/Graphics Interface Q219

Side A

| Pin | Signal Name | Function | Input or Output | Source/Destination |
|-------|-------------|---------------------|-----------------|--------------------|
| 78-77 | +5V | Logic power supply | I/P | |
| 68 | RINT | Timer IRQ | O/P | Q133 (IL12) |
| 67 | PENINT | Light pen hit IRQ | O/P | Q133 (IL52) |
| 66 | TOUCHINT | Light pen touch IRQ | O/P | Q133 (IL42) |
| 65 | VRAMEN | Video RAM Enable | I/P | RAM Card 0 |
| 64 | FCXX | Port select | I/P | Q133 |
| 63 | VRAMSEL | Video Ram Select | O/P | RAM (RAMINH) |

Slot 26: Floppy Disc Controller QFC-9

Side A

| Pin | Signal Name | Function | Input or Output | Source/Destination |
|-------|-------------|-----------------------|-----------------|----------------------------------|
| 78-77 | +5V | Logic power supply | I/P | |
| 71 | EDL | Enable Daisy Links | O/P | Floppy \overline{ETL}^1 |
| 70 | ETL | Enable This Level | I/P | Floppy & SCSI \overline{EDL}^1 |
| 69 | ENL | Enable Next Level | O/P | GIF (\overline{ETL}) |
| 68 | DMACLM | DMA claim | O/P | RAM ($\overline{DMAC21}$) |
| 65 | PENB | Peripheral Enable | I/P | RAM card 0 |
| 63 | IRQD | Floppy Controller IRQ | O/P | Q133 (IL72) |
| 48 | ACK2 | DMA cycle grant | I/P | Q209 |
| 47 | RDMA | DMA request | O/P | Q209 ($\overline{REQ2}$) |

Slot 27: SCSI Controller Q777

Side A

| Pin | Signal Name | Function | Input or Output | Source/Destination |
|-------|-------------|---------------------|-----------------|---------------------------------------|
| 78-77 | +5V | Logic power supply | I/P | |
| 72 | EDL | Enable Daisy Links | O/P | GIF (\overline{ETL}) ² |
| 71 | EDL | Enable Daisy Links | O/P | Floppy \overline{ETL}^1 |
| 70 | ETL | Enable This Level | I/P | WP ($\overline{ENL2}$) |
| 69 | ENL | Enable Next Level | O/P | N/C |
| 68 | DMACLM | DMA claim | O/P | RAM ($\overline{DMAC22}$) |
| 65 | PENB | Peripheral Enable | I/P | RAM card 0 |
| 63 | IRQD | SCSI Controller IRQ | O/P | Q133 (IL72) |
| 48 | ACK2 | DMA cycle grant | I/P | Q209 |
| 47 | RDMA | DMA request | O/P | Q209 ($\overline{REQ2}$) |

Notes

1. EDL outputs of both QFC-9 and Q777 go to ETL input of QCF-9. Link optioning on the two controller boards determines which output is actually used. QFC-9 output should only be used if no Q777 is installed. See section X.25.
2. Extra EDL output from Q777 bypasses the QFC-9 and goes directly to ETL input of GIF card to allow system to be run without QFC-9 card. Currently pin 72A of Q777 is not driven. See section X.25.

Series III CPU Interrupt Level Assignments

Processor 1

| Level | Source(s) | | o/c | IRQ input |
|-------|-----------------------------|---|-----|---------------|
| 0 | MIDIINT: CMI-28 66A | * | y | IL01: DBG 69A |
| 1 | TIMINT: Ch. Supp. 76B | * | y | IL11: DBG 70A |
| 2 | CHINT: All channels 10B-17B | | y | IL21: DBG 71A |
| 3 | P1 IPI: CPU 72A | * | y | IL31: DBG 72A |
| | SMPTE: CMI-28 65A | | y | |
| 4 | AIC: AIC 46A | * | y | IL41: DBG 69B |
| 5 | - | | | IL51: DBG 70B |
| 6 | - | | | IL61: DBG 71B |
| 7 | - | | | IL71: DBG 72B |

Processor 2

| Level | Source(s) | | o/c | IRQ input |
|-------|-------------------------|---|-----|---------------|
| 0 | RTCINT: DBG 63B | | y | IL02: DBG 73A |
| | PERRINT: Q256 46A | | y | |
| 1 | LPEN timer: Q219 68A | | y | IL12: DBG 74A |
| 2 | - | | | IL22: DBG 75A |
| 3 | P2 IPI: CPU 73A | | y | IL32: DBG 76A |
| 4 | TOUCHINT: Q219 66A | | y | IL42: DBG 73B |
| 5 | PEN INT: Q219 67A | | y | IL52: DBG 74B |
| 6 | Keyboard ACIA: DBG 68B | * | y | IL62: DBG 75B |
| | ACIAs: Q014 57A | | y | |
| 7 | DISKS: QFC-9, Q077, 63A | | y | IL72: DBG 76B |

Notes

- 1) * indicates departure from or addition to Series II assignments
- 2) "y" in the o/c column indicates IRQ outputs which are open collector and can therefore be wired in parallel with other IRQs on the same level if desired.
- 3) Source and IRQ input columns give the name of the interrupt followed by the card and edge connector pin number.
- 4) There is no second P1 interrupt control unit in Series III as there was on the Master Card in Series II. Hence the wiring together of all Channel interrupts.

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Series III DMA Daisy Chain Assignments

Modification history

Rev 3: Provision for $\overline{\text{EDL}}$ from either Q777 or QFC-9 to QFC-9 $\overline{\text{ETL}}$, and provision for $\overline{\text{EDL}}$ direct from Q777 to CMI-28.

Arbitration between the various devices which can access the CPU buss via DMA (cycle-stealing Direct Memory Access) is achieved by a daisy chain. At present the Series III daisy chains are prioritised as follows:

- P1: 1. System RAM Refresh (Q133) ($\overline{\text{EDL}}$ generated internally)
2. General Interface Card (CMI-28)
3. Waveform Processor (CMI-33)
- P2: 0. EDL from either Q777 or QFC-9
1. Floppy controller (QFC-9)
2. General Interface Card (CMI-28)
3. Waveform Processor (CMI-33)
4. SCSI Controller (Q777)

Note that for a given DMA device to work, all higher priority devices must be present in the system or the daisy chain signals for an absent device jumpered on the motherboard. The only exception to this is the bypass link from 72A of the Q777 slot ($\overline{\text{EDL}}$) to the GIF $\overline{\text{ETL}}$ which allows the system to be run without a QFC-9 simply by linking 71A and 72A on the Q777 board.

The Q256 DMA Channels are assigned as follows:

- P1: Ch 1 SMPTE/MIDI Processor FC4C
Ch 2 Waveform Processor FC4D
Ch 3 Unused FC4E
Ch 4 Unused FC4F
- P2: Ch 1 Floppy controller FC44
Ch 2 SCSI controller FC45
Ch 3 Waveform Processor FC46
Ch 4 SMPTE/MIDI Processor FC47