MFX 010

MFX CONTROLLER

fairlight

FIELD CHANGE NOTICE

DATE 21/ 8 /92
NUMBER 102

ORIGINATOR Chris Alfred **PRODUCT: CMI / MFX**

ASSEMBLY No. MFX-010 **DESCRIPTION** MFX Controler PCB

This FCN applies to REV No: REV 1 **The New REV No is:** REV 1.1

REASON FOR CHANGE:

Limit current drawn by IBM mouse which causes mouse to get hot and malfunction.

DETAILS OF CHANGE:

1. Remove modification wires to W4 pins 11 and 20.
(Check both sides of the PCB)
2. Connect 150 ohm 1/2 watt resistors in place of the wire links.
See diagram.
3. Mark PCB with new revision.

ORIGINATOR: C Alfred **DATE:** 21 - 8 - 1992

SERVICE MANAGER: [signature] **DATE:** 21. 8. 92

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FIELD CHANGE NOTICE

DATE 25/ 11/ 92
NUMBER 113

ORIGINATOR Chris Alfred **PRODUCT: CMI / MFX**

ASSEMBLY No. MFX 010 **DESCRIPTION** Main PCB in MFX Console

This FCN applies to REV No: 1.1 **The New REV No is:** Rev ~~0.1~~ 1.2

REASON FOR CHANGE:
Modification missing on PCB which do not have the 6809 processor installed.

This missing modification can cause the MFX console to "Freeze", "Lock up", "Crash".

DETAILS OF CHANGE:

1. Connect U40 pin 13 to U40 pin 14 (74AC08)

2. Label PCB as Rev 0.1

ORIGINATOR: [signature] DATE: 25-11-92	PROD: [signature] DATE: 25.11.92
SERVICE: DATE:	KIT LIST CHANGE: YES (NO)

fairlight

FIELD CHANGE NOTICE

DATE 27/ 1 / 93
NUMBER 118

ORIGINATOR Shane Morris **PRODUCT: CMI / MFX**

ASSEMBLY No. MFX 010 **DESCRIPTION** Main PCB in MFX

This FCN applies to REV No: REV 1.2 **The New REV No is:** REV 1.3

REASON FOR CHANGE:

The installation of REV 6.00 ROMs for REV 11 A or REV 11 B operation.

DETAILS OF CHANGE:

1. Power down system. Disconnect power and MFX cabling.
2. Remove bottom panel screws to gain access to the top of the main MFX pcb.
Check previous FCN information. To this date: FCN 102 and FCN 113
3. Remove U53 and replace with new REV 6.00 U53
4. Remove U54 and replace with new REV 6.00 U54.
5. Label pcb as REV 1.3

ORIGINATOR:	DATE:	PROD: [signature]	DATE: 4/2/93
SERVICE:	DATE:	KIT LIST CHANGE:	YES NO

fairlight

FIELD CHANGE NOTICE

DATE 24/ 3 /93
NUMBER 122

ORIGINATOR Chris Alfred **PRODUCT: CMI / MFX**

ASSEMBLY No. MFX-010 **DESCRIPTION** Main MFX PCB

This FCN applies to REV No: REV 1.3 **The New REV No is:** REV 1.4

REASON FOR CHANGE:
Noise on MIDI data to MIDI processor due to induction from RS232 signals in MFX cable

Causes errors in the disk recorder time when the mouse is moved or keys are pressed rapidly.

DETAILS OF CHANGE:

1. Change R68 and R72 from 56 ohm to 2K2 ohm

2. Note new revision number of PCB.

ORIGINATOR: [illegible]	DATE: 24/3/93	TEST:	DATE:
		PROD:	DATE:
SERVICE:	DATE:	KIT LIST CHANGE:	(YES) NO

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1. Introduction

The MFX keyboard is a console designed to facilitate the use of post-production software on the Series III CMI. It combines features of both the PREH alpha-numeric keyboard and the CMI music keyboard, whilst considerably extending their usefulness for post-production work. Additional features not available on previous Fairlight products include an interface to control tape synchronisers and a jogger wheel.

The MFX keyboard contains three circuit boards. MFX010 is the controller board for the MFX console, containing the microprocessors. The other two boards, MFX030 and MFX040, are used to decode the switches and trigger keys.

The MFX010 contains two processors: a 68000 and a 6309 processor. These processors have seperate memory spaces and can execute code independently of each other.

2. 68000 master processor

(refer schematic MFX010.001)

The 68000 is responsible for the bulk of the processing tasks in the MFX as it handles every task except scanning the 24 trigger keys. The 6309 slave processor appears to the 68000 as a single 8-bit register except at power-up as the boot procedure is more complicated. It has ROM, RAM and non-volatile RAM to store and execute programs and data.

The peripherals of the 68000 are memory mapped in the usual way, with the high bits of the address buss determining the active peripheral. Each peripheral capable of generating interrupts is assigned to a different interrupt level.

2.1 ROMs

(refer schematic MFX010.003)

Two 8 bit EPROMs are used in parallel to provide the 16-bit boot

code required by the 68000. These EPROMs may be either 2764 or 27256 varieties with access times of 170ns or better. Selection is via a jumper block next to the EPROMs. When accessing these EPROMs, no wait states are required by the 68000 allowing full-speed operation.

On power-up or after a reset, the EPROMs are mapped at location 0, as this is where the 68000 loads its initial stack pointer and program counter. The EPROMs can also be accessed at location $100000H. By setting the signal OVLY low (U24 pin 15) the EPROM is mapped out of location 0 and replaced by static RAM. This allows the exception vector locations to be modified by software. The OVLY signal is set high by reset. Regardless of the state of OVLY, the EPROMs may be accessed starting at $100000H.

The first instruction of the EPROM is to set OVLY low. If this does not occur then the processor is probably not able to execute any instructions. If the processor does not even load the stack pointer and program counter then the problem is very fundamental, and is not simply problems with the address or data lines.

2.2 RAM

(refer schematic MFX010.002, 003 and 005)

Two 8 bit static RAMs are used in parallel to provide the 16-bit wide memory space in which to execute code. Normally 256K-bit RAMs are installed giving 32K words of memory. The memory is mapped starting at location 0. This allows direct access to the 68000 exception vectors, which occupy the first $200H words.

On power-up or reset, the signal OVLY is high, mapping the EPROMs to location 0 and preventing access to the RAMs. Normally, the first instruction executed is sets OVLY low, mapping the RAM to location 0. OVLY should remain low until power is removed or the processor is reset.

The MFX keyboard has been designed to allow down-loading of software from the Series III CMI, eliminating the need for costly EPROM updates. The task of the boot code in the EPROMs is to move the application code from the non-volatile memory to the

RAM for execution.

2.3 Non-volatile RAM

(refer schematic MFX010.003)

An 8K by 8-bit static RAM with battery-backup is provided to store programs, configuration setups and data. This RAM is protected by a DS1234 non-volatile controller (U38), which controls write-protection and battery usage. The memory may be configured to be read-only or read-write and volatile or non-volatile. Normally the memory is kept as ready-only non-volatile memory, and changed to read-write memory only when the data is being changed.

As this memory space is only 8 bits wide, it is not possible to execute programs directly from this RAM. At a temperature of 25°C, the BR2325 battery should provide a life of 8 years. Care should be taken to avoid exposing the MFX to extremes of temperature for long periods of time, as elevated temperature decreases the battery life rapidly.

At the time of writing this document, 100% CMOS RAMs are only made by Toshiba and are proving difficult to obtain. However they offer such low stand-by currents that they would offer non-volatility for the shelf-life of the battery (> 10 years).

There is a jumper block provided which allows selection of a variable number of wait states for the non-volatile RAM - either 0, 2, 4 or 6 wait states. This may be necessary as the DS1234 shortens the access times of the RAM by around 30ns. The actual setting used depends on the speed of the installed static RAM.

The 6309 processor does not have any non-volatile RAM, so the application program for this processor is stored in the 68000 non-volatile RAM and downloaded on power-up.

2.4 Address Decoding

(refer schematic MFX010.002)

The address decoding is performed by two 74ACT138

demultiplexers (U48 and U49) and half of a 74HC139 demultiplexer (U39). The 16 megabyte memory space of the 68000 is divided up into sixteen 1 megabyte areas by the two 74ACT138s, with each register or peripheral given its own area. All the peripherals decoded by U49 are no wait-state devices, whilst those decoded by U48 must supply an open collector /DTACK signal.

The second last address space is supplied to the 74HC139, which subdives this space into four areas for use by peripherals which require synchronisation to the 1MHz E clock of the 68000. The /CS6800 signal tells the 68000 to synchronise to the E clock by asserting VPA low whenever this address range is selected.

The highest 1 megabyte address space should be left vacant, as this space is selected whenever an interrupt acknowledge cycle is commenced.

/DTACK is generated by all four DUARTs (U12, U13, U20 and U24) and by the 74HC175 (U55). Whenever the demultiplexer U49 is selected, U55 is reset causing /DTACK to be asserted low. Whenever the non-volatile RAM is selected, the select signal is shifted through the flip-flops of U55 on the rising edge of PCLK (10MHz) until is appears at the link block (W5) causing /DTACK to be asserted low.

2.5 LED Circuitry

(refer schematic MFX010.006 and 007)

The LEDs controlled by the MFX are arranged into rows and columns, and lit using a multiplexed scheme. Under this scheme, each LED is pulsed on for 1ms with a high current, and then turned off for 7ms. By pulsing the LED its efficiency is improved and the drive circuitry is simplified.

The 16 columns are controlled by two 74HC273 latches (U8 and U9). If a bit is set to high, then the corresponding column is active. The columns are driven by two UDN2981 high-current source drivers (U10 and U11) and the current set by the 100R 1W resistors. The outputs of the source drivers are either VLED (+12V) if they are driven or floating if they are off.

The 8 rows are controlled by a 74HC164 shift register (U16). This register is arranged as a circulating buffer with one bit high (the active row) and the other bits low. Every time an access is made to the column register, the active row is incremented. The rows are driven by two ULN 2803A darlington drivers (U17 and U18) in parallel. The outputs of the drivers are either around 1 volt if driven, or floating if they are off.

The circuitry has been designed to work optimally if the LED column register is accessed every 1ms. This speed ensures that the blinking of the LEDs (125Hz) is faster than the human eye. If an LED were to be driven by this circuitry continuously then it would burn-out because the driving currents are greater than the maximum allowable average current through the LEDs. To prevent this undesirable event, protection circuitry has been installed to turn off the LEDs if the column register is not accessed for 3ms. This protection circuitry consists of a 74HC123 dual monostable (U4) and a flip-flop (U6). If a fault condition is detected then U8, U9 and U16 are reset, and the signal START goes high. When the LED register is next accessed, START supplies the initial conditions to drive output Q0 of U16 high.

If the next row to become active will be ROW0 then the signal CHECK will be high. This signal is available at ACIA2 (U13), input port signal IP4 (pin 39). The software should check this signal to determine if it agrees with what software expects. If a disagreement is detected, the software should immediately write a 0 to the LED column register and wait 10ms. If the signal CHECK is now high, the LED scanning may resume, otherwise the software should disable LED scanning and inform the user.

2.6 Clocks

(refer schematic MFX010.004 and 008)

The main system clock, PCLK, is supplied by a 10MHz oscillator (OSC1). The 68000 divides this signal by 10 to give the 1MHz E clock (6:4 duty cycle) used by slow synchronous peripherals (displays and fader ADC). The E clock is divided by a flip-flop (U6) to give a 1/2 MHz square wave. The 1/2 MHz clock is used by duart U12 as the 16 x MIDI clock.

A 3.6864MHz clock is generated by duart U20 for use in generating RS232 baud rates. See the section on the DUARTs for more information.

An 8MHz clock is used by the 6309 processor to generate its E and Q clocks. See the 6309 section for more information.

2.7 Watchdog

(refer schematic MFX010.008)

A DS1232 watchdog (U32) is used to supervise the operation of the MFX keyboard. It drives the open collector /RESET and /HALT signals low whenever the +5V power supply is out of range (4.75V to 5.25V), if the optional reset button has been pressed (connector J1), or if the watchdog has not been accessed by the 68000 for 100ms. The 68000 requires both /RESET and /HALT to cause it to reset. If the 68000 does a double buss fault (e.g. loading an odd address pointer during an exception vector fetch) then it will drive /HALT low. If the 68000 executes a reset instruction, then it will drive /RESET only low.

Both /RESET and /HALT also drive low-current red LEDs (LD6 and LD7). If both LEDs light simultaneously, then it is likely that the watchdog is driving these lines. However if the /HALT LED lights marginally before the /RESET LED then it is likely that the 68000 has had a double buss fault. This would occur if the ROMs were corrupt or if there was a serious problem with the address or data buss.

If the green LED (LD8) remains lit, then the 68000 is executing code and keeping the watchdog at bay. If the green and red LEDs light alternately, then the 68000 is not executing correct code.

2.8 Faders

(refer schematic MFX010.010)

The MFX supports the attachment of up to 8 faders through the expansion port on the rear panel of the MFX. The 8 channel ADC0848 (U27) can read the voltage on the signals

FADER0-FADER7 to 8 bit accuracy over the range 0V to 5V. The input channel and operation mode is set-up by a write instruction. Approximately 30µs later FR goes low signalling the end of conversion. FR is available at ACIA1 (U12) input pin IP0 (pin 7). A read to the ADC returns the result of the conversion.

2.9 Displays

(refer schematic MFX010.011 and 042)

The MFX keyboard supports the attachment of two LM402B01 displays. These displays each offer 40 columns by 2 rows with up to 8 custom characters. The display is backlit by yellow LEDs, which shine through the characters (clear characters on a black background). The data buss, address buss and R/W are buffered (74HCT245 at U2 and elsewhere) before driving the display signal cables (J5 and J6).

The backlight is driven from -12V, as very little other use is made of the negative supply capacity of the MFX.

A contrast adjustment pot is accessable from the underside of the MFX keyboard. Before concluding that a display is faulty because nothing is visible, you should check the contrast adjustment.

2.10 DUARTs

(refer schematic MFX010.004 and 005)

The MFX supports serial communications with the following devices:

1) MIDI to MIDI D on the CMI
2) MIDI from MIDI D on the CMI
3) MIDI from the Fairlight music keyboard
4) RS422 to and from a LYNX synchroniser or other synchroniser supporting the ES buss.
5) RS232 to and from an MFX expansion device
6) RS232 to the CMI keyboard input
7) RS232 from printer port 2 on the CMI (this port is no longer an external connector)
8) RS232 from the music keyboard

9) RS232 to and from a mouse

Four 68C681 DUARTs (U12, U13, U20 and U24) support these communic- ation channels.

U20 drives a 3.6864Mhz crystal, which when buffered by a 74HC240 (U23) is supplied to the other DUARTs. This clock is divided by the 68C681s to give the RS232 baud rates. A 1/2MHz clock is used as the MIDI 16 times clock.

The 68C681 duart has two transmit channels, and two receive channels. All channels have independent baud rates. An internal 16-bit counter can be programmed in a variety of ways to act as a timer, counter or frequency generator. An 8 bit output port is provided, with some of the bits being able to provide status information. A 6 bit input port can be read directly, or programmed to generate interrupts on either or both edges of a signal.

The 68C681 implements the full 68000 interrupt vectoring scheme, by providing the contents of an interrupt vector register to the 68000 during the interrupt acknowledge cycle.

2.10.1 ACIA1

(Refer schematic MFX010.004)

ACIA1 (U12) handles MIDI communications. MIDI to and from the CMI (port D) is handled by the "A" side, whilst MIDI from the music keyboard is received by side "B". The 1/2MHz clock is supplied to input pins IP2 to IP5, and the software configures these inputs to be the 16 times clock inputs. This duart can generate level 5 interrupts, enabling quick response to MIDI data.

2.10.2 ACIA2

(Refer schematic MFX010.004)

ACIA2 (U13) handles RS422 communications at 38k4 baud to Lynx synchronisers, or other synchronisers supporting the ES-buss. The Lynx synchroniser generates a square wave synchronised to the field edges of a video signal (SYSC on pin2 of U13), which can

be programmed to cause an interrupt in the MFX. It also handles the RS232 bidirectional channel available on the MFX expansion port. This duart can generate level 4 interrupts.

2.10.3 ACIA3

(Refer schematic MFX010.004)

ACIA3 (U24) handles RS232 communication to and from the CMI, and from the music keyboard or preh keyboard. Printer port #2 on CMI 317 has been removed from the rear panel of CMI 354-355 and instead sent to the MFX keyboard. This signal arrives at the receive pin of side "A". Side "A" transmit drives the alphanumeric keyboard input signal on the CMI, replacing the Preh or music keyboard when the MFX is installed. The RS232 keyboard output from the Preh or music keyboard is re-routed to the MFX keyboard, appearing at the receive input, side "B". This duart can generate level 3 interrupts.

2.10.4 ACIA4

(Refer schematic MFX010.005)

ACIA4 (U20) handles RS232 communications to and from a mouse using side "A". This mouse should be a serial mouse with a DB9 connector for attachment to the serial port of an IBM PC-AT. There are numerous software protocols possible. SIde "B" is unused. This duart can generate level 2 interrupts.

2.11 Interface drivers

(refer schematic MFX010.015 and 016)

MIDI is received using PC900 opto-couplers (U42, U43). This circuit is the circuit recommended by the MIDI specifications. The MIDI transmitter is a BC549 transistor (Q7), which makes this circuit more rugged than the usual 7407 open-collector transmitter circuit.

The tape synchroniser is interfaced using a DS8921 RS422 transmitter/ receiver pair (U41). The driver has a source impedance of 110Ω and a low-pass filter. The receiver has a

termination impedance of 110Ω at high frequency, increasing to high impedance at DC. Pull-up resistors cause the +ve input to see a higher voltage than the -ve input if the inputs are not being driven.

RS232 is driven by a 14C88 driver (U51), with all outputs filtered and output impedances of 110Ω. The voltage swing is +11V to -11V typically. A 14C89 receiver (U50) has termination impedances of 120Ω at high frequency, increasing to high-impedance at DC.

2.12 Speaker

(refer schematic MFX010.009)

Five of the output pins of ACIA2 (U13) are used to produce tones through the speaker of the MFX. Each output is connected to a different resistor and summed at a common node. The signal is then AC-coupled and low-pass filtered before reaching the non-inverting input of a power op-amp (U1). By turning a pot accessable from the underside of the MFX, the gain of the op-amp may be varied. The op-amp directly drives an 8Ω speaker.

Each output can produce an independent tone, with a volume level that depends upon the output used. The signal SL1 produced by OP3 (pin 13 of ACIA2) can be programmed to be a free-running square-wave derived from the internal counter. The other four outputs require that the processor toggle each bit directly.

2.13 Key scanning

(refer schematic MFX010.004 and 009)

The keys on the MFX keyboard are arranged into two sections. The 24 trigger keys (the 6 groups of 4 keys above the numbered function keys) are scanned by the 6309 processor. All other switches are scanned by the 68000. This section deals only with those keys which can be scanned by the 68000. See the section on the 6309 processor for details of the other switches.

The switches are arranged into banks, with each bank containing 8 switches. The bank address is written to the output register of

ACIA1 (U12), and the state of the 8 switches can then be read from the 74HC244 buffer (U3). A 1 in a switches bit position indicates that the switch is open (up), whilst a 0 indicates that the switch is closed (depressed).

The bank address consists of a 4-bit diode network number, and a 4-bit circuit board selection number.

Bit	Name	Function
7	—	unused (future expansion)
6	—	unused (future expansion)
5	ENPANEL	0= panel circuit board (MFX040) enabled 1= panel circuit board disabled
4	ENQWERTY	0= qwerty board (MFX030) enabled 1= qwerty board disabled
3	SWI3	} number of the active
2	SWI2	} diode-network on
1	SWI1	} each circuit board
0	SWI0	} (MFX030 and MFX040)

Fig 1. Switch bank address register (output port of U12)

Up to 24 switches may also be attached to the expansion port of the MFX keyboard. These switches are arranged into three banks of 8 switches. The state of the switches is read from the same switch register as the other switches. Bank 1, 2 or 3 is addressed by setting the signal SW0OUT, SW1OUT or SW2OUT respectively low. These signals are driven by OP0, OP1 and OP2 (pin 29, 12 and 28) of ACIA4 (U20) and are supplied directly to the expansion port.

2.14 Parallel mouse support

(refer schematic MFX010.004)

There is provision for the MFX to support a parallel mouse of the type used on the Macintosh® or Amiga® computers. By appropriately setting jumper block W4, the four quadrature

signals and up to two switch signals will be supplied to the input port of ACIA3. The input port can be programmed to generate interrupts on either or both edges of any of the quadrature signals.

2.15 Jogger wheel

(refer schematic MFX010.004)

The MFX supports the decoding of a mechanical or optical shaft encoder. The quadrature output of the encoder is pulled up and low-pass filtered before being buffered by a 74HC132 schmitt trigger (U14). The outputs of the schmitt trigger are fed to ACIA2 (U13), input port bits IP0 and IP1. The duart can be configured to cause an interrupt on the edges of the quadrature signal.

3. 6309 slave processor

(refer schematic MFX010.020)

The 6309P micro-processor (U58) is a CMOS version of the 6809P. The task of this processor is to interpret the signals from the hall effect sensors, and output information to the 68000 as to the velocity and position of the trigger keys. Only the 24 trigger keys are of interest to this processor, and the processor has no tasks other than to respond to these keys.

By seperating this very time critical task from the mass of less timing critical serial communication tasks that are handled by the 68000, the response and accuracy of the trigger keys is not affected by the load of other tasks that the MFX is handling. The 6309 is capable of carrying out its tasks without using interrupts, except when the timer overflows.

The circuitry has been designed to appear to the 68000 as a peripheral, which causes interrupts when it needs attention and delivers packets of information describing the changes in the state of the keys. Communications from the 68000 to the 6309 are slightly cumbersome, but communications in this direction only need to occur after reset.

3.1 Addressing

(refer schematic MFX010.020)

A 74HC138 demuliplexer (U36) is used to decode the 64K bytes of address space into 8 address spaces of 8K bytes each. The EPROM is the highest address space ($E000H to $FFFFH), as the 6309 fetches the interrupt and reset vectors from the top of memory. Other areas are used by the RAM, DAC, ADC, FIFO and VIA.

3.2 EPROM

(refer schematic MFX010.020)

An 8K by 8 bit 2764 EPROM (U52) with an access time of 250ns or better is used for the boot code. The EPROM is mapped from $E000H to $FFFFH as the 6309 processor fetches the reset and interrupt vectors from the top of memory.

3.3 RAM

(refer schematic MFX010.020)

An 8K by 8 bit 6264 static RAM (U44) is used for variable and program code storage. After reset, the 68000 downloads application code to the 6309, which places this code into the RAM. After the code has been downloaded, the 6309 will execute code out of this memory space.

3.4 Hall-effect data aquisition

(refer schematic MFX010.021)

The circuitry on the qwerty board (MFX030) outputs three signals IH1, IH2 and IH3. These signals are a current sink between 0 and 1mA proportional to the output of three of the hall effect sensors.

A current output DAC produces a current source of 0 to 500µA to offset the rest current produced by the hall sensor circuitry. The resulting current is summed at a node and converted into a voltage between 0 and 5V by an op-amp. This voltage is read by

an ADC, giving a value proportional to the position of a particular key.

3.4.1 DAC

(refer schematic MFX010.021)

The DAC is a AD7524 resistive divider (U34). If both outputs are held at 0V, then the current in signal IOUT1 (pin 1) is proportional to the input code. By writing a value from $00H to $FFH, the output of the DAC may be set from 0 to 500µA respectively. As the hall effect circuitry in its rest state acts as a current sink of less than 500µA, the signal from the hall effect sensor can be completely nulled.

The address space used by the DAC is also a copy of the RAM address space. A write to the DAC also has the effect of writing to the RAM, while a read to the DAC address space loads the value in RAM into the DAC and a 6309 register. In this way, a table of offset values in RAM can be used and maintained while accessing the DAC at the same time.

3.4.2 ADC

(refer schematic MFX010.021)

The ADC is an ADC7820 half-flash converter (U28). The ADC has an inherent sample and hold function, as the conversion is a two stage flash process. An input voltage between 0V and 5V can be converted to an 8-bit result which can be read about 2.5µs after the beginning of the conversion. A read to the address of the ADC starts the conversion, and the ADC asserts MRDY09 low causing the 6309 to halt until the end of conversion. At the end of conversion MRDY09 is released, causing the read instruction to terminate with the result of the conversion.

An AD711 fast settling op-amp (U33) is used to convert the current signal into a voltage which can be read by the ADC. A 5V6 zener diode in the feedback loop of the op-amp prevents the output voltage from exceeding the 0V to 5V input range of the converter. A 47pF capacitor in the feedback loop and a series of passive low-pass filters are used to eliminate high frequency

noise from the signal.

3.5 VIA

(refer schematic MFX010.022)

A 65C22 **V**ersatile **I**nterface **A**dapter (U19) provides 16 parallel outputs and a 16-bit timer/counter. The 8-bit port "B" is configured as outputs to set up the address of the active hall effect sensor (signals HA0 through HA7). Side "A" bit 7 (pin 9) is the input signal HS which represents the state of the currently addressed switch. If HS is low then the switch is depressed, otherwise the switch is open.

The interface from the 68000 to the 6309 is conducted through side "A" of the VIA. Signals TH0 through TH6 (pins 2 through 8) carry the 7-bit data, with DT and DR (pins 39 and 40) being used for the handshaking. Seven bits of data makes the software protocol slighly more complicated than it could have been, but this interface should only be used during the downloading of software.

The VIA can generate /FIRQ interrupts to the 6309 processor. There are a large range of conditions which can be programmed to generate interrupts, but when the application code is executing then interrupts should only occur when the timer overflows. Following reset, the handshake signals generate interrupts to signal that another data word is available.

3.6 Key addressing

(refer schematic MFX010.022 and 040)

The trigger keys are arranged into three banks of 8 keys. The address of the active trigger key is set up by the 8-bit code HA0 through HA7. HA[0,1] are fed to the 74HC4052 analog muliplexer (U22) which selects the active bank of trigger keys. HA[2,3,4] selects the active key in banks 1 and 2. HA[5,6,7] selects the active key in bank 3.

Optimal speed from the hardware can be obtained by one reading key from each bank before selecting a new active key. By being

able to select the active key in bank 3 independently from banks 1 and 2, the circuitry on the qwerty board (MFX030) can be allowed to settle whilst a key in another bank is being read. The circuitry on the controller and qwerty boards never needs to settle at the same time.

4. Inter-processor communications

The 6309 can communicate with the 68000 using a 15 byte deep FIFO. The allows the 6309 to send its messages to the 68000 without having to wait for the 68000 to respond. In normal operation, the FIFO should not fill completely.

At power-up, the 68000 downloads code to the 6309 using a 7-bit latch and handshaking. This communication is interrupt driven on both sides, but only occurs at power-up. (Note: future releases of the software may involve the 68000 communicating with the 6309 at times other than at power-up).

4.1 FIFO

(refer schematic MFX010.030)

There is a 15 byte deep FIFO allowing communication from the 6309 processor to the 68000. The FIFO consists of two 74HCT40105 4-bit FIFOs (U29 and U30) in parallel. When the 6309 writes to the FIFO, the byte loaded into the FIFO falls through to the output. If the FIFO becomes full as a result of the write (i.e. 16 writes without a read by the 68000) the MRDY09 signal is asserted low halting the 6309 until the 68000 reads a byte from the FIFO. When the 68000 does this read, the write instruction of the 6309 will complete. In this way, no information can be lost when the FIFO overflows. The 6809 processor has dynamic registers which are corrupted if MRDY09 is asserted for more than 16µs. If a 6809 processor is used instead of a 6309 processor, then the FIFO should assert /HALT instead of /MRDY (this will require a mod to the circuit).

When a byte is written to the FIFO, /IRQ6 on the 68000 is

asserted low causing a level 6 interrupt (assuming that interrupts are not masked). /IRQ6 will remain low until all the bytes are read from the FIFO. The state of /IRQ6 can be read from ACIA4, IP0 (pin 7). Because the FIFO is at the highest interrupt level, the FIFO should not become full and the 6309 will continue execution of instructions.

The FIFOs have an active high reset (pin 9) which is driven by FIFOR. If FIFOR is high, then the FIFO is cleared preventing the FIFO from generating interrupts or overflowing. FIFOR is generated by ACIA4, OP6 (pin 26). On reset, FIFOR is high.

4.2 Handshake register

(refer schematic MFX010.004 and 022)

For communications from the 68000 to the 6309, a 7 bit port with hand- shaking is provided. The 68000 signals that new data has been placed on the port by asserting DR (data-ready) low. After reading the data, the 6309 asserts the signal DT (data-taken) low.

The 68000 processor writes to the port by setting up the data on ACIA3 (U24), OP0 through OP6 (pins 29, 12, 28, 13, 27, 14, 26). DR is driven by ACIA2 (U13), OP2 (pin 28). DT can be read from ACIA1 (U12), IP1 (pin 4). ACIA1 can be programmed to generate an interrupt to the 68000 on the falling edge of DT.

The 6309 processor can read the data from the port by reading the VIA (U19), PA0 through PA6 (pins 2 through 8). DR is available at CA1 (pin 40) and this can be used to generate an interrupt on the falling edge of DR. DT is driven by CA2 (pin 39). The VIA has a handshake mode which automatically generates the required protocol.

5. Power supplies

(refer schematic MFX010.035)

The MFX receives all its power from the +20V and -20V keyboard power signals generated from the CMI-310 Audio Power Supply in

the CMI. The supplies are regulated using 78 and 79 series linear regulators. These regulators feature short-circuit and over-temperature shutdown. Heat is dissipated by convection cooling within the MFX console, and by heat-sinking to the rear panel of the MFX unit.

The regulated +5V supply is generated by a 7805 regulator, and is used by all the digital circuitry and the hall effect sensors. A regulated supply of -5V is used by the current mirrors and the 74HC4051 and 74HC4052 analog multiplexers. The regulated +12V supply is used by the op-amps and the RS232 driver. The -12V supply is used by the op-amps, the RS232 driver and the backlight of the LCD display. A special supply, called VLED, is generated by a 7812 regulator for use by the LED circuitry. The output of this 7812 regulator is passed through a 1Ω 5W resistor into a 15000μF capacitor. This large capacitor serves as a reservior of power for the LED circuitry, as the LED circuitry may require 1.6A for 1ms followed by 0A for 7ms.

All five supplies are connected to a row of five yellow LEDs. These LEDs should glow with equal brightness if the power supplies are functioning.

The expansion port is designed to cope with future expansion needs of the MFX console. The port has the +12V and -12V supplies to power external circuitry. A special +5V supply is available on the expansion port which has a current limit of 100mA. This supply is intended to be connected to one end of the faders (the other end is connect to GND). The wipers of the faders are then attached to the signals FADER0 through FADER7.

Typical power consumption is approximately 500mA on +20V if no LEDs are lit. Of this 500mA, approximately 300mA is used by the hall effect sensors. If all the LEDs are lit then power consumption rises to 1A. From the -20V supply approximately 200mA is drawn regardless of what the MFX is doing. Almost all this current is used by the backlights of the LCD displays.

Peripherals attached to the expansion port are capable of drawing current from the MFX and increasing the power consumption accordingly.

6. MFX030 Qwerty board.

(Refer schematic MFX030.001 to 005)

The Qwerty board supports and decodes the qwerty keyboard, the function keys and the sound trigger keys. It receives power from MFX010 through a 10-way Molex connector, and communicates with MFX010 (in parallel with MFX040) through a 50-way IDC connector.

The sound trigger keys are scanned by the 6309 processor on MFX010, whilst all other switches are scanned by the 68000 processor. For this reason, the circuitry for these two sections of MFX030 are seperate and different.

6.1 Qwerty switches and function keys.

(refer schematic MFX030.001)

The qwerty and function keys are decoded using a diode matrix, with an active row/column scheme. This allows infinite key roll-over to be implemented. The diodes are contained in 11 common cathode diode networks (DN1 through DN11). The cathodes of these diode networks are connected to the outputs of two 74HC138 8-channel multiplexors (U1 and U2). If the signal ENQWERTY is low, then the signals SWI0 through SWI4 set which of the 11 (plus 5 unused) outputs will be low. The signals SWO0 through SWO7 are pulled up to +5V by resistors on MFX010. Thus only one diode network will have its cathode near GND, allowing its diodes to conduct if the attached switches are closed.

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MFX CONSOLE DIAGNOSTICS

24 November 1992

1. To reset the non volatile RAM in the MFX console switch OFF power and hold down numeric keypad keys 1:2:3. Switch on power while keys are depressed. Go to the shell from MFX project screen by typing "SHIFT" $ <ret>. At the # type "mfxload" <ret>. The system will load the non volatile RAM. When operation is complete depress "ESC" key.

2. To enter diagnostics on the MFX console hold down numeric keypad keys 4:5:6. Switch on power while keys are depressed. Release keys when you are ready to enter diagnostics. Depress F1:F3:F5:F7 to exit test.

TEST NUMBER	TEST DESCRIPTION
0	LCD, 68000 RAM, LED circuits
1	Raw Keyboard Test
2	ASCII keyboard Test, depress keys and check LCD display
3	Jogger and Mouse X axis / Y axis
4	N/A
5	N/A
6	N/A
7	Speaker level test. Adjustment on under side of console
8	RS422 / N/A
9	Return MFX console to MFX operation

To set LCD contrast adjust pre set on under side of console.

3. Depressing keys -:÷:BLUE will set console for software up load. This does not reset the non volatile RAM as in point 1.

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