25.0 MFX Console

25.1 MFX010 Conroller Card Description

The MFX keyboard is a console designed to facilitate the use of post-production software on the MFX.

The MFX keyboard contains two circuit boards. MFX010 is the controller board for the MFX console, containing the Microprocessor. The other board, MFK, is used to decode the switches and trigger keys.

25.1.1 68000 Master Processor

(refer schematic MFX010-CPU (page 2 of 8))

The 68000 is responsible for the processing tasks in the MFX as it handles every task including scanning the 24 trigger keys. It has ROM, RAM and non-volatile RAM to store and execute programs and data.

The peripherals of the 68000 are memory mapped in the usual way with the high bits of the address buss determining the active peripheral. Each peripheral capable of generating interrupts is assigned to a different interrupt level.

25.1.2 ROM's

(refer schematic MFX010-MEMORY (page 3 of 8))

Two 8 bit EPROM's are used in parallel to provide the 16-bit boot code required by the 68000. These EPROM's are 27256 varieties with access times of 170ns or better. When accessing these EPROM's, no wait states are required by the 68000 allowing full-speed operation.

On power-up or after a reset, the EPROM's are mapped at location 0, as this is where the 68000 loads its initial stack pointer and program counter. The EPROM's can also be accessed at location $100000H. By setting the signal OVLY low (U9 pin 17) the EPROM is mapped out of location 0 and replaced by static RAM. This allows the exception vector locations to be modified by software. The OVLY signal is set high by reset. Regardless of the state of OVLY, the EPROM's may be accessed starting at $100000H.

The first instruction of the EPROM is to set OVLY low. If this does not occur then the processor is probably not able to execute any instructions. If the processor does not even load the stack pointer and program counter then the problem is very fundamental, and is not simply problems with the address or data lines.

25.1.3 RAM

(refer schematic MFX010-MEMORY (page 3 of 8))

Four 8-bit static RAM's are used in parallel to provide the 16-bit wide memory space in which to execute code. Normally 256K-bit RAM's are installed giving 64K words of memory. The memory is mapped starting at location 0. This allows direct access to the 68000 exception vectors, which occupy the first $200H words.

On power-up or reset, the signal OVLY is high, mapping the EPROM's to location 0 and preventing access to the RAM's. Normally, the first instruction executed is sets OVLY low, mapping the RAM to location 0. OVLY should remain low until power is removed or the

processor is reset.

The MFX keyboard has been designed to allow downloading of software from the Series III CMI, eliminating the need for costly EPROM updates. The task of the boot code in the EPROM's is to move the application code from the non-volatile memory to the RAM for execution.

25.1.4 Non-volatile RAM

(refer schematic MFX010-MEMORY (page 3 of 8))

Three 8K by 8-bit static RAM with battery-backup is provided to store programs configuration setups and data. This RAM is protected by a DS1234 non-volatile controller (U38), which controls write-protection and battery usage. The memory may be configured to be read-only or read-write and volatile or non-volatile. Normally the memory is kept as ready-only non- volatile memory, and changed to- read-write memory only when the data is being changed.

As this memory space is only 8 bits wide, it is not possible to execute programs directly from this RAM. At a temperature of 25'C, the BR2325 battery should provide a life of 8 years. Care should be taken to avoid exposing the MFX to extremes of temperature for long periods of time, as elevated temperature decreases the battery life rapidly.

At the time of writing this document, 100% CMOS RAM's are only made by Toshiba and are proving difficult to obtain. However they offer such low stand-by currents that they would offer non-volatility for the shelf life of the battery (> 10 years).

There is a jumper block provided which allows selection of a variable number of wait states for the non-volatile RAM - either 0, 2, 4 or 6 wait states. This may be necessary as the DS1234 shortens the access times of- the RAM by around 30ns. The actual setting used depends on the speed of the installed static RAM.

25.1.5 Address Decoding

(refer schematic MFX010-CPU (page 2 of 8))

The address decoding is performed by two 74ACT138 demultiplexers (U21 and U26) and half of a 74HCT138 demultiplexer (U27). The 16 megabyte memory space of the 68000 is divided up into sixteen 1 megabyte areas by the two 74ACT138, with each register or peripheral given ifs own area. All the peripherals decoded by U26 are no wait-state devices, whilst those decoded by U21 must supply an open collector /DTACK signal.

The second last address space is supplied to the 74HCT138, which subdivides this space into four areas for use by peripherals which require synchronization to the 1MHz E clock of the 68000. The /CS6800 signal tells the 68000 to synchronise to the E clock by, asserting VPA low whenever this address range is selected. The highest 1 megabyte address space should be left vacant, as this space is selected whenever an interrupt acknowledge cycle is commenced.

/DTACK is generated by all four DUARTs (U7, U8, U9 and U10) and by the 74HC175 (U33). Whenever the demultiplexer U26 is selected, U33 is reset causing /DTACK to be asserted low. Whenever the non-volatile RAM is selected, the select signal is shifted through the flip-flops of U33 on the rising edge of PCLK (10MHz) until is appears at the link block (W4) causing /DTACK to be asserted low.

25.1.6 LED Circuitry

(refer schematic MFX010-DISPLAY (page 6 of 8))

The LED's controlled by the MFX are arranged into rows and columns, and lit using a multiplexed scheme. Under this scheme each LED is pulsed on for 1ms with a high current, and then turned off for 7ms. By pulsing the LED its efficiency is improved and the drive circuitry is simplified.

The 16 columns are controlled by two 74HC273 latches (U37and U38). If a bit is set to high, then the corresponding column is active. The columns are driven by two UDN2981A high-current source drivers (U29 and U30) and the current set by the 100R 1W resistors. The outputs of the source drivers are either VLED (+12V) if they are driven or floating if they are off.

The 8 rows are controlled by a 74HC164 shift-register (U19). This register is arranged as a circulating buffer with one bit high (the active row) and the other bits low. Every time an access is made to the column register, the active row is incremented. Two ULN2803A Darlington drivers (U15 and U12) drive the rows in parallel. The outputs of the drivers are either around 1 volt if driven or floating if they are off.

The circuitry has been designed to work optimally if the LED column register is accessed every 1ms. This speed ensures that the blinking of the LED's (125Hz) is faster than the human eye. If a Led were to be driven by this circuitry continuously then it would burnout because the driving currents are greater than the maximum allowable average current through the LED's. To prevent this undesirable event, protection circuitry has been installed to turn off the LED's if the column register is not accessed for 3ms. This protection circuitry consists of a 74HC123 dual monostables (U44 and U50) and a flip-flop (U31B). If a fault condition is detected then U37, U38 and U19 are reset, and the signal START goes high. When the LED register is next accessed, START supplies the initial conditions to drive output QH of U19 high. If the next row to become active will be ROWO then the signal CHECK will be high. This signal is available at ACIA2 (U10), input port signal IP4 (pin 43). The software should check this signal to determine if it agrees with what software expects. If a disagreement is detected, the software should immediately write a 0 to the LED column register and wait 10ms. If the signal CHECK is now high, the LED scanning may resume; otherwise the software should disable LED scanning and inform the user.

25.1.7 Clocks

(refer schematic MFX010-CPU (page 2 of 8))

A 10MHz oscillator (OSC1) supplies the main system clock, PCLK. The 68000 divides this signal by 10 to give the 1MHz E clock (6:4 duty cycle) used by slow synchronous peripherals (displays). The E clock is divided by a flip-flop (U31) to give a 1/2 MHz square wave. The 1/2 MHz clock is used by DUART U7 as the 16 x MIDI clock. A 3.6864MHz clock is generated by DUART U8 for use in generating RS232 baud rates. See the section on the DUARTS for more information.

25.1.8 Watchdog

(refer schematic *MFX010-CPU (page 2 of 8))*

A DS1232 watchdog (U45) is used to supervise the operation of the MFX keyboard. It drives the open collector /RESET and /HALT signals low whenever the +5V power supply is out of

range (4.76V to 5.25V), if the optional reset button has been pressed (connector J11), or if, the watchdog has not been accessed by the 68000 for 100ms. The 68000 requires both /RESET and /HALT to cause it to reset. If the 68000 does a double buss fault (e.g. loading an odd address pointer during an exception vector fetch) then it will drive /HALT low. If the 68000 executes a reset instruction, then it will drive /RESET only low. Both /RESET and /HALT also drive low-current red LED's (LD6 and LD8). If both LED's light simultaneously, then it is likely that the watchdog is driving these lines. However if the /HALT LED lights marginally before the /RESET LED then it is likely that the 68000 has had a double buss fault. This would occur if the ROM's were corrupt or if there was a serious problem with the address or data buss. If the green LED (LD7) remains lit, then the 68000 is executing code and keeping the watchdog at bay. If the green and red LED's light alternately, then the 68000 is not executing correct code.

25.1.9 Displays

(refer schematic MFX010-DISPLAY (page 6 of 8))

The MFX keyboard supports the attachment of two LM402B01 displays. These displays each offer 40 columns by 2 rows with up to 8 custom characters. The display is backlit by yellow LED's, which shine through the characters (clear characters on a black background). The data buss, address buss and R/W are buffered (74HCT245 at U36 and elsewhere) before driving the display signal cables (J8 and J9). The backlight is driven from 12V, as very little other use is made of the negative supply capacity of the MFX. A contrast adjustment pot is accessible from the top right hand corner of the MFX keyboard. Before concluding that a display is faulty because nothing is visible, you should check the contrast adjustment.

25.1.10 DUARTs

(refer schematic MFX010-DUARTS & DRIVERS (page 4&5 of 8))

The MFX supports serial communications with the following devices:

1. MIDI to MIDI D on the MFX
2. MIDI from MIDI D on the MFX
3. Midi from the Fairlight music keyboard
4. RS422 to and from a LYNX synchroniser or other synchroniser supporting the ES Bus
5. RS232 to and from an MFX expansion device
6. RS232 to the MFX keyboard input
7. RS232 from printer port 2 on the MFX (this port is no longer an external connector)
8. RS232 from the music keyboard
9. RS232 to and from a mouse

Four 68C681 DUARTs (U7, U8, U9 and U10) support these communication channels.

U8 drives a 3.6864Mhz crystal, which when buffered by a 74HC240 (U6H) is supplied to the other DUARTs. This clock is divided by the 68C681s to give the RS232 baud rates. A 1/2MHz

clock is used as the MIDI 16 times clocks.

The 68C681 DUART has two transmit channels, and two receive channels. All channels have independent baud rates. An internal, 16-bit counter can be programmed in a variety of ways to act as a timer, counter or frequency generator. An 8-bit output port is provided, with some of the bits being able to provide status information. A 6 bit input port can be read directly, or programmed to generate interrupts on either or both edges of a signal.

The 68C681 implements the full 68000 interrupt vectoring scheme, by providing the contents of an interrupt vector register to the 68OOO during the interrupt acknowledge cycle.

25.1.11 AC1A1

(refer schematic MFX010-DUARTS (page 4 of 8))

AClA1 (U7) handles MIDI communications. MIDI to and from the MFX (port D) is handled by the “A” side, whilst MIDI from the music keyboard is received by side “B”. The 1/2MHz clock is supplied to input pins IP2 to IP5, and the software configures these inputs to be the 16 times clock inputs. This DUART can generate level 5 interrupts, enabling quick response to MIDI data.

25.1.12 ACIA2

(refer schematic MFX010-DRIVERS (page 5 of 8))

AClA2 (U10) handles RS422 communications at 38k4 baud to Lynx synchronisers, or other synchronisers supporting the ES-buss. The Lynx Synchroniser generates a square Wave synchronised to the field edges of a video signal (SYSC on pin3 of U10), which can be programmed to cause an interrupt in the MFX. It also handles the RS232 bi-directional channel available on the MFX expansion port. This DUART can generate level 4 interrupts.

25.1.13 ACIA3

(refer schematic MFX010-DUARTS (page 4 of 8))

ACIA3 (U8) handles RS232 communication to and from the MFX. Side “A” transmit drives the alphanumeric keyboard input signal on the MFX. The RS232 keyboard output from the MFX appears at the receive input, side “B”. This DUART can generate level 2 interrupts.

25.1.14 ACIA4

(refer schematic MFX010-DUARTS (page 4 of 8))

ACIA4 (U9) handles RS232 communications to and from a mouse using side “A”. This mouse should be a serial mouse with a DB9 connector for attachment to the serial port of an IBM PC-AT. There are numerous software protocols possible. Side “B” is unused, This DUART can generate level 2 interrupts.

Interface drivers

(refer schematic MFX010-DRIVERS (page 5 of 8))

MIDI is received using PC900 opto-couplers (U1, U2). This circuit is the circuit

recommended by the MIDI specifications. The MlDI transmitter is a BC549 transistor (Q7), which makes this circuit more rugged than the usual 7407 open-collector transmitter circuit. The tape synchroniser is interfaced using a DS8921 RS422 transmit receiver pair (U3), The driver has a source impedance of 110ohm and a low-pass filter. The receiver has termination impedance of 110ohm at high frequency, increasing to high impedance at DC. Pull-up resistors cause the +ve input to see a higher voltage than the -ve input if the inputs are not being driven. RS232 is driven by a 14C88-driver (U4), with all outputs filtered and output impedance's of 110 ohm. The voltage swing is +11V to -11V typically. A 14C89-receiver (U5) has termination impedances of 120 ohm at high frequency, increasing to high-impedance at DC.

25.1.15 Speaker

(refer schematic MFX010-DRIVERS (page 5 of 8))

Five of the output pins of AClA2 (U10) are used to produce tones through the speaker of the MFX. Each output is connected to a different resistor and summed at a common node. The signal is then AC-coupled and low-pass filtered before reaching the non-inverting input of a power op-amp (U14). By turning a pot accessible from the top right hand corner of the MFX, the gain of the op-amp may be varied. The op-amp directly drives an 8ohm speaker. Each output can produce an independent tone, with a volume level that depends upon the Output Used. The Signal SL1 produced by OP3 (pin 15 of ACIA2 (U10)) can be programmed to be a free running square-wave derived from the internal counter. The other four outputs require that the processor toggle each bit directly.

25.1.16 Key scanning

(refer schematic MFX010.004 and 009)

The switches are arranged into banks, with each bank containing 8 switches. The bank address is written to the output register of ACIA1 (U7), and the state of the 8 switches can then be read from the 74HC244 buffer (U11). A 1 in a switches bit position indicates that the switch is open (up), whilst a 0 indicates that the switch is closed (depressed). The bank address consists of a 4-bit diode network number, and a 4-bit circuit board selection number.

7		unused (future expansion)
6		unused (future expansion)
5	ENPANEL	0 panel key (MFK panel keys) enabled 1 panel key disabled
4	ENQWERTY	0- qwerty key (MFK qwerty keys) enabled 1= qwerty key disabled
3	SWI3	number of the active
2	SWI2	diode-network on
1	SWI1	each circuit board
0	SWI0	(MFX030 and MFX040)

Fig 1. Switch bank address register (output port of U7)

25.1.17 Jogger wheel

(refer schematic MFX010-DRIVERS (page 5 of 8))

The MFX supports the decoding of an optical shaft encoder. The quadrature output of the encoder is pulled up and low-pass filtered before being buffered by a 74HC132-schmitt-trigger (U18). The outputs of the Schmidt trigger are fed to ACIA2 (U10), input port bits IPO and lP1. The DUART can be configured to cause an interrupt on the edge of the quadrature signal.

25.1.18 MFK Qwerty board.

(Refer schematic MFK)

The MFK board supports and decodes the QWERTY keyboard, the function keys and the panel trigger keys. It receives power from MFX010 through a 10-way Molex connector, and communicates with, MFX010 through a 50-way lDC connector. The panel trigger keys and all other switches are scanned by the 68000 processor.

25.1.19 Qwerty, Panel trigger switches and function keys.

(refer schematic MFK-MFX console key panel)

The QWERTY, function and panel keys are decoded using a diode matrix, with an active row/column scheme. This allows infinite key roll-over to be implemented. The diodes are contained in 25 common cathode diode networks (DN1 through DN25).

25.1.20 Qwerty

(refer schematic MFK-qwerty keys 1 to 4)

The QWERTY keys are arranged into 4 banks (qwerty1, qwerty2, qwerty3, and qwerty4). The address of the active QWERTY key is set up by the 12-bit code SWQ0 through SWQ12. SWQ0-3 selects qwerty1, SWQ4-7 selects qwerty2, SWQ8-11 selects qwerty3, and SWQ12 selects qwerty4.

The anodes of the QWERTY diode networks are connected to the outputs of two 74HC138 8-channel multiplexors (U3 and U4). If the signal ENQWERTY is low, then the signals SWI0 through SWI3 set which of the 12 (plus 4 unused) outputs SWQ0 through SWQ15 will be low.

25.1.21Panel

(refer schematic MFK-panel keys 1 to 4)

The PANEL keys are arranged into 4 banks (panel1, panel2, panel3, and panel4). The address of the active PANEL key is set up by the 14-bit code SWP0 through SWP13. SWP0-3 selects panel1, SWP4-7 selects panel2, SWP8-11 selects panel3, and SWP12-13 selects panel4.

The anodes of the PANEL diode networks are connected to the outputs of two 74HC138 8-channel multiplexors (U2 and U1). If the signal ENPANEL is low, then the signals SWI0 through SWI3 set which of the 14 (plus 2 unused) outputs SWP0 through SWP15 will be low.

The signals SWOO0 through SWO7 are pulled up to +5V by resistors on MFX010. Thus only

one diode network will have its cathode near GND, allowing its diodes to conduct if the attached switches are closed.

25.2 MFX CONSOLE DIAGNOSTICS

1. To reset the non-volatile RAM in the MFX console switch OFF power and hold down numeric keypad keys 1:2:3. Switch on power while keys are depressed. Go to the shell from MFX project screen by typing “SHIFT” $ <ret>. At the # type “mfxload” ret>. The system will load the non-volatile RAM. When operation is complete depress “ESC” key.

2. To enter diagnostics on the MFX console hold down numeric keypad keys 4:5:6. Switch on power while keys are depressed. Release keys when you are ready to enter diagnostics. Depress Fl:F3:F5:F7 to exit test.

TEST NUMBER	TEST DESCRIPTION
0	LCD, 68000 RAM, LED circuits
1	Raw Keyboard Test
2	ASCII keyboard Test, depress ‘keys and Check LCD display
3	Jogger and mouse X axis / Y axis
4	N/A
5	N/A
6	NIA
7	Speaker level test. Adjustment on top right corner of console
8	RS422 / N/A
9	Return MFX console to MFX operation

To set LCD contrast, adjust preset on top right corner of console.

3. Depressing keys -:+:BLUE will set console for software up load. This does not reset the non-volatile RAM as in point 1.

CABG8529 - MFX Plus Cable Assembly

REV.	DATE	DESIGNED BY	DESCRIPTION	PCO	ZONE
1.0	5/8/96	L.Stewart	RELEASE		
1.1	16/1/97	L.Stewart	Cable spec and connections		
1.2	7/12/98	N.Plummer	Rotated drawing to match connection drawing. Corrected title name.		

NOTE :

1. Cable to be to the following specification;
   12 Pair + Drain Twisted Pair
   7/0.02mm Stranded Cores
   RS422 Hi Speed Data (50pF/m)
   Low Impedance & Braided Screen
   e.g. MCP-12S/BS (supplier A.G.Garland)
2. Refer to Dwg # CABC8529.DW2 for connections
3. Refer to supplied documentation for additional information regarding termination of cable screens
4. Ferrites to be FairRite P/N 2643626402 Fairlight P/N FERB0110)
5. Cover ferrites with heatshrink

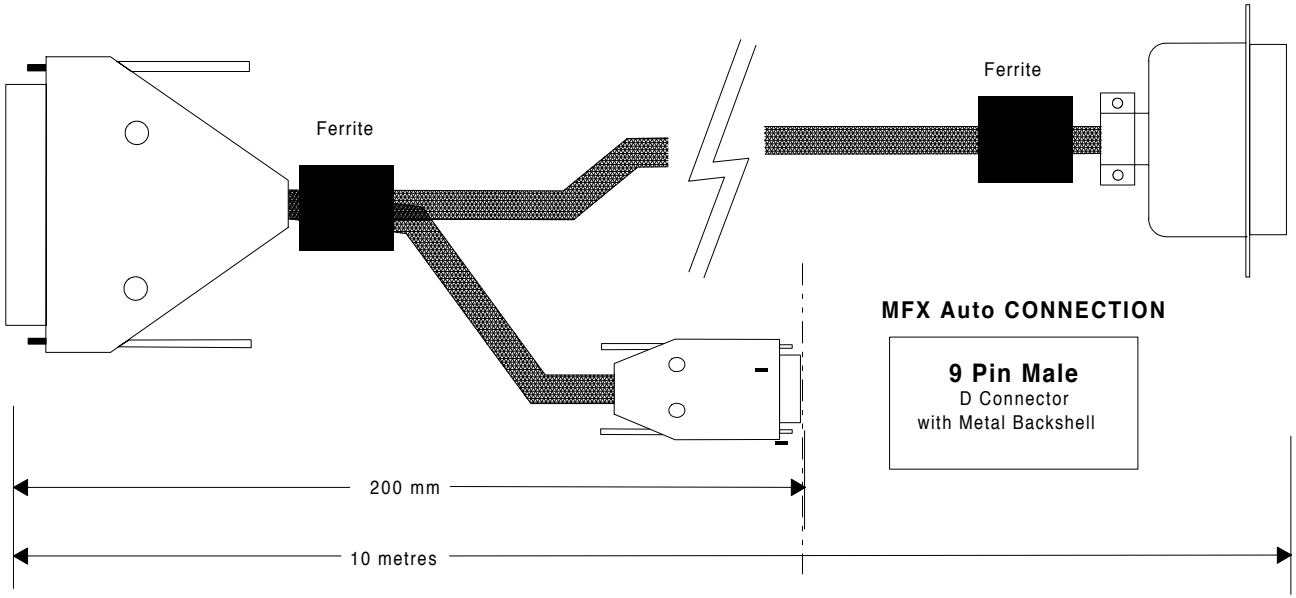
See also related connection drawing
Cabg8529 MFXP 1 of 2 Connect rev 1-3.dc

MAINFRAME CONNECTION

24 Pin Male
Centronics Connector
with Metal Backshell

CONSOLE CONNECTION

37 Pin Male
D Connector
with Metal Backshell



MFX Auto CONNECTION

9 Pin Male
D Connector
with Metal Backshell

DIMENSION UNITS: mm	DESIGNED BY ENGINEERING: L.Stewart	TITLE: CABG8529 - MFX Plus Cable Assembly	REV. 1.2
TOLERENCE: ± 3%	APPROVED BY ENGINEERING		
FILE NAME: CABG8529.DW2	APPROVED BY PRODUCTION	FILE NAME: Cabg8529 MFXP 1 of 2 Assy rev 1-2.dc	
	APPROVED BY QUALITY CONTROL	SCALE N.T.S. / SHEET 1 OF 1 / COMPANY CONFIDENTIAL	

CABG8529 - MFX Plus Cable Connection Diagram

REV.	DATE	DESIGNED BY	DESCRIPTION	PCO	ZONE
1.0	16/12/96	L.Stewart	RELEASE		
1.1	16/1/96	L.Stewart	Cable Spec & Connections		
1.2	27/8/98	M.Paolino	Signal names corrected (Midin / out)		
1.3	7/12/98	N.Plummer	Previous change reversed. Signal names changed to PCB name at each end. Corrected part number in title.		

NOTES :

** Assumes this signal when appropriate jumper is in place

1. Cable is to be to the following specification;
   14 Pair + Drain Twisted Pair
   7/0.02 Stranded cores
   RS422 HI SPEED Data (50pF/m)
   LOW IMPEDANCE
   Braided screen
   e.g. MCP-12S/BS (Supplier: A.G. Garland)

See also related assembly drawing
Cabg8529 MFXP 2 of 2 Assy rev 1-2.dc

Console Connection

37 Pin Male
D Connector
with Metal Backshell
UL Recognised
(Connects to J2 on MFX010)

Signal Name (MFX010 PCB)	Connector Pin No.	Colour	Mandatory	Connector Pin No.	Signal Name (ESP-MIDI PCB)	
FS+	13	Brown	Yes	5	X422+	Pair
FS-	31	Brown/White	Yes	17	X422-	
TS+	12	Grey	Yes	6	R422+	Pair
TS-	30	Grey/White	Yes	18	R422-	
MO1+	8	Green		10	Mid+	Pair
MO1-	26	Green/White		22	Mid-	
MI1+	9	Blue		9	MOut+	Pair
MI1-	27	Blue/White		21	MOut-	
MI2+	11	Orange		7	n/c	Pair
MI2-	29	Orange/White		19	n/c	
RSI1	6	Brown	Yes	12	Data2	Pair
Gnd	21	Brown/Black	Yes	14	Gnd **	
RSI2	7	Grey		11	Data1 **	Pair
Gnd	20	Grey/Black	Yes	13	Gnd **	
RSO2 **	25	Green		23	KEYBDOUT**	Pair
n/c	16	Green/Black		15	n/c	
Gnd	10	Green	Yes	8	*MFXPresent	Pair
SYSC	28	Green/Yellow		20	n/c	
RSO1	24	Orange	Yes	24	Datain	Pair
Gnd	23	Orange/Black	Yes	16	Gnd **	
n/c	2	Grey		2	n/c	Pair
n/c	4	Grey/Red		3	n/c	
Gnd	1	Green	Yes	1	Gnd **	Pair
n/c	14	Green/Red		4	n/c	
MRXD	36	(any)	Yes	2	(MRXD)	
MTXD	37	(any)	Yes	3	(MTXD)	
Gnd	33	(any)	Yes	5	Gnd	

Mainframe Connection

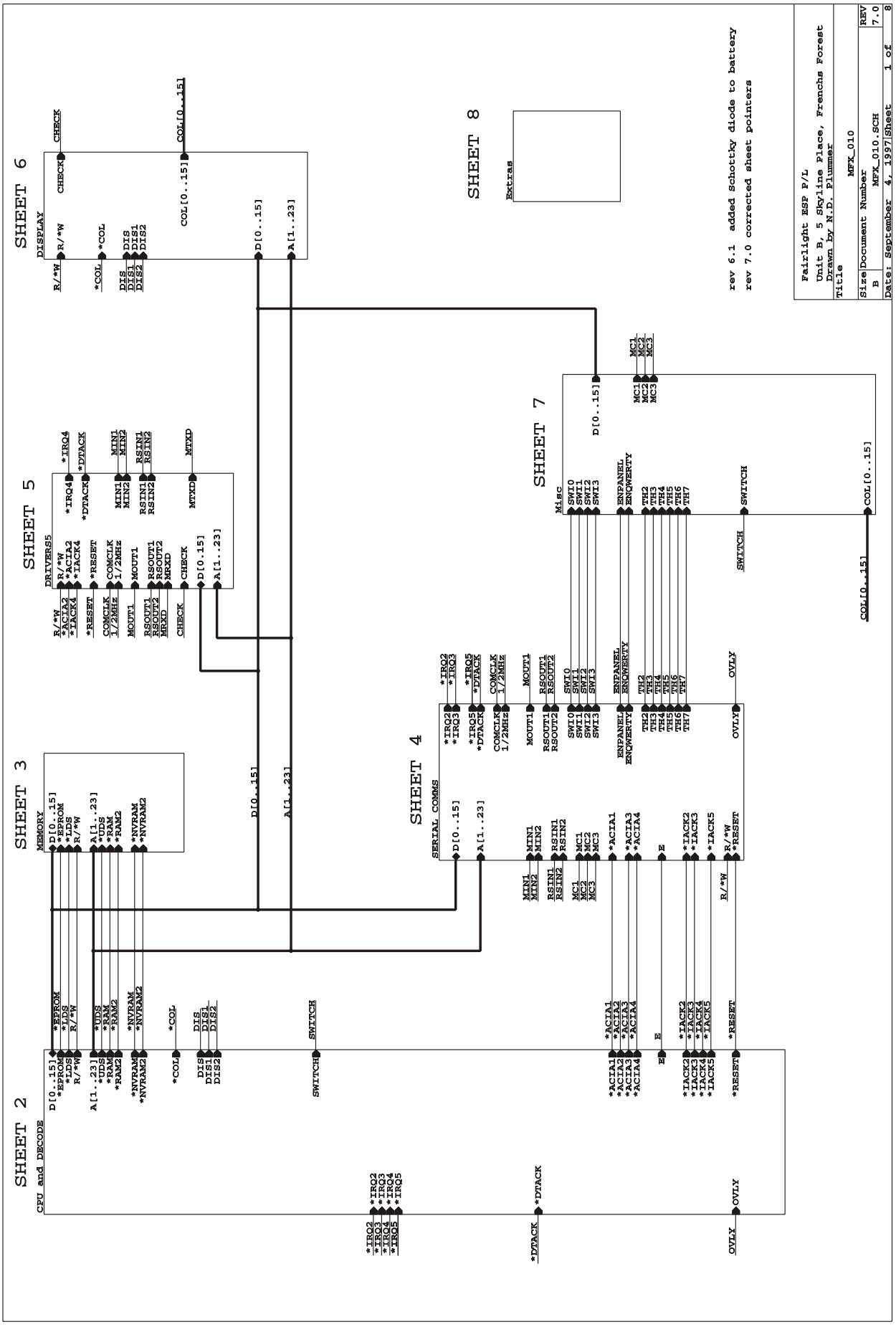
24 Pin Male
Centronics Connector
with Metal Backshell
UL Recognised
(Connects to P5 on ESP-MIDI)

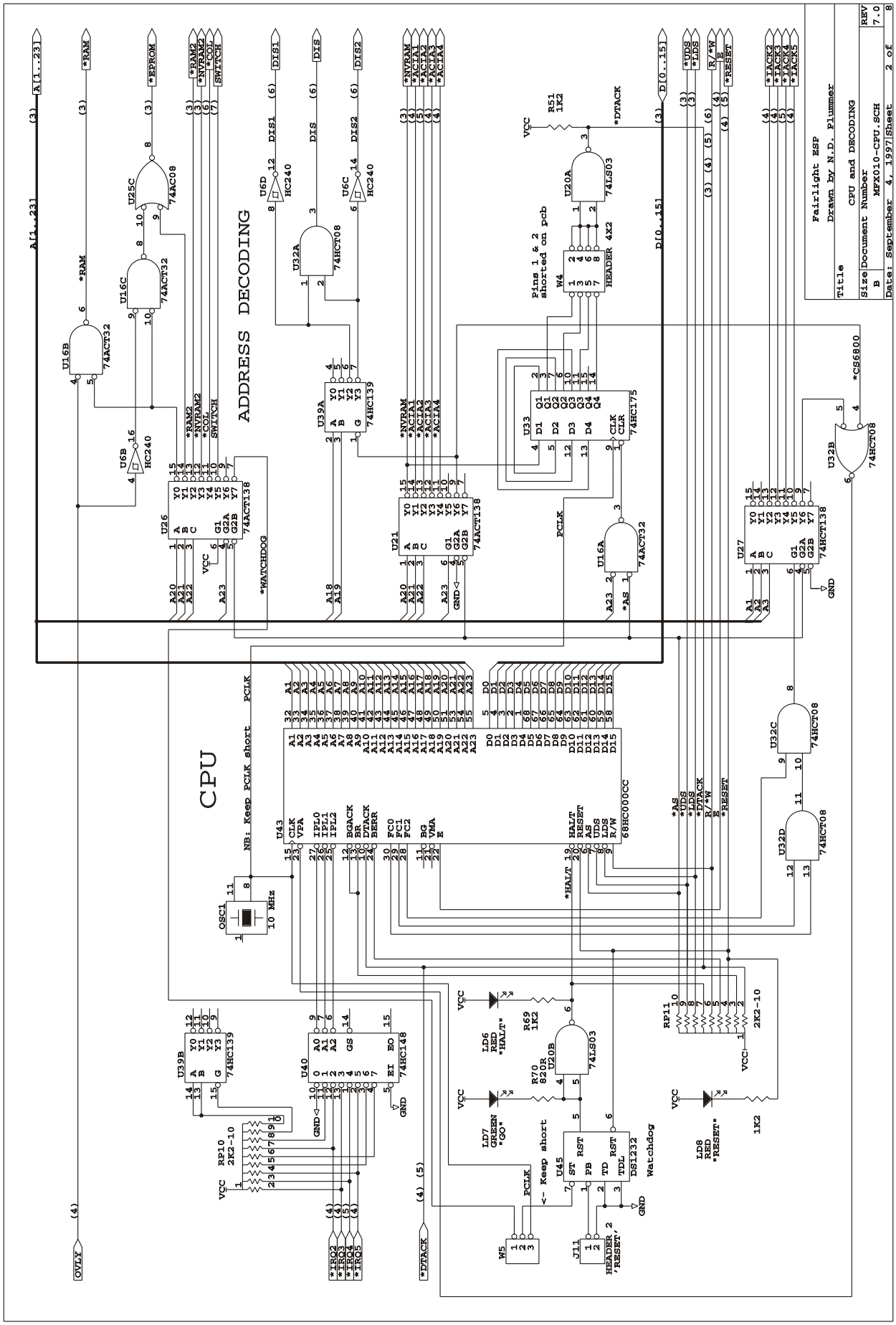
MFX Auto Connection

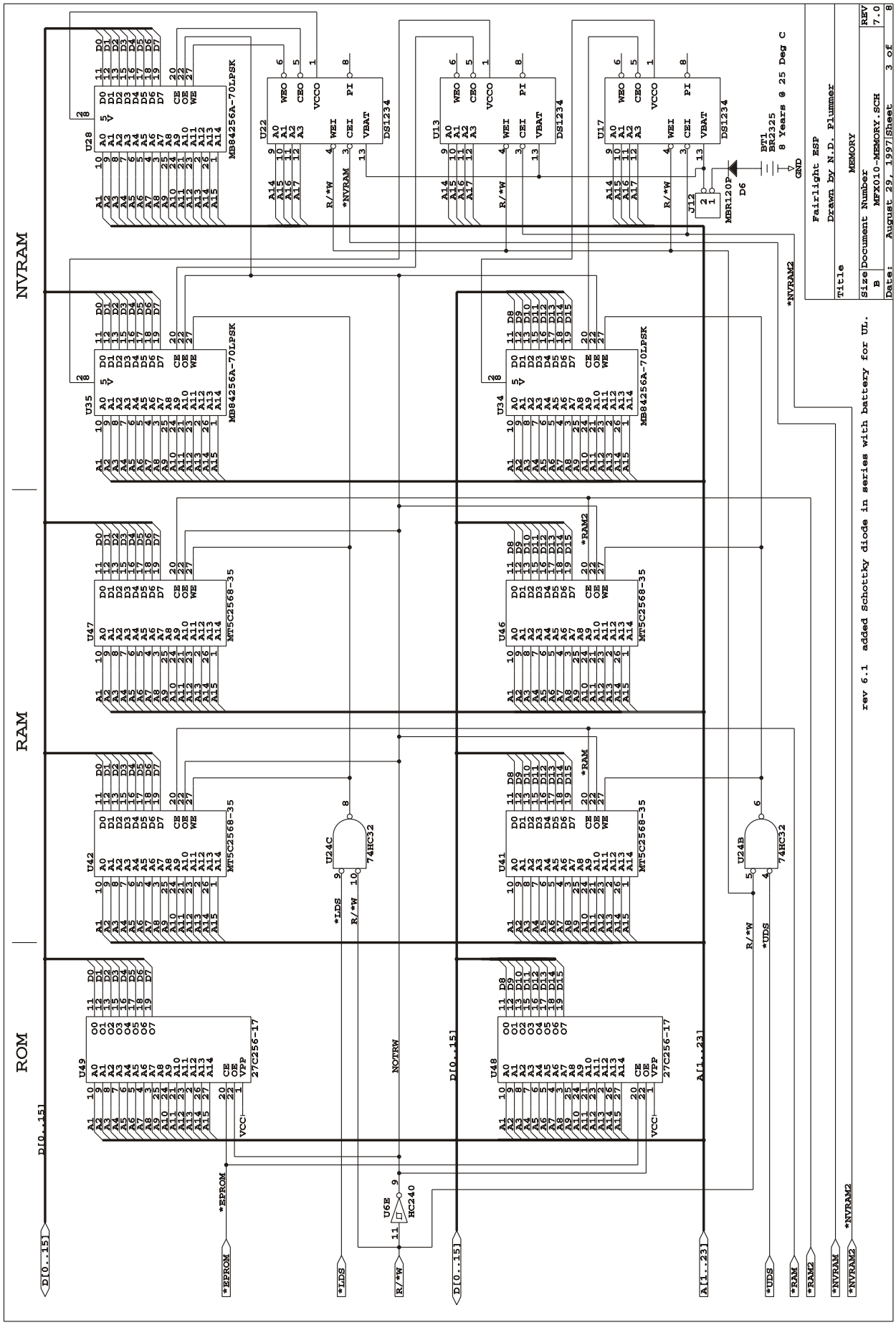
9 Pin Male
D Connector
with Metal Backshell
UL Recognised
(Connects to Serial Port on PC)

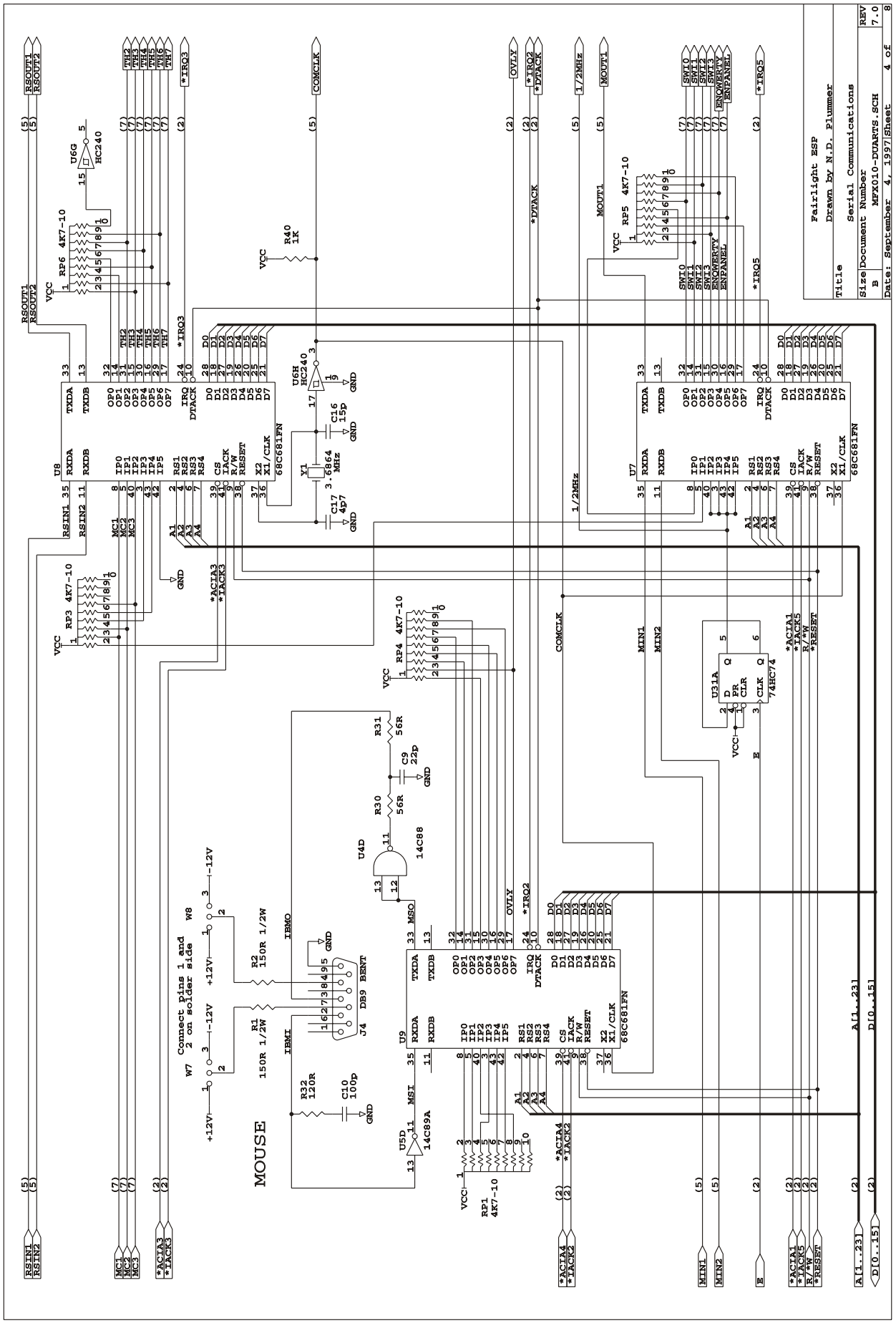
DIMENSION UNITS: mm	DESIGNED BY ENGINEERING: L.Stewart	TITLE: CABG8529 - MFXP Cable Connection Diagram	REV. 1.3
TOLERENCE: ± 3%	APPROVED BY ENGINEERING	FILE NAME: Cabg8529 MFXP 2 of 2 Connect rev 1-3.dc	
FILE NAME: CABC8529.DW2	APPROVED BY PRODUCTION	SCALE N.T.S. / SHEET 1 OF 1	COMPANY CONFIDENTIAL
	APPROVED BY QUALITY CONTROL		

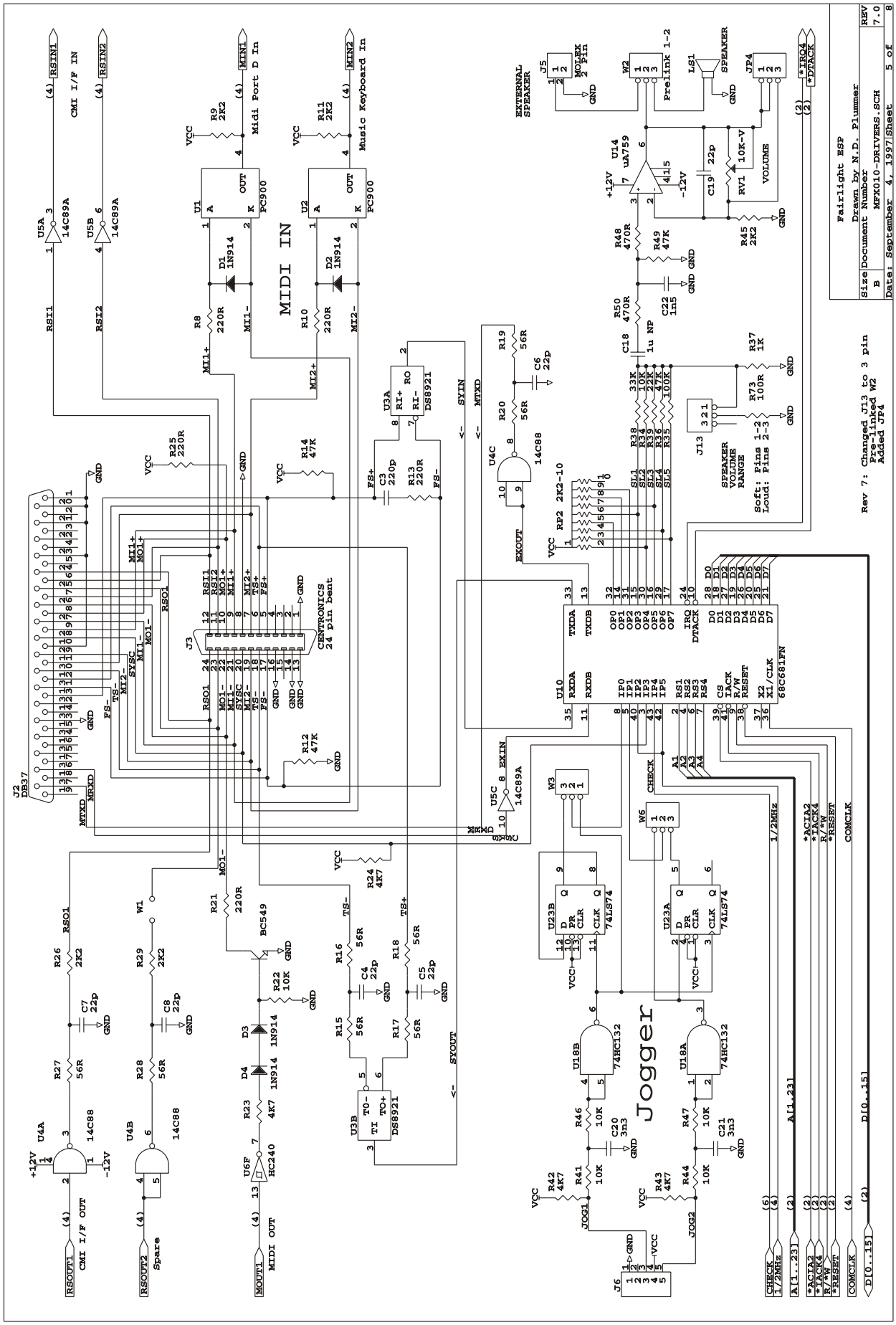
25.4 MFX010 Controller Card Schematics

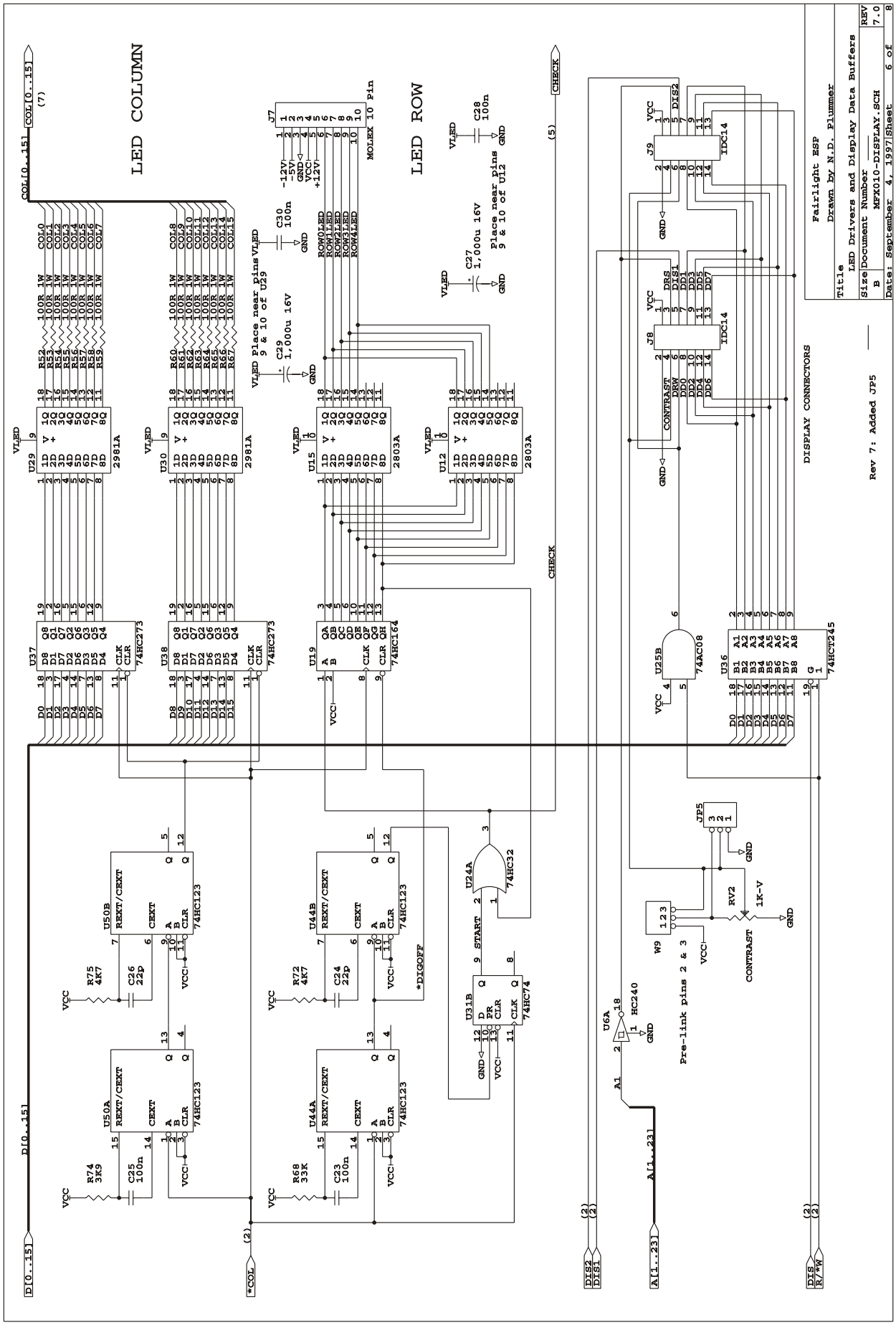


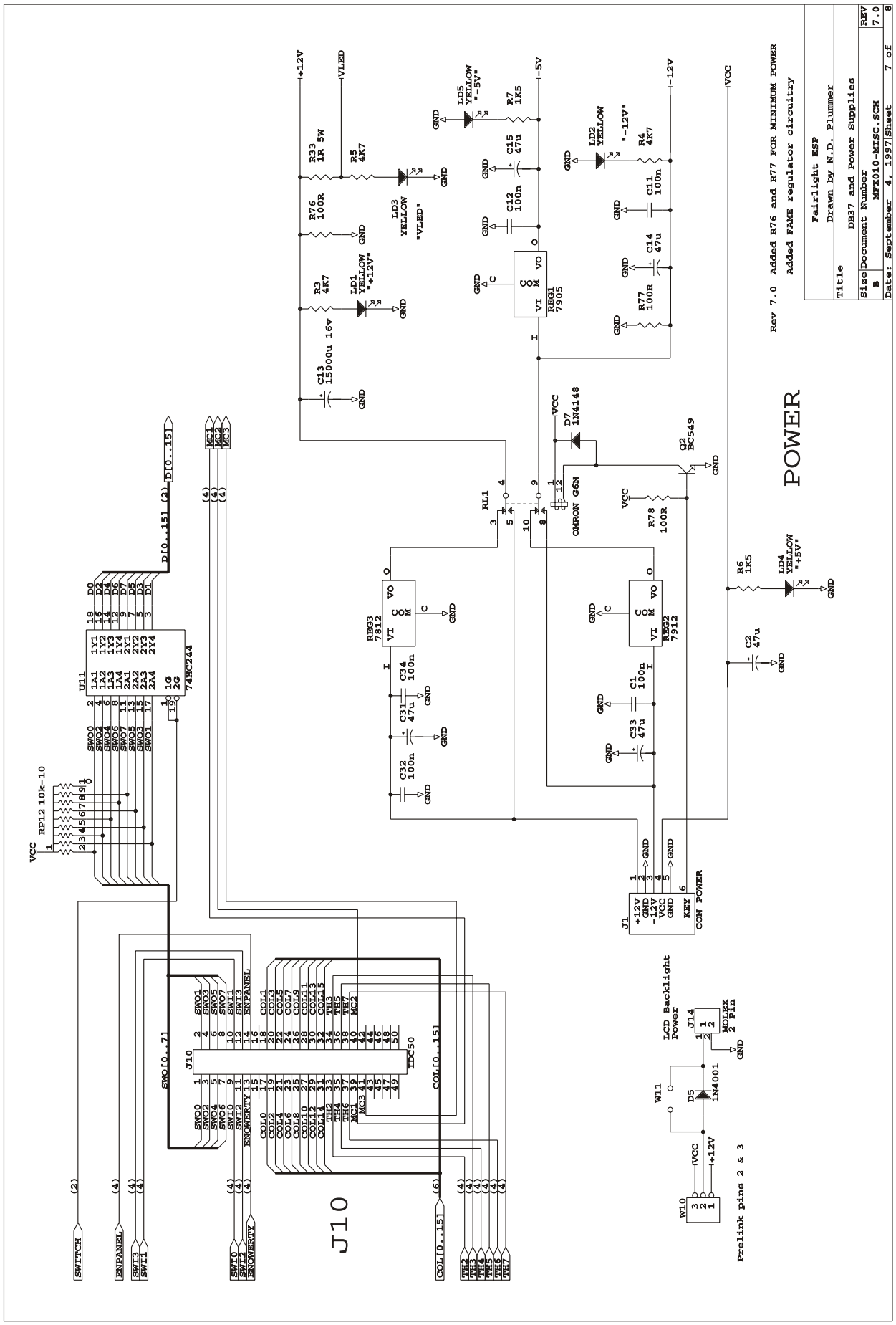

ADDRESS DECODING
CPU
Fairlight ESP
Drawn by N.D. Plummer
Title CPU and DECODING
Size B Document Number MFX010-CPU.SCH REV 7.0
Date: September 4, 1997 Sheet 2 of 8
NB: Keep PCLK short
<- Keep short
Watchdog
Pins 1 & 2 shorted on pcb
10 MHz
*RAM
*EPROM
*RAM2
*NVRAM2
*COL
SWITCH
DIS1
DIS
DIS2
*NVRAM
*ACIA1
*ACIA2
*ACIA3
*ACIA4
*WATCHDOG
*DTACK
*CS6800
*UDS
*LDS
R/*W
*RESET
*TACK2
*TACK3
*TACK4
*TACK5
*IRQ2
*IRQ3
*IRQ4
*IRQ5
*HALT
*AS
OVLY
A[1..23]
D[0..15]
LD6 RED "HALT"
LD7 GREEN "GO"
LD8 RED "RESET"
HEADER 'RESET'
RP10 2K2-10
RP11 2K2-10
R69 1K2
R70 820R
RS1 1K2
HEADER 4X2
74ACT32
74AC08
74ACT32
HC240
74HCT08
HC240
74HC139
74ACT138
74ACT138
74HC175
74ACT32
74HCT138
74HCT08
74HCT08
74HCT08
74LS03
74LS03
74HC139
74HC148
68HC000CC
DS1232

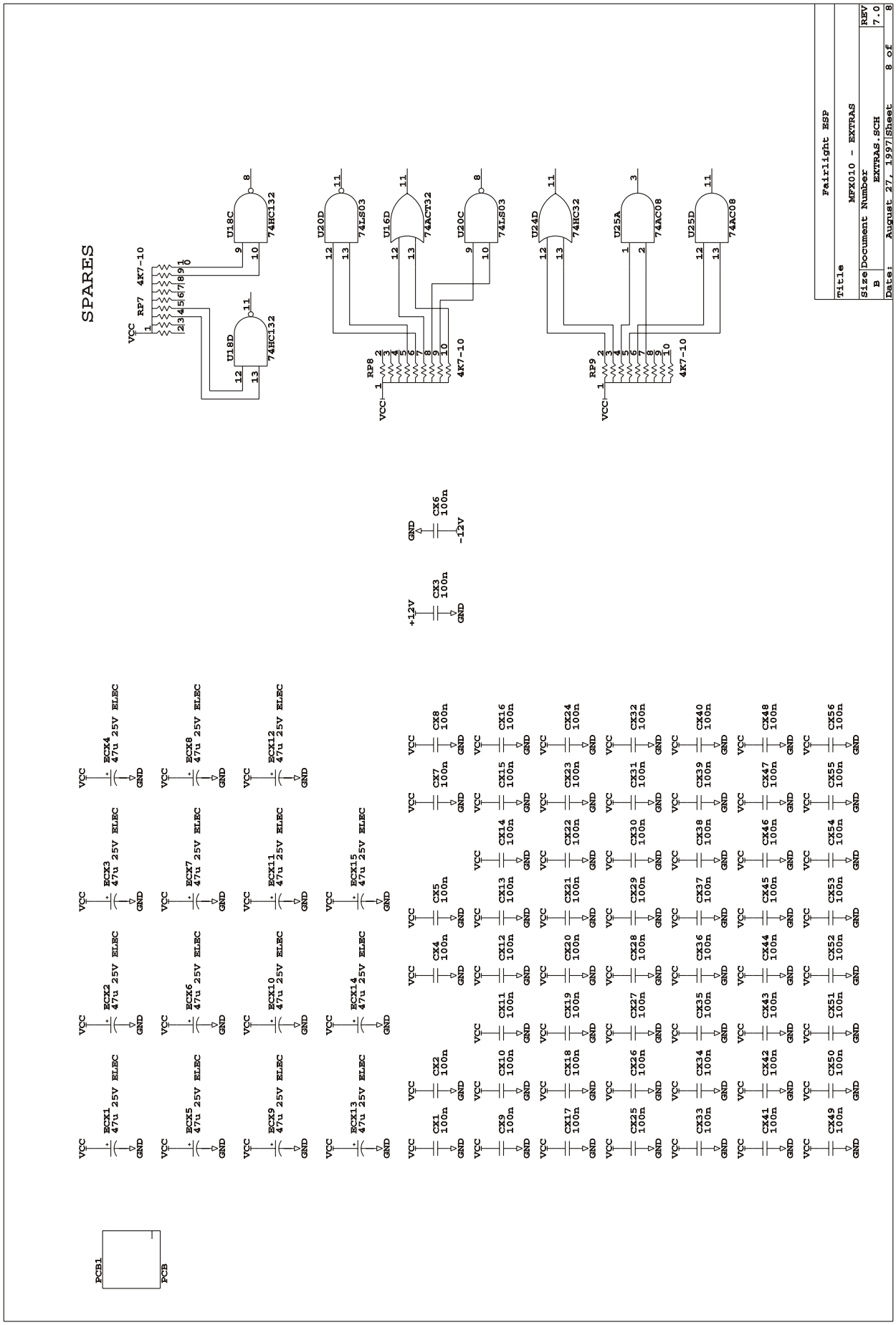

NVRAM
RAM
ROM
Fairlight ESP
Drawn by N.D. Plummer
Title
MEMORY
Size
Document Number
MFX010-MEMORY.SCH
REV
7.0
Date: August 29, 1997
Sheet 3 of 8
rev 6.1 added Schottky diode in series with battery for U1.
MB84256A-70LPSK
MT5C2568-35
27C256-17
74HC32
HC240
DS1234
MBR120P
BR2325
8 Years @ 25 Deg C
GND
D[0..15]
A[1..23]
*EPROM
*LDS
*UDS
*RAM
*RAM2
*NVRAM
*NVRAM2
R/*W
NOTRW


Fairlight ESP
Drawn by N.D. Plummer
Title Serial Communications
Size B Document Number MFX010-DUARTS.SCH REV 7.0
Date: September 4, 1997 Sheet 4 of 8
MOUSE
Connect pins 1 and 2 on solder side
U8
U9
U7
68C681FN
U4D
14C88
U5D
14C89A
U31A
74HC74
U6G
U6H
HC240
RP3 4K7-10
RP4 4K7-10
RP5 4K7-10
RP6 4K7-10
RP1 4K7-10
R1 150R 1/2W
R2 150R 1/2W
R30 56R
R31 56R
R32 120R
R40 1K
C9 22p
C10 100p
C16 15p
C17 4p7
Y1 3.6864 MHz
J4 DB9 BENT
VCC
GND
COMCLK
1/2MHz
*IRQ3
*IRQ5
*IRQ2
*DTACK
OVLY
MOUT1
SWI0
SWI1
SWI2
SWI3
ENOWERTY
ENPANEL
RSOUT1
RSOUT2
RSIN1
RSIN2
MC1
MC2
MC3
*ACIA3
*TACK3
*ACIA4
*TACK4
*ACIA1
*TACK5
R/*W
*RESET
MIN1
MIN2
E
A[1..23]
D[0..15]

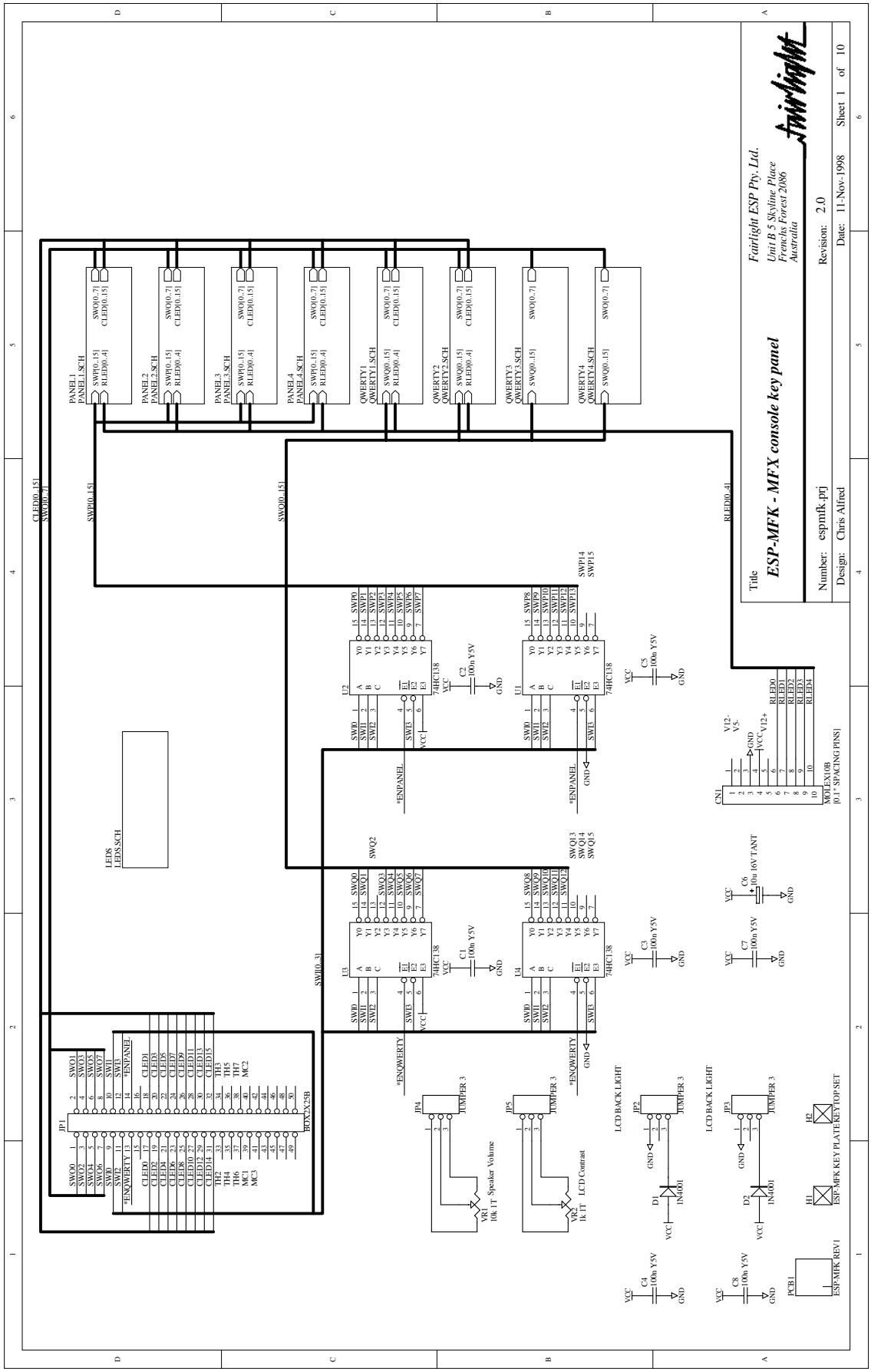

MIDI IN
Joggger
Midi Port D In
Music Keyboard In
CMI I/F IN
CMI I/F OUT
Spare
MIDI OUT
CENTRONICS
24 pin Dent
SPEAKER
VOLUME
RANGE
Soft: Pins 1-2
Loud: Pins 2-3
Prelink 1-2
SPEAKER
VOLUME
EXTERNAL
SPEAKER
Rev 7: Changed J13 to 3 pin
Pre-linked W2
Added JP4
Fairlight ESP
Drawn by N.D. Plummer
MFX010-DRIVERS.SCH
Date: September 4, 1997 Sheet 5 of 8

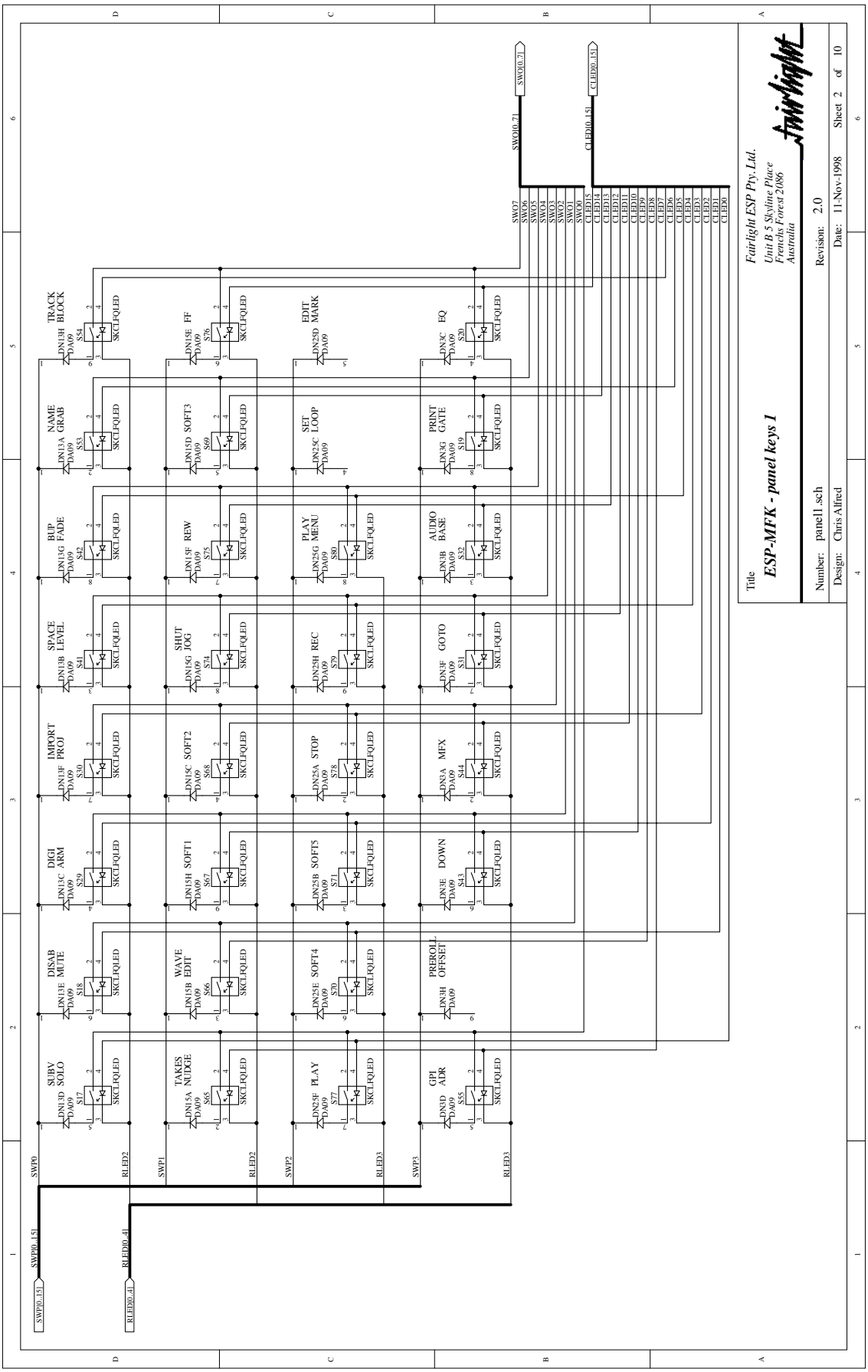

LED COLUMN
LED ROW
DISPLAY CONNECTORS
Fairlight ESP
Drawn by N.D. Plummer
Title
LED Drivers and Display Data Buffers
Size|Document Number
B
MFX010-DISPLAY.SCH
REV
7.0
Date: September 4, 1997|Sheet 6 of 8
Rev 7: Added JP5
Pre-link pins 2 & 3
CONTRAST
*DIGOFF
*COL
CHECK
D[0..15]
A[1..23]
COL[0..15]
VLED Place near pins 9 & 10 of U29
Place near pins 9 & 10 of U12
MOLEX 10 Pin
IDC14
74HC273
74HC164
74HC123
74HC32
74HC74
74HC240
74HCT245
74AC08
2981A
2803A

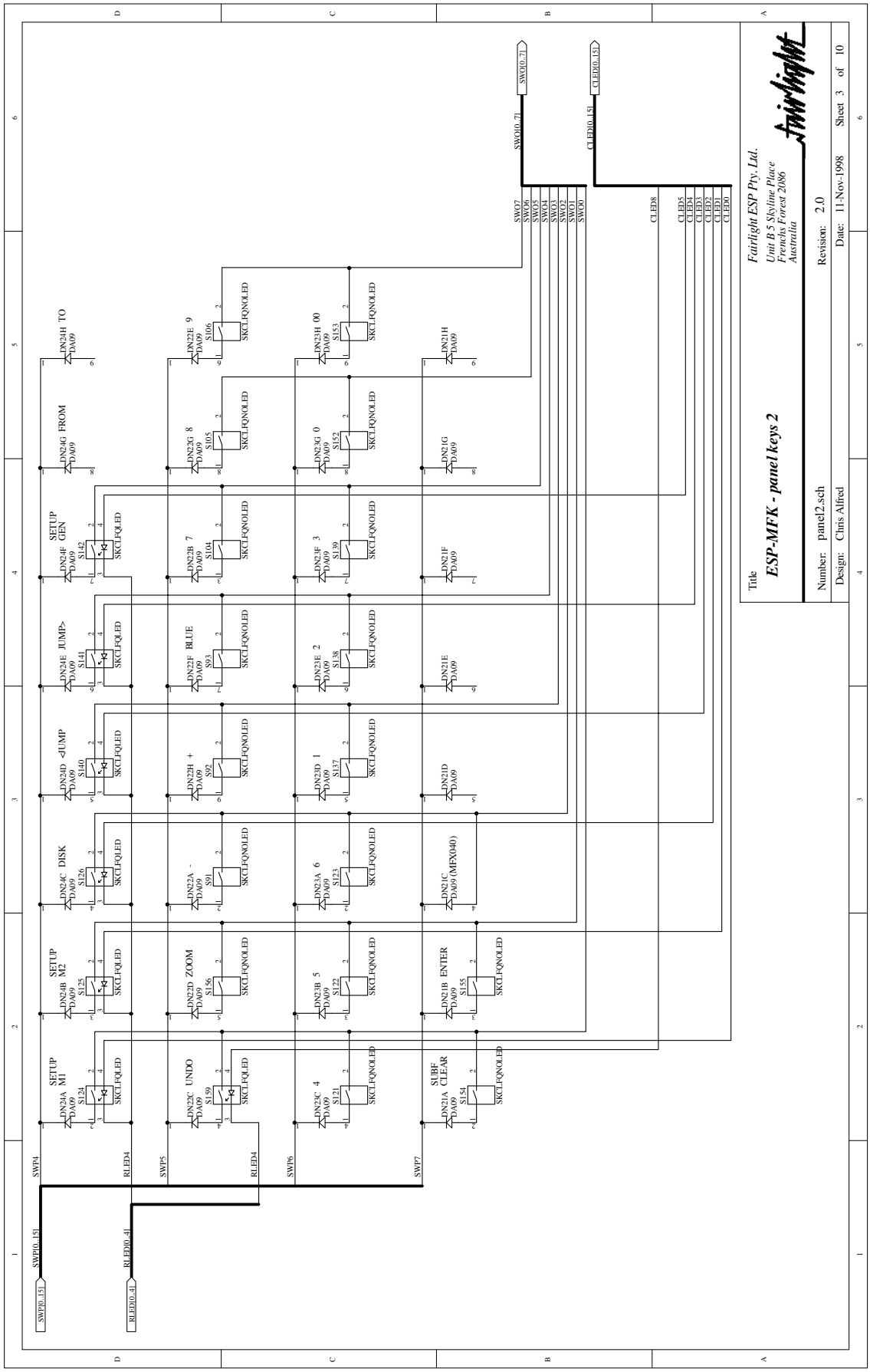

POWER
J10
Rev 7.0 Added R76 and R77 FOR MINIMUM POWER
Added FAME regulator circuitry
Fairlight ESP
Drawn by N.D. Plummer
DB37 and Power Supplies
MFX010-MISC.SCH
Date: September 4, 1997 Sheet 7 of 8
Prelink pins 2 & 3
LCD Backlight Power
+12V
-12V
-5V
VCC
VLED
GND
SWITCH
ENPANEL
ENQWERTY
SWI0..71
COL[0..15]
D[0..15]
MC1
MC2
MC3
RP12 10k-10
U11
74HC244
J1
CON POWER
REG1 7905
REG2 7912
REG3 7912
RL1
OMRON G6N
Q2 BC549
D7 1N4148
D5 1N4001
LD1 YELLOW "+12V"
LD2 YELLOW "-12V"
LD3 YELLOW "VLED"
LD4 YELLOW "+5V"
LD5 YELLOW "-5V"
R3 4K7
R4 4K7
R5 4K7
R6 1K5
R7 1K5
R33 1R 5W
R76 100R
R77 100R
R78 100R
C1 100n
C2 47u
C11 100n
C12 100n
C13 15000u 16v
C14 47u
C15 47u
C31 47u
C32 100n
C33 47u
C34 100n
W10
W11
J14
MOLEX 2 Pin

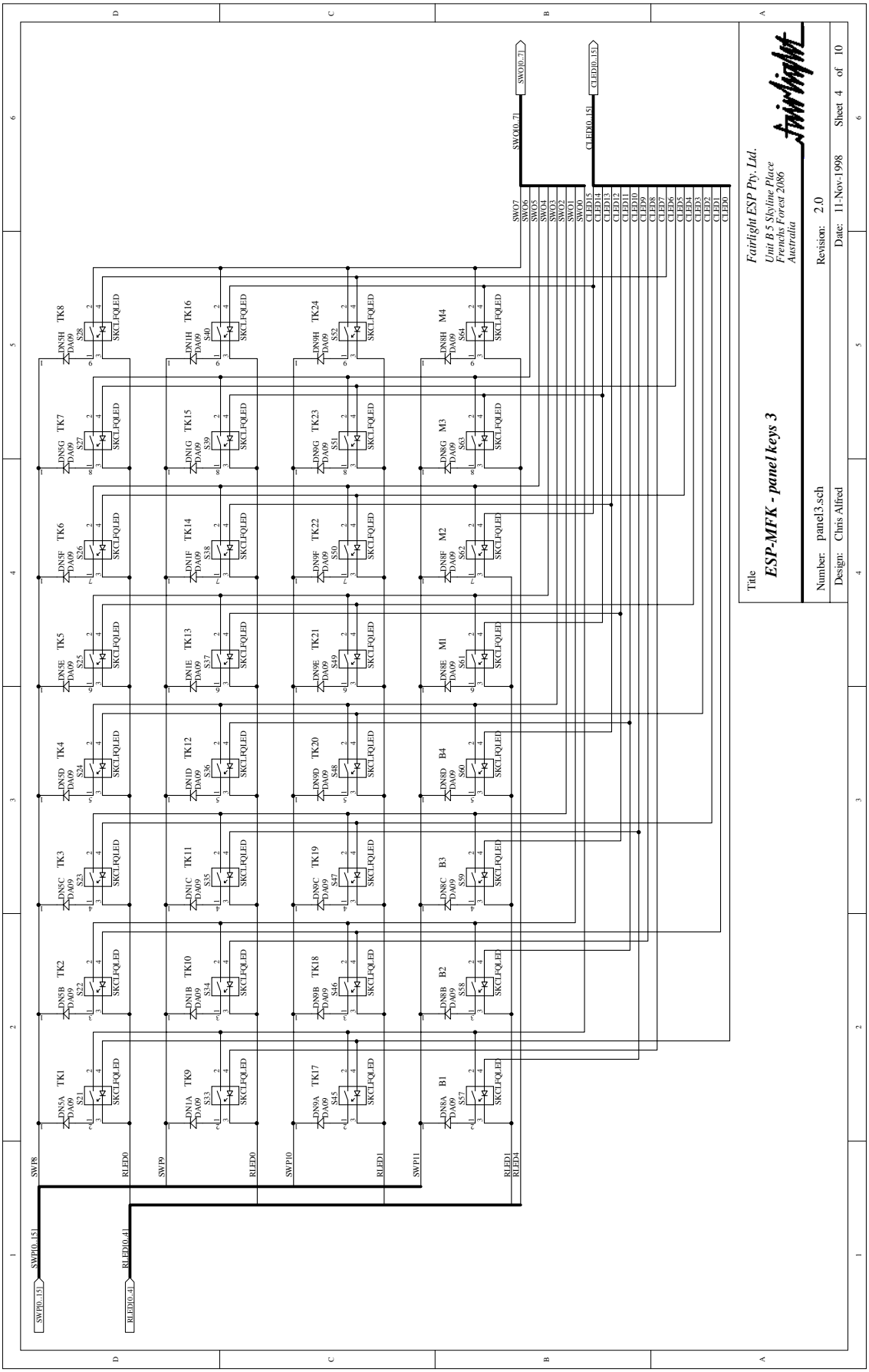

SPARES
Fairlight ESP
Title
MFX010 - EXTRAS
Size
B
Document Number
EXTRAS.SCH
REV
7.0
Date: August 27, 1997
Sheet 8 of 8

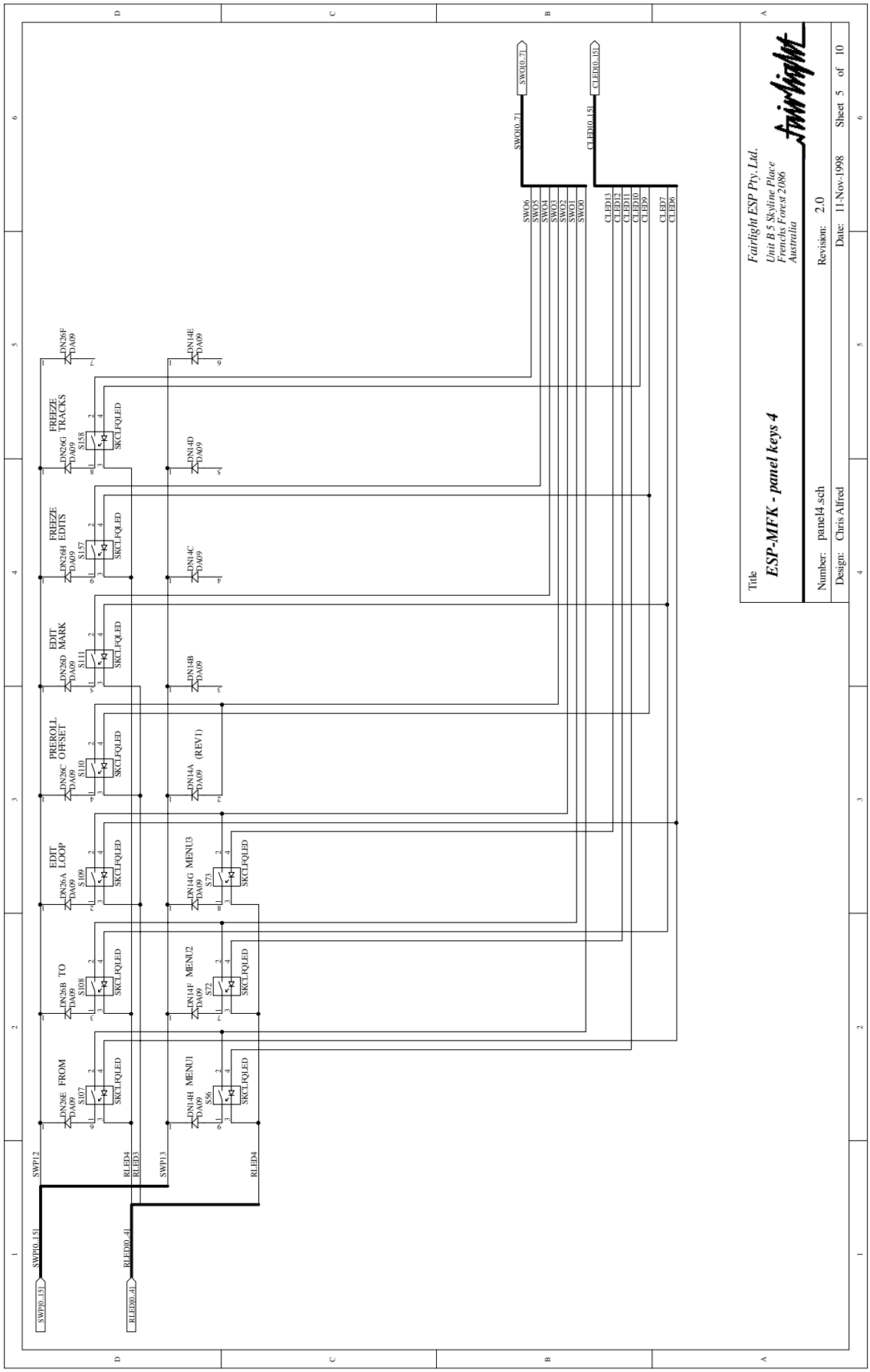
25.5 MFK SCHEMATICS

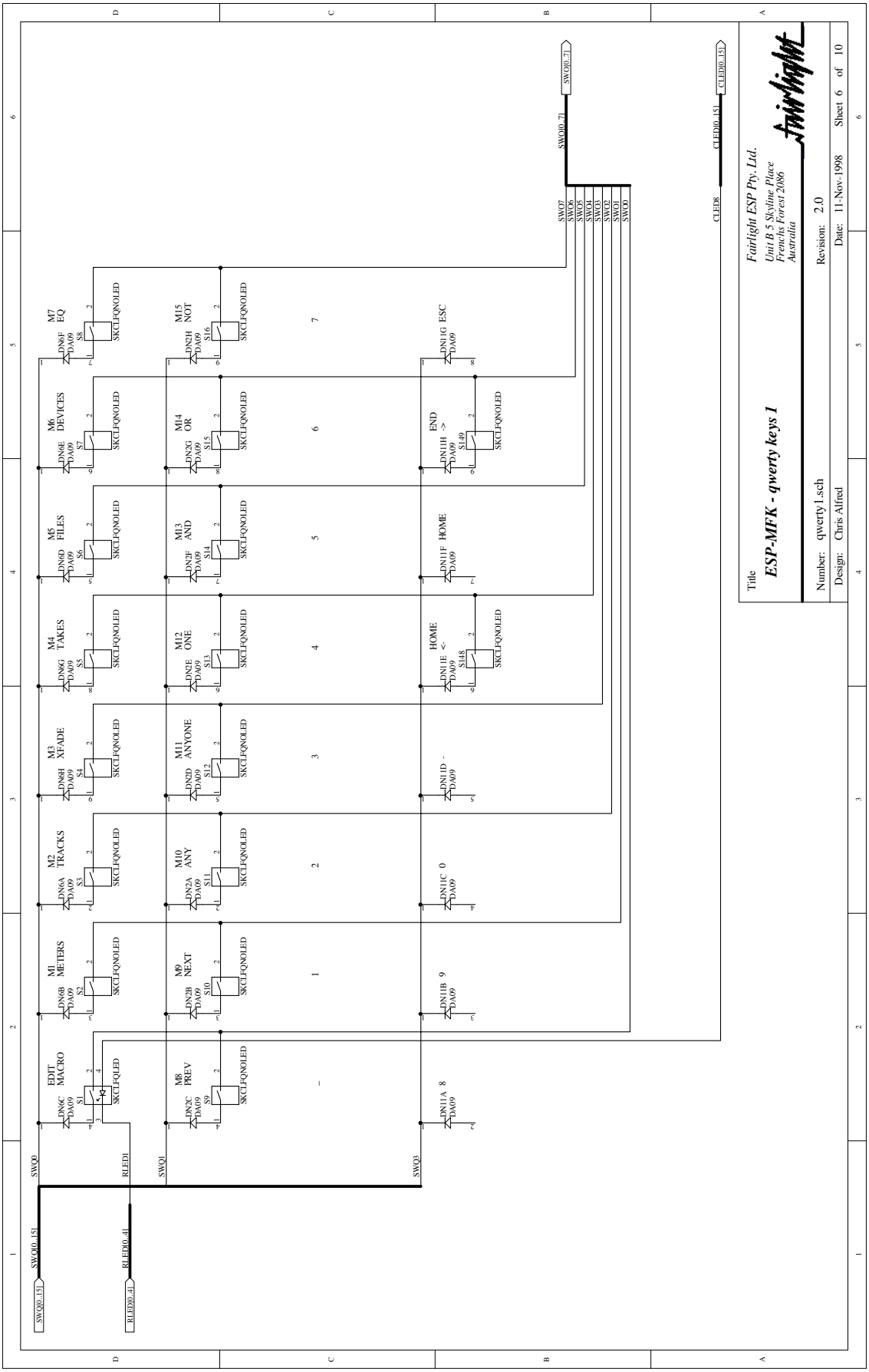


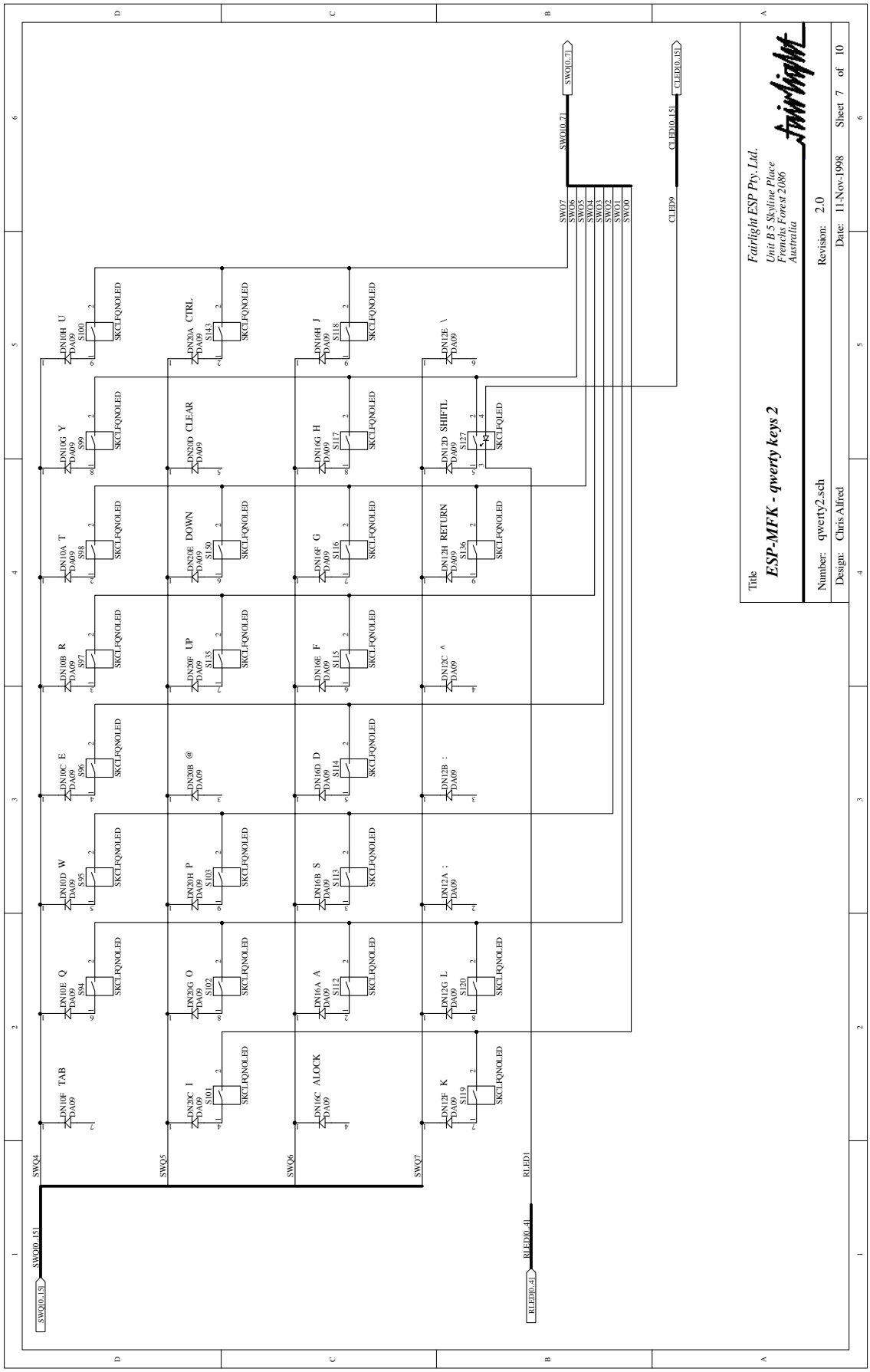

Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Title
ESP-MFK - panel keys 1
Number: panel1.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 2 of 10
SWP0.15]
RLED0.4]
SWP0
SWP1
SWP2
SWP3
RLED2
RLED3
SW0.7]
CLED0.15]
SUBV SOLO
TAKES NUDGE
GPI ADR
DISAB MUTE
WAVE EDIT
PREROLL OFFSET
DIGI ARM
IMPORT PROJ
SPACE LEVEL
BUP FADE
NAME GRAB
TRACK BLOCK
SOFT1
SOFT2
SOFT3
FF
REW
SHUT JOG
SOFT4
SOFT5
PLAY
REC
STOP
MFX
DOWN
GOTO
SET LOOP
EDIT MARK
PLAY MENU
AUDIO BASE
PRINT GATE
EQ
SKCLFQLED

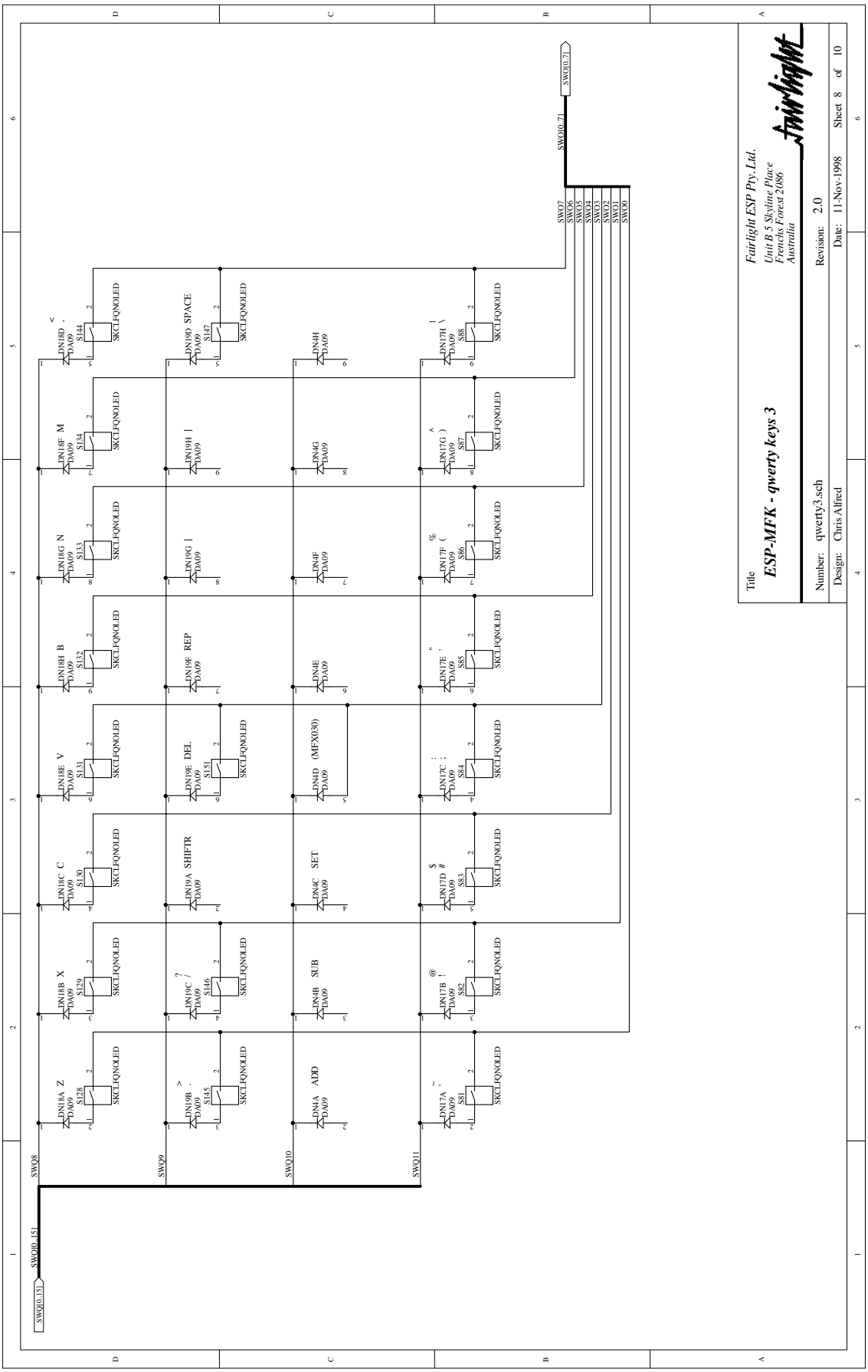

Title
ESP-MFK - panel keys 2
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Number: panel2.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 3 of 10
SWP0..15
RLED0..4
SWO0..7
CLED0..15
SETUP M1
SETUP M2
DISK
SETUP GEN
UNDO
ZOOM
-
+
6
5
4
BLUE
JUMP>
<JUMP
FROM
TO
CLEAR
ENTER
MFX040
SKCLFQLED
SKCLFQNOLED

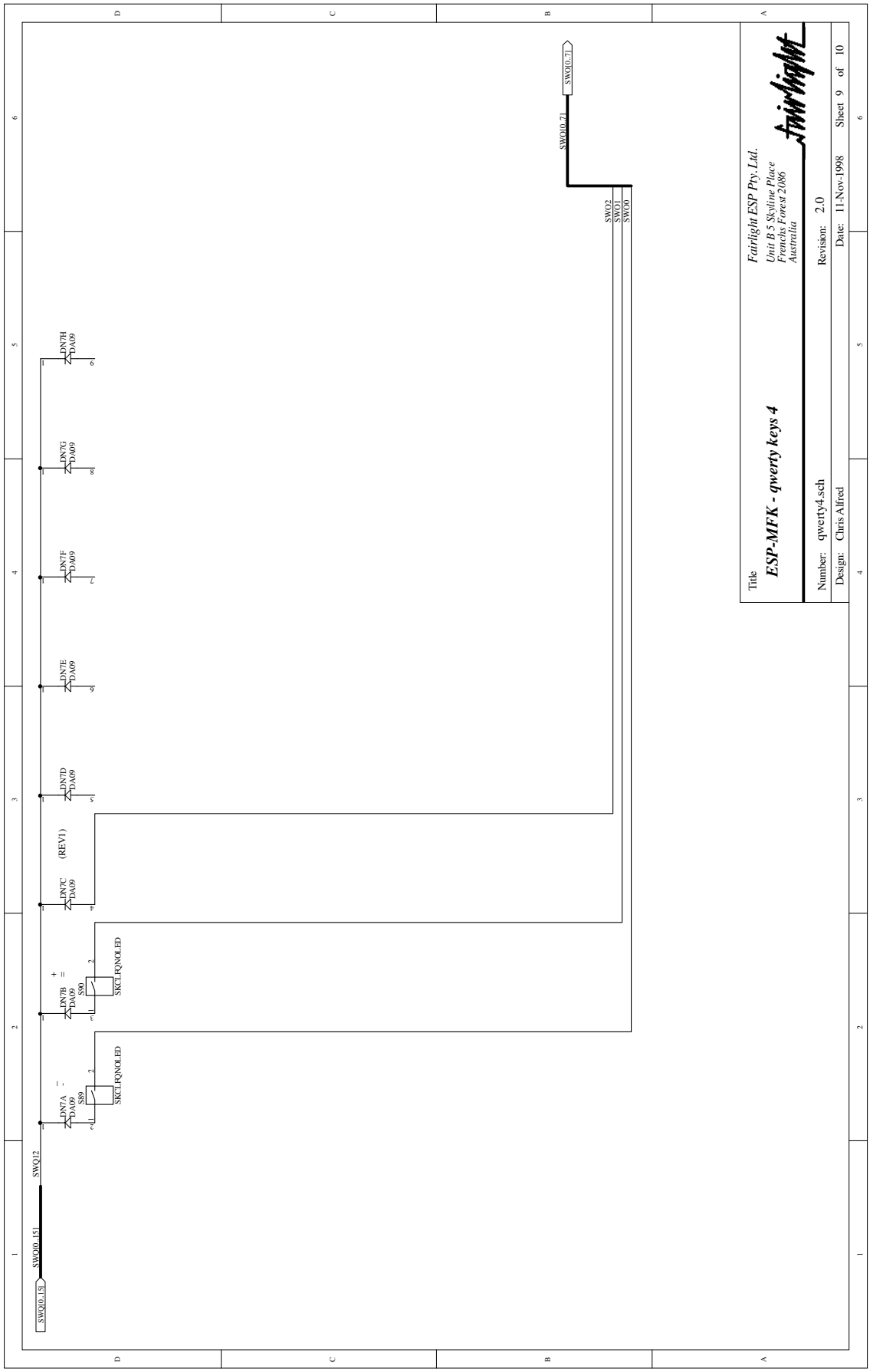

Title
ESP-MFK - panel keys 3
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Number: panel3.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 4 of 10
SWP0..15
RLED0..4
SWO0..7
CLED0..15

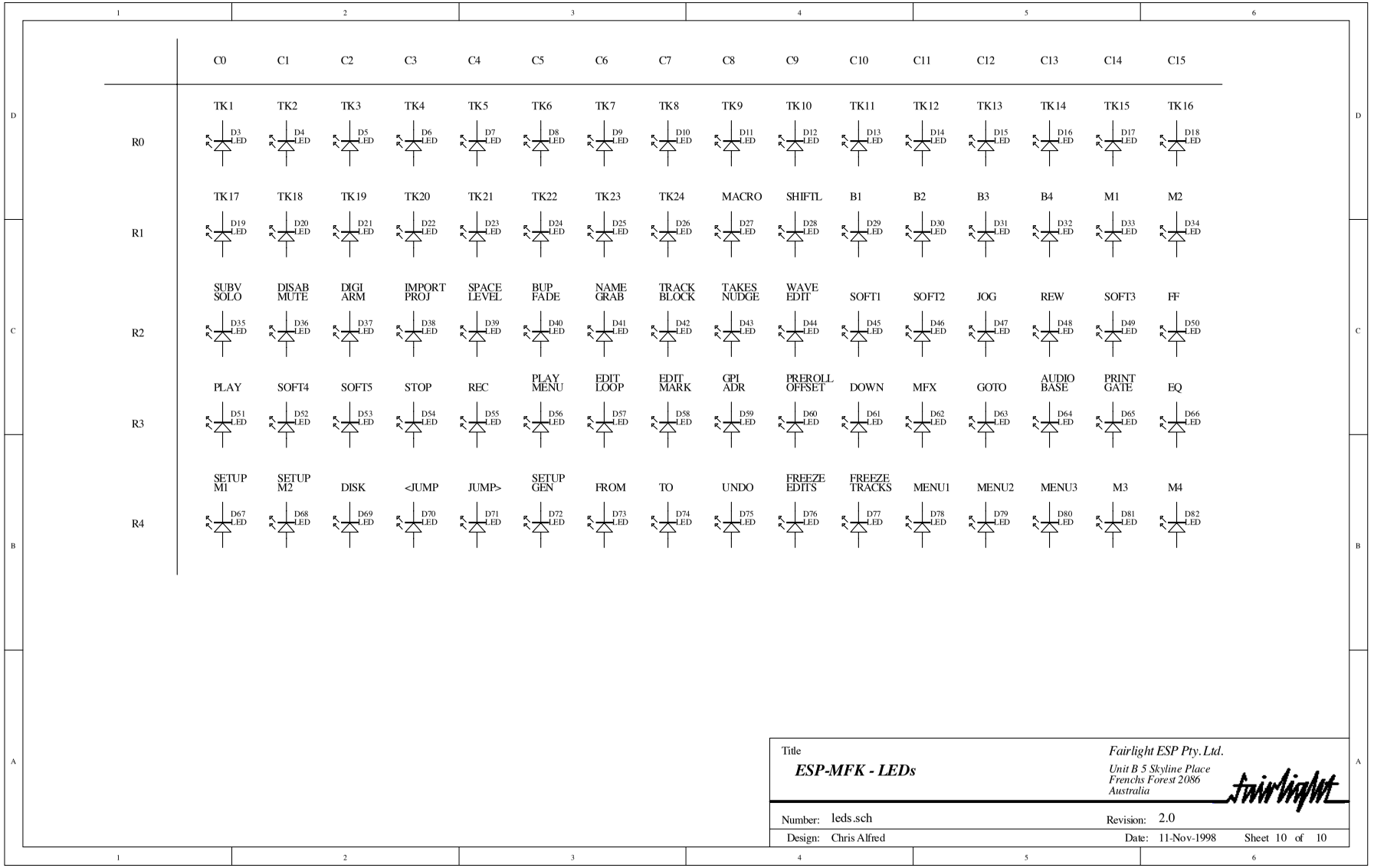

Title
ESP-MFK - panel keys 4
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
French's Forest 2086
Australia
Number: panel4.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 5 of 10
SWP[0..15]
RLED[0..4]
SW0[0..7]
CLED[0..15]
SWP12
SWP13
RLED4
RLED3
SW06
SW05
SW04
SW03
SW02
SW01
SW00
CLED13
CLED12
CLED11
CLED10
CLED9
CLED7
CLED6
FROM
TO
MENU2
MENU1
EDIT LOOP
PREROLL OFFSET
EDIT MARK
FREEZE EDITS
FREEZE TRACKS
MENU3
(REV1)
SKCLFQLED


Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Title
ESP-MFK - qwerty keys 1
Number: qwerty1.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 6 of 10
SWQ0..15
RLED0..41
CLED0..15
SWQ0
SWQ1
SWQ3
RLED1
M1 METERS
M2 TRACKS
M3 XFADE
M4 TAKES
M5 FILES
M6 DEVICES
M7 EQ
M8 PREV
M9 NEXT
M10 ANY
M11 ANYONE
M12 ONE
M13 AND
M14 OR
M15 NOT
EDIT MACRO
HOME <-
END ->
ESC
HOME
SKCLFQNOLED
SKCLFQLED


Title
ESP-MFK - qwerty keys 2
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
French's Forest 2086
Australia
Number: qwerty2.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 7 of 10
SWQ[0..15]
SWO[0..15]
RLED[0..4]
CLED[0..15]
SWQ4
SWQ5
SWQ6
SWQ7
RLED1
CLED9
SKCLFQNOLED
SKCLFQLED


SWQ0.15]
SWQ0 15]
SWQ8
SWQ9
SWQ10
SWQ11
SWQ0.7]
SWQ0 7]
SW07
SW06
SW05
SW04
SW03
SW02
SW01
SW00
DN18A Z
DN19B .
DN4A ADD
DN17A ~
DN18B X
DN19C /
DN4B SUB
DN17B @
DN18C C
DN19A SHIFTR
DN4C SET
DN17D $
DN18E V
DN19E DEL
DN4D (MFX030)
DN17C : ;
DN18H B
DN19F REP
DN4E
DN17E " '
DN18G N
DN19G [
DN4F
DN17F % (
DN18F M
DN19H]
DN4G
DN17G ^)
DN18D < ,
DN19D SPACE
DN4H
DN17H | \
SKCLFQNOLED
Title
ESP-MFK - qwerty keys 3
Number: qwerty3.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 8 of 10
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia


SWQ[0..15]
SWQ0..15
SWQ12
SW0[0..7]
SW0[0..7]
SW02
SW01
SW00
DN7A DA09
DN7B DA09
DN7C DA09
DN7D DA09
DN7E DA09
DN7F DA09
DN7G DA09
DN7H DA09
S89
S90
SKCLFQNOLED
SKCLFQNOLED
(REV1)
Title
ESP-MFK - qwerty keys 4
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
French's Forest 2086
Australia
Number: qwerty4.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 9 of 10


C0 C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15
R0
TK1 TK2 TK3 TK4 TK5 TK6 TK7 TK8 TK9 TK10 TK11 TK12 TK13 TK14 TK15 TK16
D3 LED D4 LED D5 LED D6 LED D7 LED D8 LED D9 LED D10 LED D11 LED D12 LED D13 LED D14 LED D15 LED D16 LED D17 LED D18 LED
R1
TK17 TK18 TK19 TK20 TK21 TK22 TK23 TK24 MACRO SHIFTL B1 B2 B3 B4 M1 M2
D19 LED D20 LED D21 LED D22 LED D23 LED D24 LED D25 LED D26 LED D27 LED D28 LED D29 LED D30 LED D31 LED D32 LED D33 LED D34 LED
R2
SUBV SOLO DISAB MUTE DIGI ARM IMPORT PROJ SPACE LEVEL BUP FADE NAME GRAB TRACK BLOCK TAKES NUDGE WAVE EDIT SOFT1 SOFT2 JOG REW SOFT3 FF
D35 LED D36 LED D37 LED D38 LED D39 LED D40 LED D41 LED D42 LED D43 LED D44 LED D45 LED D46 LED D47 LED D48 LED D49 LED D50 LED
R3
PLAY SOFT4 SOFT5 STOP REC PLAY MENU EDIT LOOP EDIT MARK GPI ADR PREROLL OFFSET DOWN MFX GOTO AUDIO BASE PRINT GATE EQ
D51 LED D52 LED D53 LED D54 LED D55 LED D56 LED D57 LED D58 LED D59 LED D60 LED D61 LED D62 LED D63 LED D64 LED D65 LED D66 LED
R4
SETUP M1 SETUP M2 DISK <JUMP JUMP> SETUP GEN FROM TO UNDO FREEZE EDITS FREEZE TRACKS MENU1 MENU2 MENU3 M3 M4
D67 LED D68 LED D69 LED D70 LED D71 LED D72 LED D73 LED D74 LED D75 LED D76 LED D77 LED D78 LED D79 LED D80 LED D81 LED D82 LED
Title
ESP-MFK - LEDs
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Number: leds.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 10 of 10