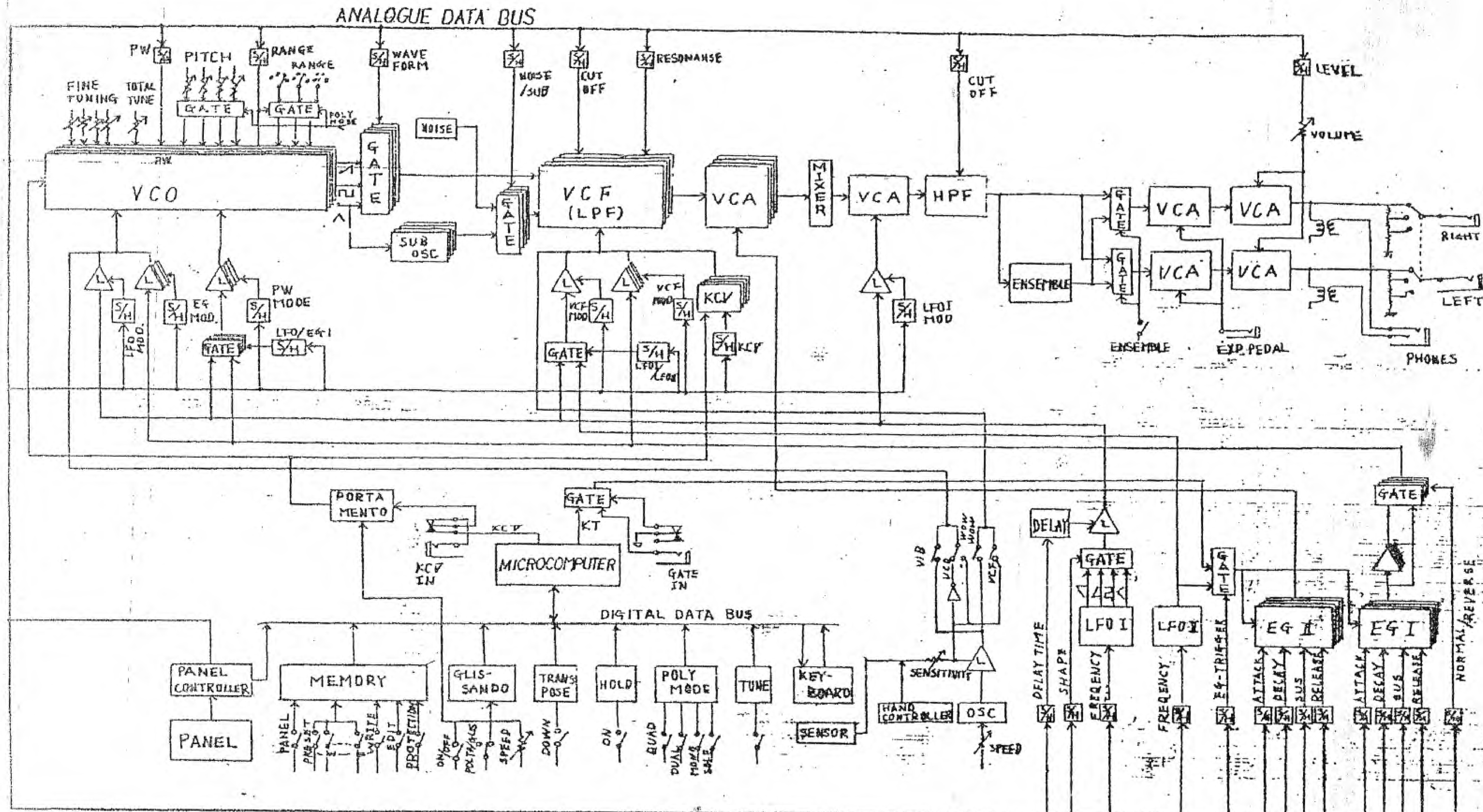


SX-400 BLOCK DIAGRAM

設計	製図	検図	承認	三角法			1			
	81.3.30			m/m	材質	仕上寸法	No.	部品名	数	摘要
	UCHIYAMA		川井	尺度	指質	SX-400	名称		図番	AGA-0113
									仮番	

テスコ株式会社

Quad 2-Input NOR Gate

CD4001UB

4-Bit Full Adder with Parallel Carry Out

CD4008B

Dual "D" Flip-Flop with Set/Reset Capability

CD4013B

Quad AND/OR Select Gate

CD4019B

$V_{DD} = 16$
$V_{SS} = 8$

8-Stage Static Shift Register Asynchronous Parallel or Synchronous Serial Input/ Serial Output

CD4021B

TRUTH TABLE

$V_{DD} = 14$
$V_{SS} = 7$

7-Stage Ripple-Carry Binary Counter/Divider

CD4024B

Dual J-K Master-Slave Flip-Flop with Set-Reset Capability

CD4027B

BCD-to-Decimal Decoder

CD4028B

$V_{DD} = 16$
$V_{SS} = 8$

TABLE I – TRUTH TABLE

D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

1 = HIGH LEVEL 0 = LOW LEVEL

Quad 3-State NAND R/S Latch

CD4044B

Hex Buffer/Converter Inverting Type

CD4049UB

Hex Buffer/Converter Non-Inverting Type

CD4050B

Single 8-Channel Analog Multiplexer/Demultiplexer

CD4051B

INPUT STATES				"ON" CHANNEL
INHIBIT	C	B	A	
CD4051B				
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	NONE

X = Don't care

Truth table

Dual 4-Channel Analog Multiplexer/Demultiplexer

CD4052B

INPUT STATES		"ON" CHANNELS
CD4052B		
INHIBIT	B	A	
0	0	0	0x, 0y
0	0	1	1x, 1y
0	1	0	2x, 2y
0	1	1	3x, 3y
1	X	X	NONE

X = Don't care Truth table

Triple 2-Channel Multiplexer/Demultiplexer

CD4053B

INPUT STATES		"ON" CHANNELS
CD4053B		
INHIBIT	A or B or C	
0	0	ax or bx or cx
0	1	ay or by or cy
1	X	NONE

X = Don't care

Truth table

Quad Bilateral Switch

CD4066B

Quad Exclusive-OR Gate

CD4070B

Quad 2-Input OR Gate

CD4071B

Dual 4-Input OR Gate

CD4072B

Quad 2-Input AND Gate

CD4081B

TRUTH TABLE

MODE	INPUTS		OUTPUTS
	A, B, C, D	ENABLE A, B, C, D	E, F, G, H
Low-to-high level shift	0	1	0
	1	1	1
	X	0	Z

LOGIC 0 = LOW V_{SS} X = DON'T CARE Z = HIGH IMPEDANCE
LOGIC 1 = V_{CC} in INPUTS and V_{DD} in OUTPUTS

Quad Low-to-High Voltage Level Shifter

CD4010B

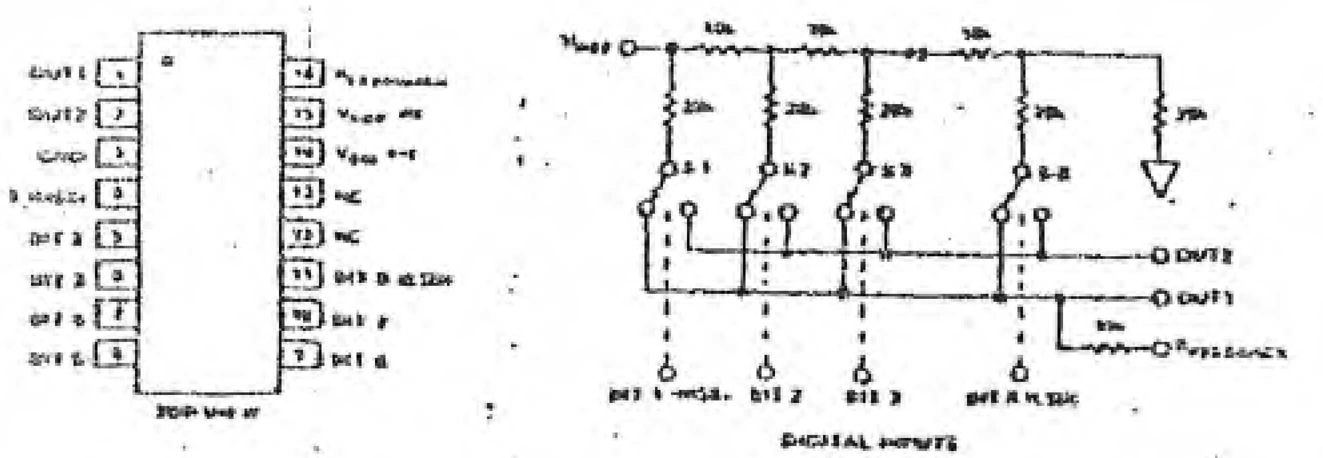
Dual D-Type Flip-Flop

CD4013B

SX-400
IC INFORMATION No 1
CMOS
1/5

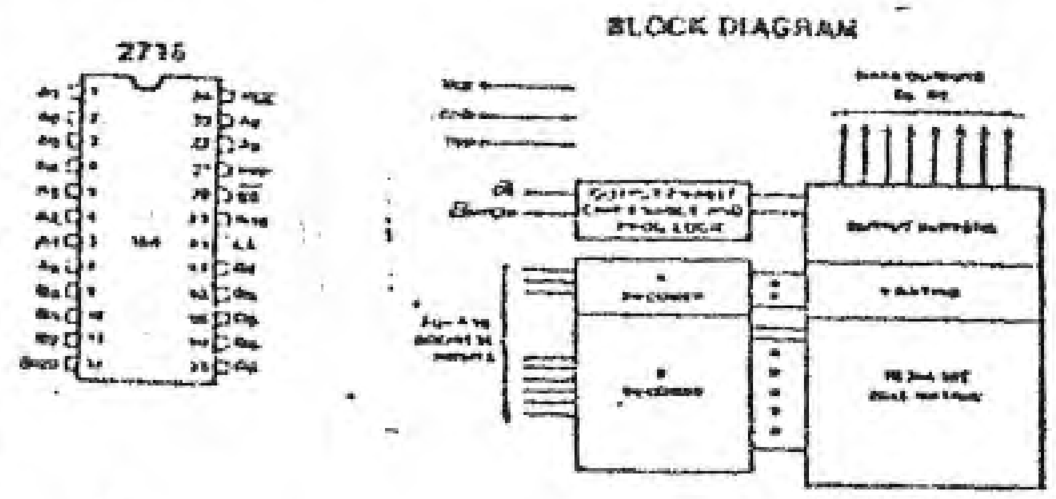
SX-400

AGA-0121



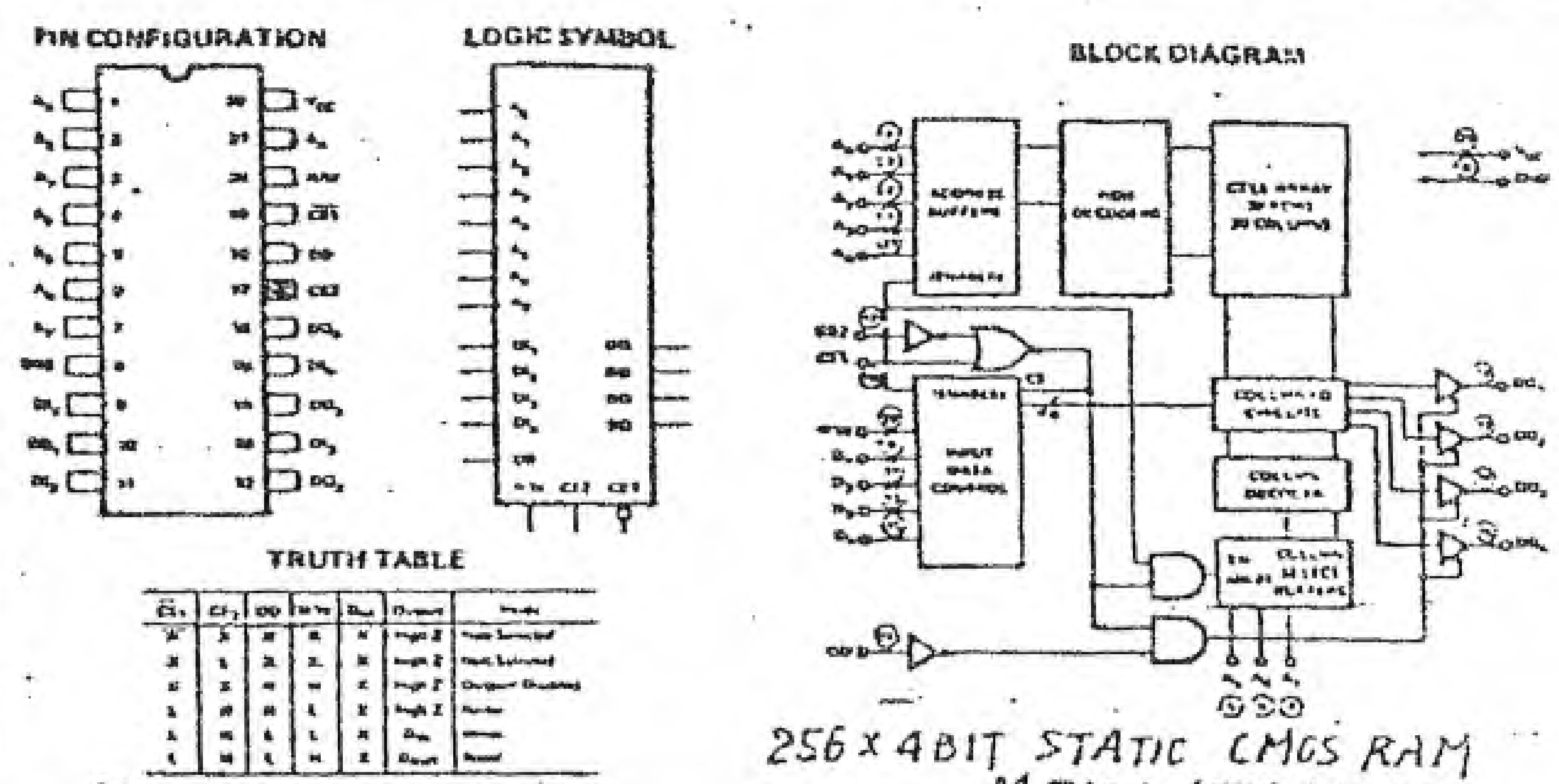
CMOS 8-BIT MULTIPLYING D/A CONVERTER

7523

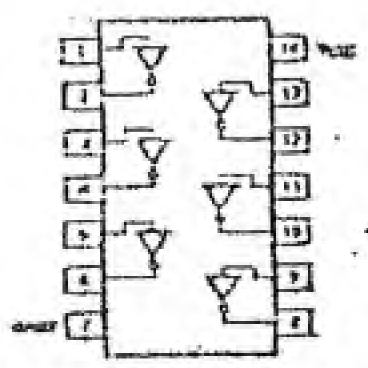


16K (2K BIT) UV ERASABLE PROM

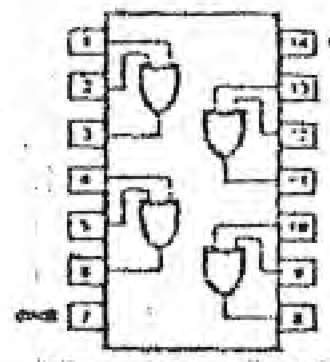
2716



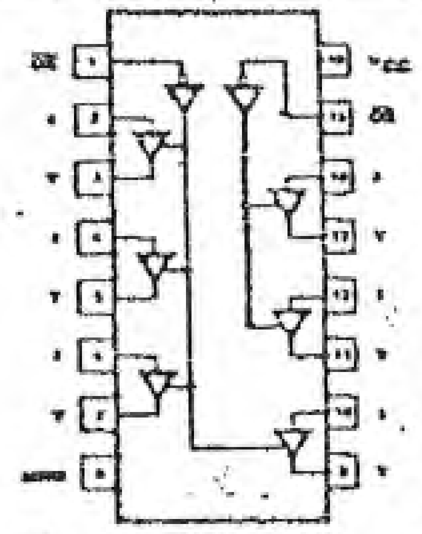
256 x 4 BIT STATIC CMOS RAM
M5101 (TC5501)



HEX INVERTER
SN 7404N



QUAD 2 INPUT OR GATE
SN 74 LS32N



TRUTH TABLE

INPUTS		OUTPUTS
$\overline{OE}$	I	Y
L	L	L
L	H	H
H	X	(Z)

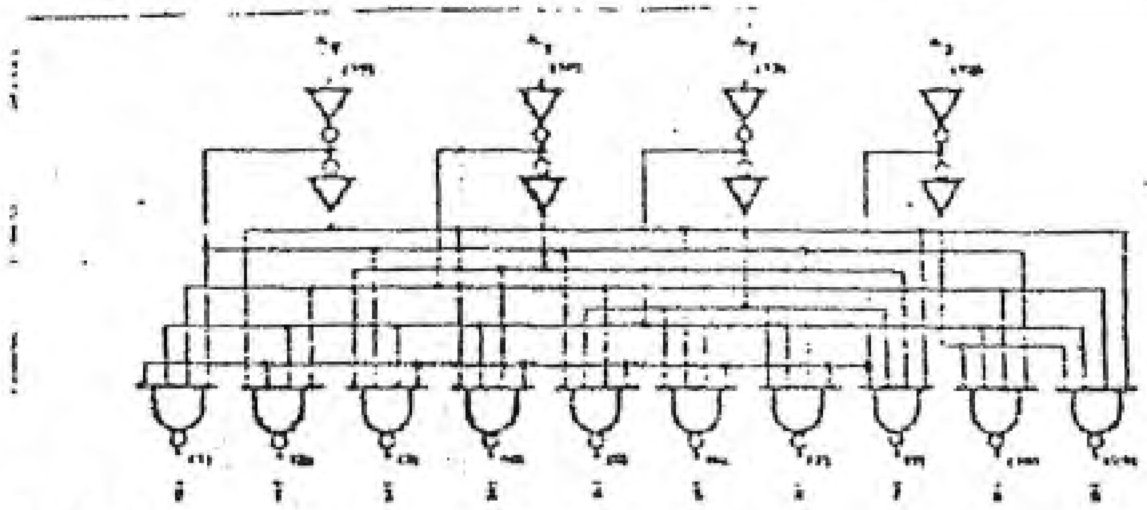
L = LOW voltage level
H = HIGH voltage level
X = Don't care
(Z) = High impedance (off) state

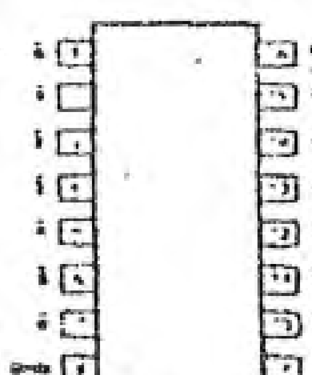
HEX BUFFER/DRIVER (3-STATE)
SN 74 LS367N

TRUTH TABLE

A_3	A_2	A_1	A_0	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

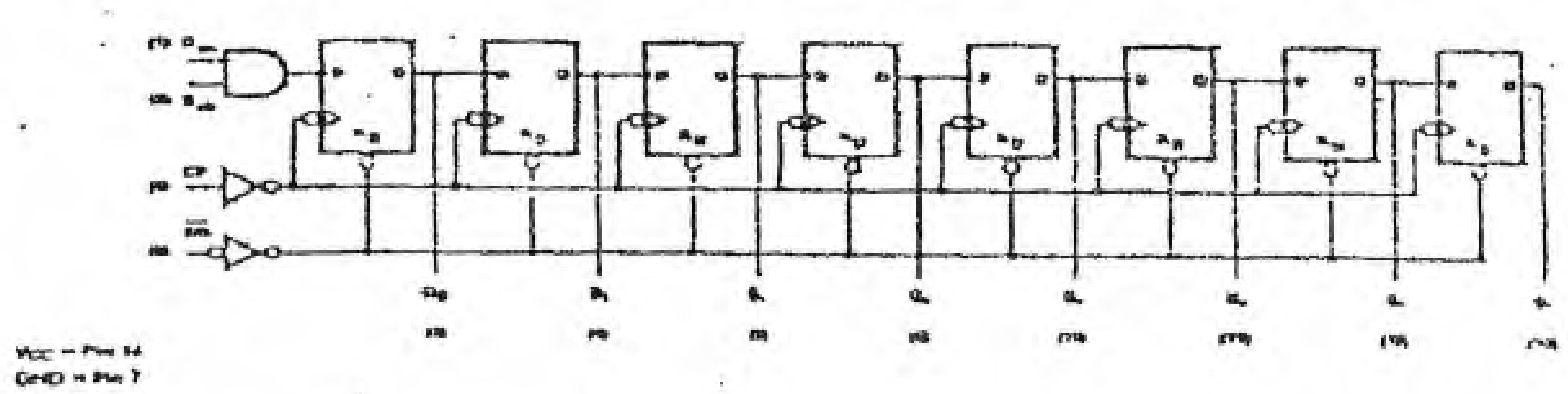
H = HIGH voltage levels
L = LOW voltage levels





BCD-TO-DECIMAL DECODER (1of-10)

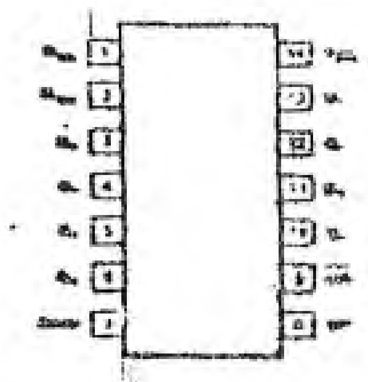
SN 74LS42N



MODE SELECT—TRUTH TABLE

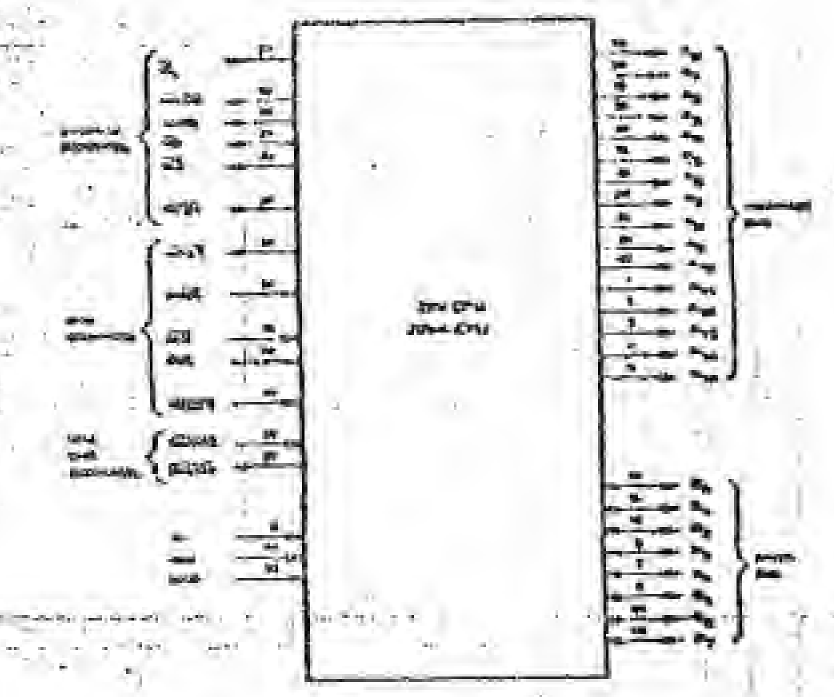
OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{MR}$	CP	D_{sa}	D_{sb}	Q_0	Q_1 – Q_7
Reset (Clear)	L	X	X	X	L	L – L
Shift	H	↑	l	l	L	q_0 – q_6
	H	↑	l	h	L	q_0 – q_6
	H	↑	h	l	L	q_0 – q_6
	H	↑	h	h	H	q_0 – q_6

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
q = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care
↑ = LOW-to-HIGH clock transition



8BIT SERIAL-IN
PARALEL-OUT SHIFT REGISTER
SN 74-LS164N

△	SX-400 IC INFORMATION (DIGITAL)	設計	製図	検図		三角法		1
△		81.1.31				m/m	材質	仕上寸法
△						尺度	品名 SX-400	部品名 IC INFORMATION (DIGITAL) 3/5
△								図番 AGA 0121



Z80, Z80A CPU PIN CONFIGURATION

A_0-A_{15} (Address Bus) Tri-state output, active high. A_0-A_{15} constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges and for I/O device data exchanges.

D_0-D_7 (Data Bus) Tri-state input/output, active high. D_0-D_7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.

$\overline{M_1}$ (Machine Cycle one) Output, active low. $\overline{M_1}$ indicates that the current machine cycle is the OP code fetch cycle of an instruction execution.

$\overline{MREQ}$ (Memory Request) Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.

$\overline{IORQ}$ (Input/Output Request) Tri-state output, active low. The $\overline{IORQ}$ signal indicates that the lower half of the address bus holds a valid I/O address for a I/O read or write operation. An $\overline{IORQ}$ signal is also generated when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus.

$\overline{RD}$ (Memory Read) Tri-state output, active low. $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

$\overline{WR}$ (Memory Write) Tri-state output, active low. $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.

$\overline{RFSH}$ (Refresh) Output, active low. $\overline{RFSH}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current $\overline{MREQ}$ signal should be used to do a refresh read to all dynamic memories.

$\overline{HALT}$ (Halt state) Output, active low. $\overline{HALT}$ indicates that the CPU has executed a HALT software instruction and is awaiting either a non-maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.

$\overline{WAIT}$ (Wait) Input, active low. $\overline{WAIT}$ indicates to the Z-80 CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active.

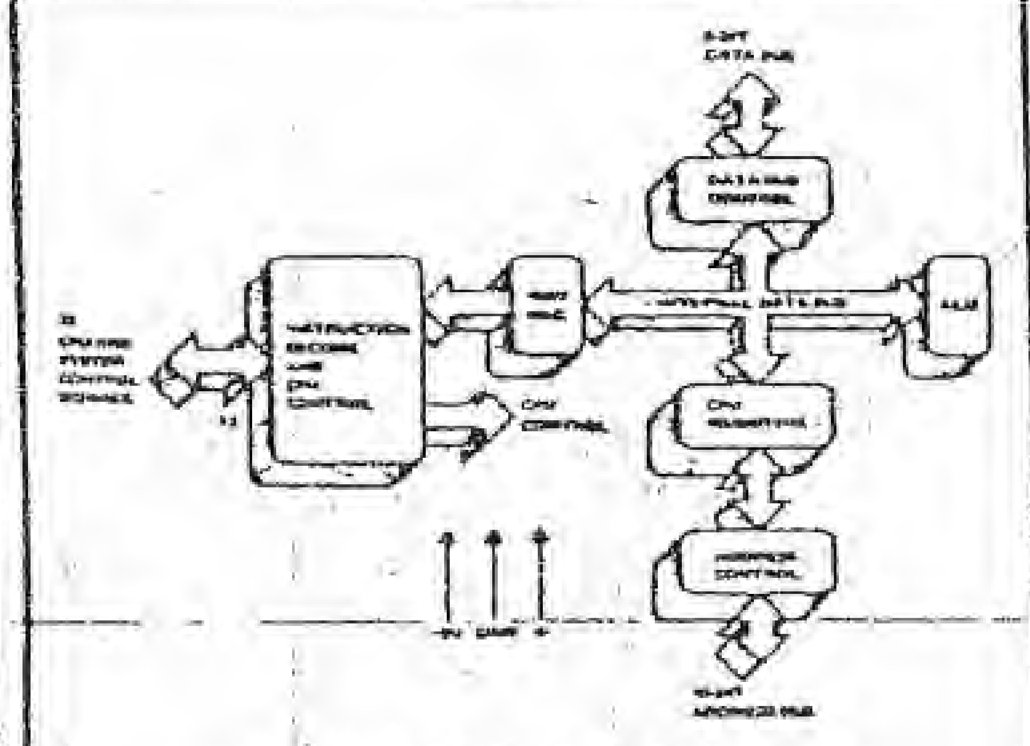
$\overline{INT}$ (Interrupt Request) Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled.

$\overline{NMI}$ (Non Maskable Interrupt) Input, active low. The non-maskable interrupt request line has a higher priority than $\overline{INT}$ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. $\overline{NMI}$ automatically forces the Z-80 CPU to restart to location 0066_H.

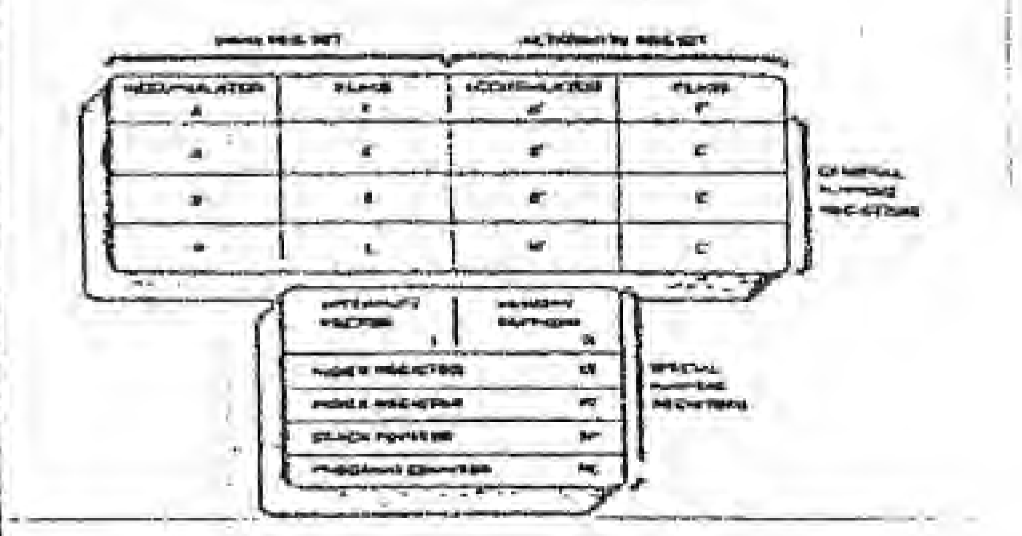
$\overline{RESET}$ Input, active low. $\overline{RESET}$ initializes the CPU as follows: reset interrupt enable flip-flop, clear PC and registers I and R and set interrupt to 8080A mode. During reset time, the address and data bus go to a high impedance state and all control output signals go to the inactive state.

$\overline{BUSRQ}$ (Bus Request) Input, active low. The bus request signal has a higher priority than $\overline{NMI}$ and is always recognized at the end of the current machine cycle and is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control these busses.

$\overline{BUSAK}$ (Bus Acknowledge) Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.



Z80, Z80A CPU BLOCK DIAGRAM



Z80, Z80A CPU REGISTERS

IC INFORMATION (CPU)

5/5

設計	製図	検図	承認	三角法
	56/4/1			m/m
	丹山		川真	

SX-400

AGA - 0112

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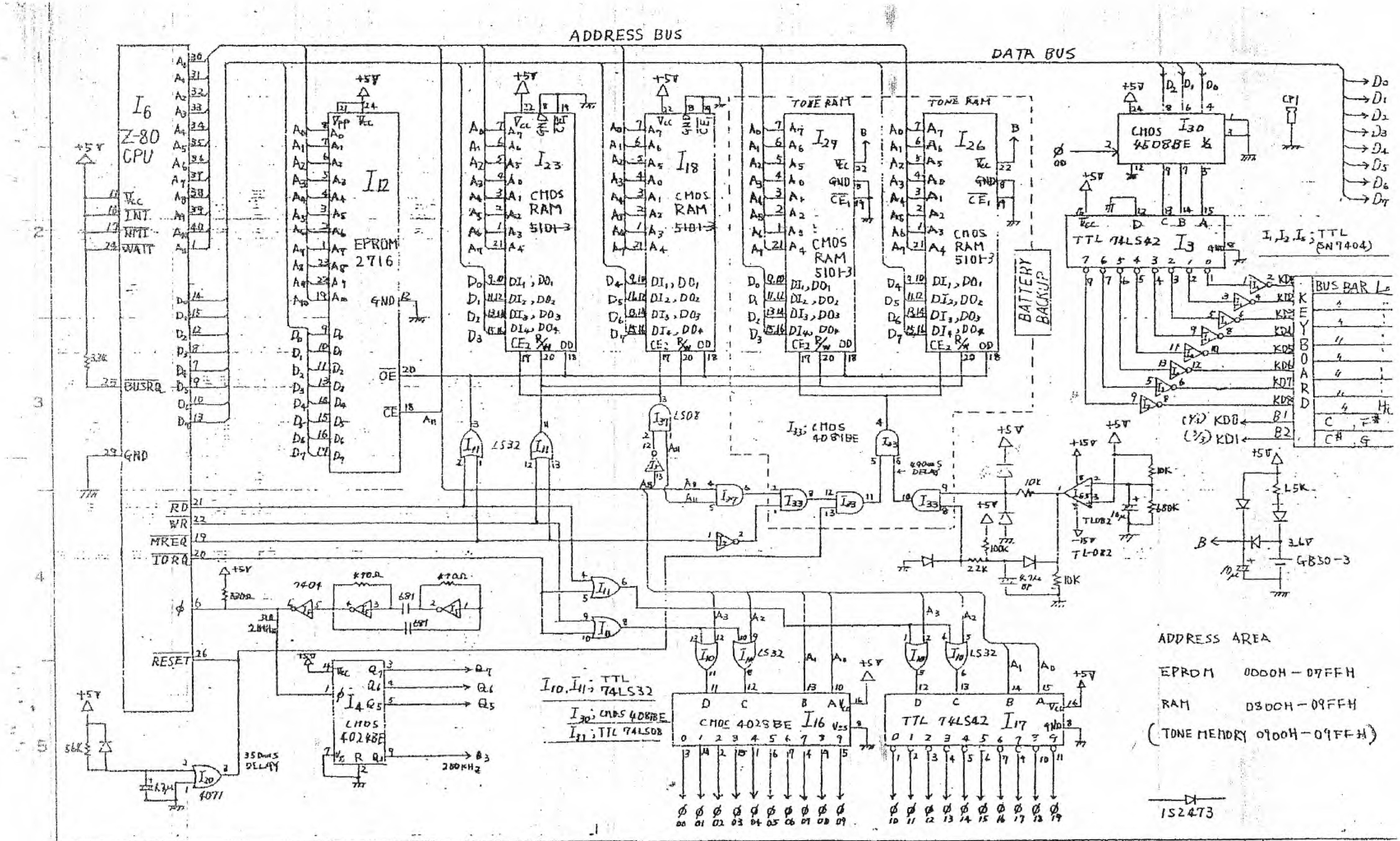

SX−400 SYN−32

MICROCOMPUTER

1/3

設計	製図	検図	承認	三角法
	81,3,30			m / m
	内山	林	川井	

材質 | 仕上寸法 | No. | 部品名 | 数 | 摘要

機種 SX−400

図番 AGA−0117

仮番

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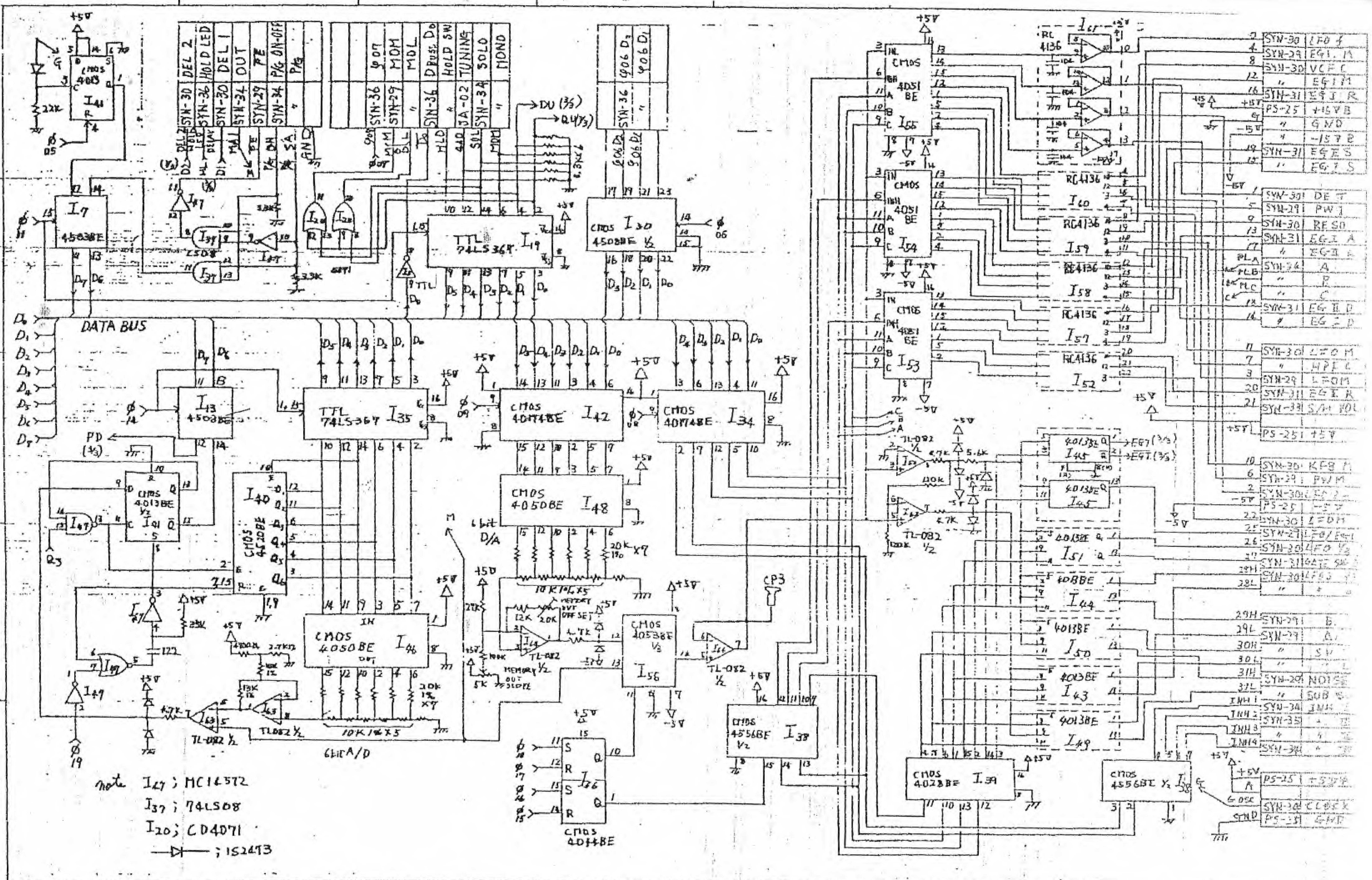

SX-400 SYN-32 MICROCOMPUTER	2/3	設計	製図	検図	承認
			81.3.30		
			内山	林	川井

三角法				1			
m/m	材	質	仕上寸法	No.	部品名	数	摘要
尺度	容積	SX-400		名称		図番	AGA-b117
						改番	

テスコ株式会社

DATA BUS

I_{22} CMOS 4508BE (CH1)

I_{25} CMOS 4508BE (CH2)

I_{28} CMOS 4508BE (CH3)

I_{32} CMOS 4508BE (CH4)

I_{13} CMOS 4503BE

I_{7} CMOS 4503BE

I_{27} 4052BE (CMOS)

I_{24} 4052BE (CMOS)

I_{21} 4052BE (CMOS)

I_{31} 4028BE (CMOS)

I_{15} 4072

I_{8} 4081

I_{9} 4017BE (CMOS)

KEYBOARD

KEY BOARD	B3	D	G#
	B4	D#	A
	B5	E	A#
	B6	F	B
	B7	C1	

TRAN STO	SYN-33	TRANS
KA0	SYN-29	KA0
KA1	〃	KA1
KA2	〃	KA2
KA3	〃	KA3
KA4	〃	KA4
KA5	〃	KA5
Q5	〃	Q5
Q6	〃	Q6
Q7	〃	Q7
DUAL	SYN-34	DUAL
QUAD	〃	QUAD
GATE SYN1	SYN-31	GATE SYN1
〃	〃	〃
〃	〃	〃
〃	〃	〃
EXT GATE	SYN-32	EXT GATE
EXT CHANGE	〃	EXT CHANGE
φ1L D7	SYN-35	φ1L D7
LFO	SYN-30	LFO

Note
I_2 ; TTL 7404
I_8, I_{14} ; CMOS 4081BE
I_{15} ; CMOS 4072BE
I_{20} ; CMOS 4071BE
; 1S2473

設計	製図	検図	承認	三角法				1			
	81.3.30			m/m	材質	仕上寸法	No.	部品名	数	摘要	
	内山	56.4.-2	56.4.2 川井	尺度 /	器種	SX-400	名称		図番	ACA-0117	
									仮番		

SX-400 SYN-32 3/3

MICROCOMPUTER

テスコ株式会社

SX-400 SYN-29 (VCO) 1/2

設計	製図	検図	承認	三角法						
	81.3.30			m/m	材質	仕上寸法	No.	部品名	数	摘要
	内山		川井	尺度	SX-400				図番	AGA-0114
									仮番	

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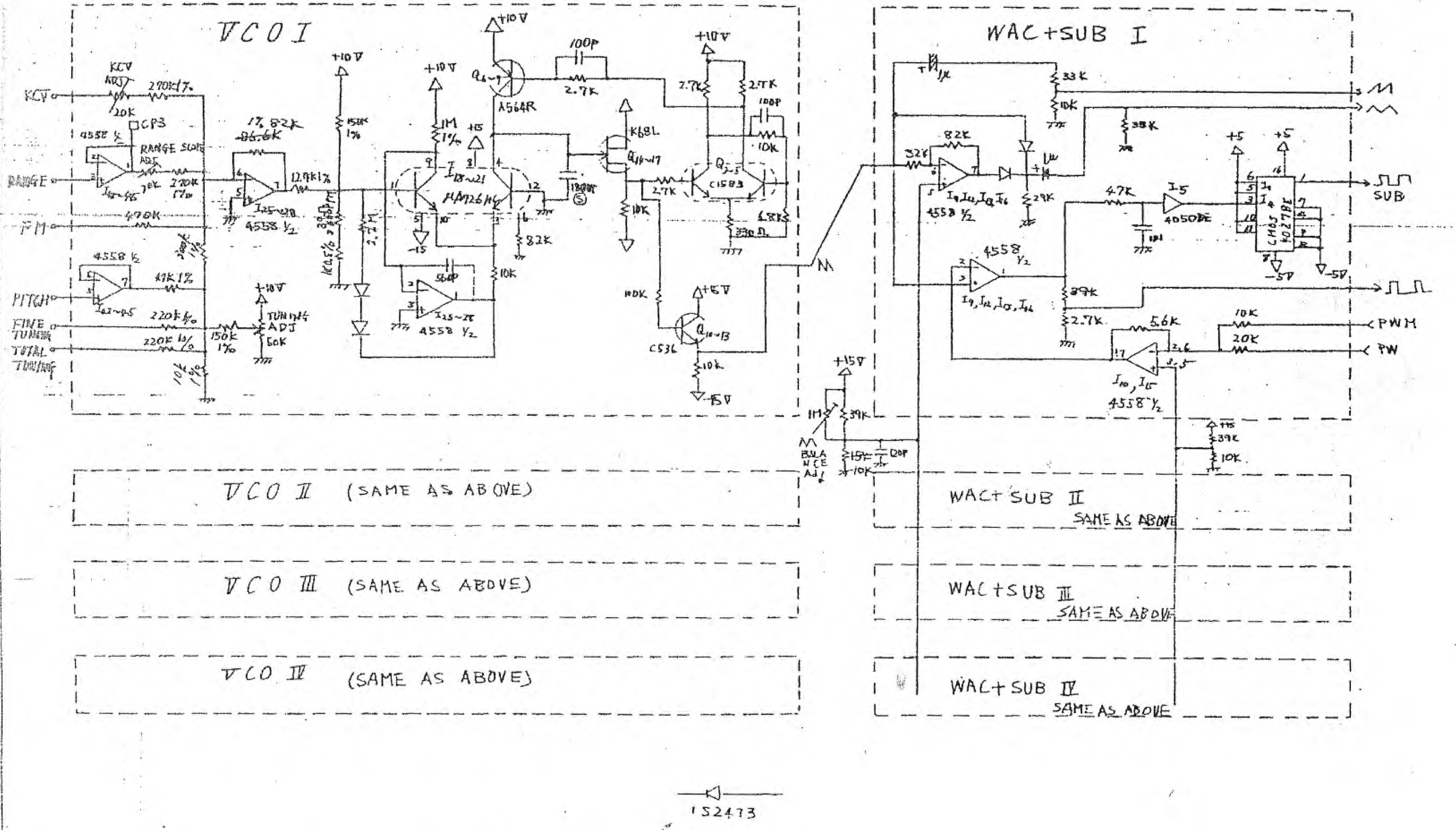


SX-400 SYN-29 (VCO)	2/2	設計	製図 81.3.30 内山	検図	審査認 川井	三角法 m/m 尺度	材質 器種 SX-400	仕上寸法
							No. 部品名	図番 AGA-0114

テスコ株式会社

SIG OUT L	JA-02
OUT 1	SYN-29
〃 2	〃
〃 3	〃
〃 4	〃
−15V B	PS-25
+15V B	PS-25

KEY OUT 1	SYN-29
〃 2	〃
〃 3	〃
〃 4	〃
EGT MIX 4	SYN-31
〃 3	〃
〃 2	〃
〃 1	〃
12	SYN-32
10	〃

8	SYN-32
9	〃
+5V A	SYN-36
+5V A	PS-25
−5V	SYN-36
−5V	PS-25
VCF	SYN-35
11	SYN-32

SYN-32	26
〃	28H
〃	29L
SYN-31	SIG 1
SYN-32	7
SYN-31	EXP
JA-02	SIG OUT
〃	EXT P
〃	PHONE
〃	4

ENV 1	SYN-31	4
〃 2	〃	〃
〃 3	〃	〃
〃 4	SYN-32	4 EGM
22	SYN-33	TOT
VCA VOL	SYN-33	E1L
OUT L	SYN-31	E1R
OUT R	〃	〃

SX-400 SYN-30

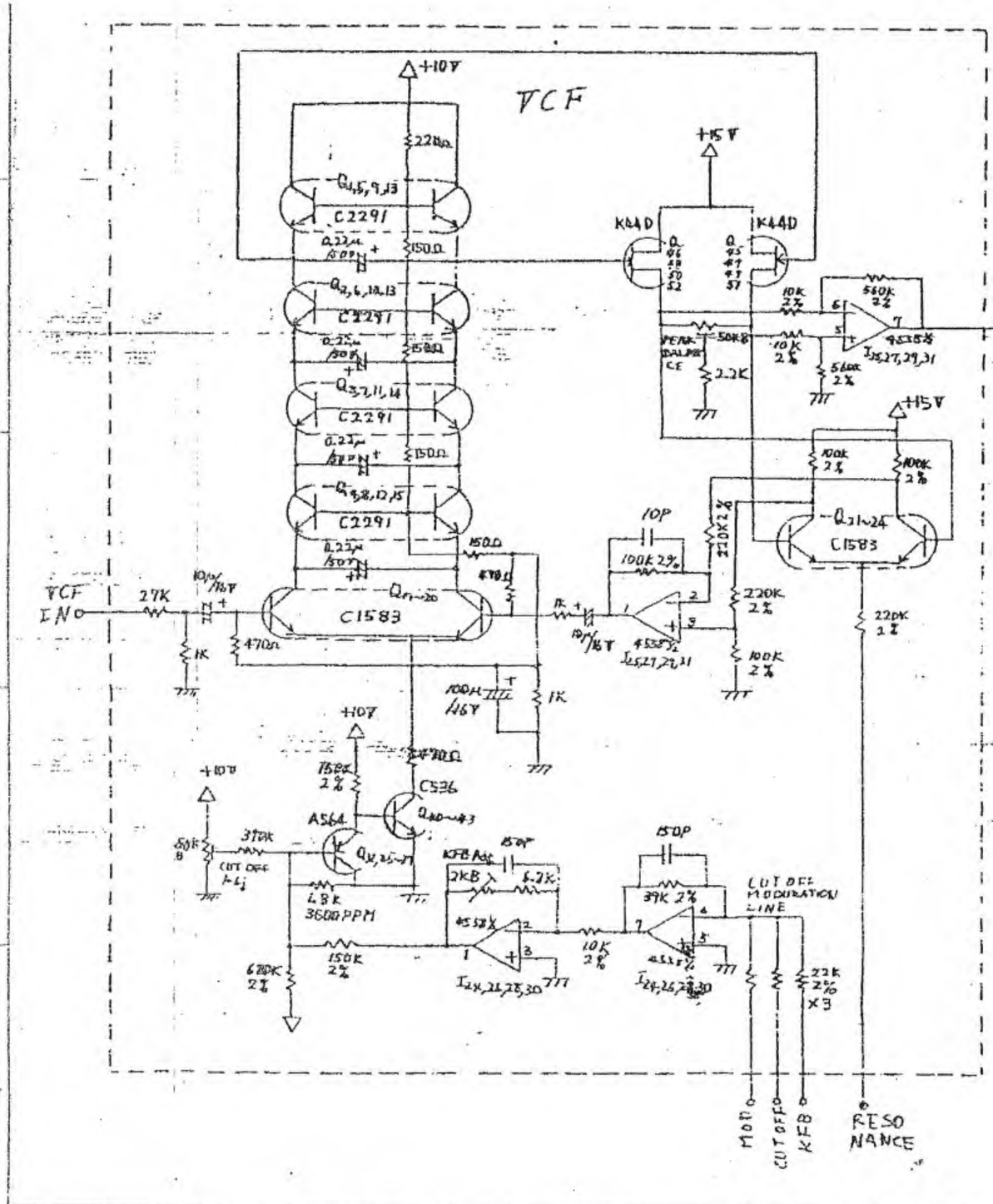
VCF

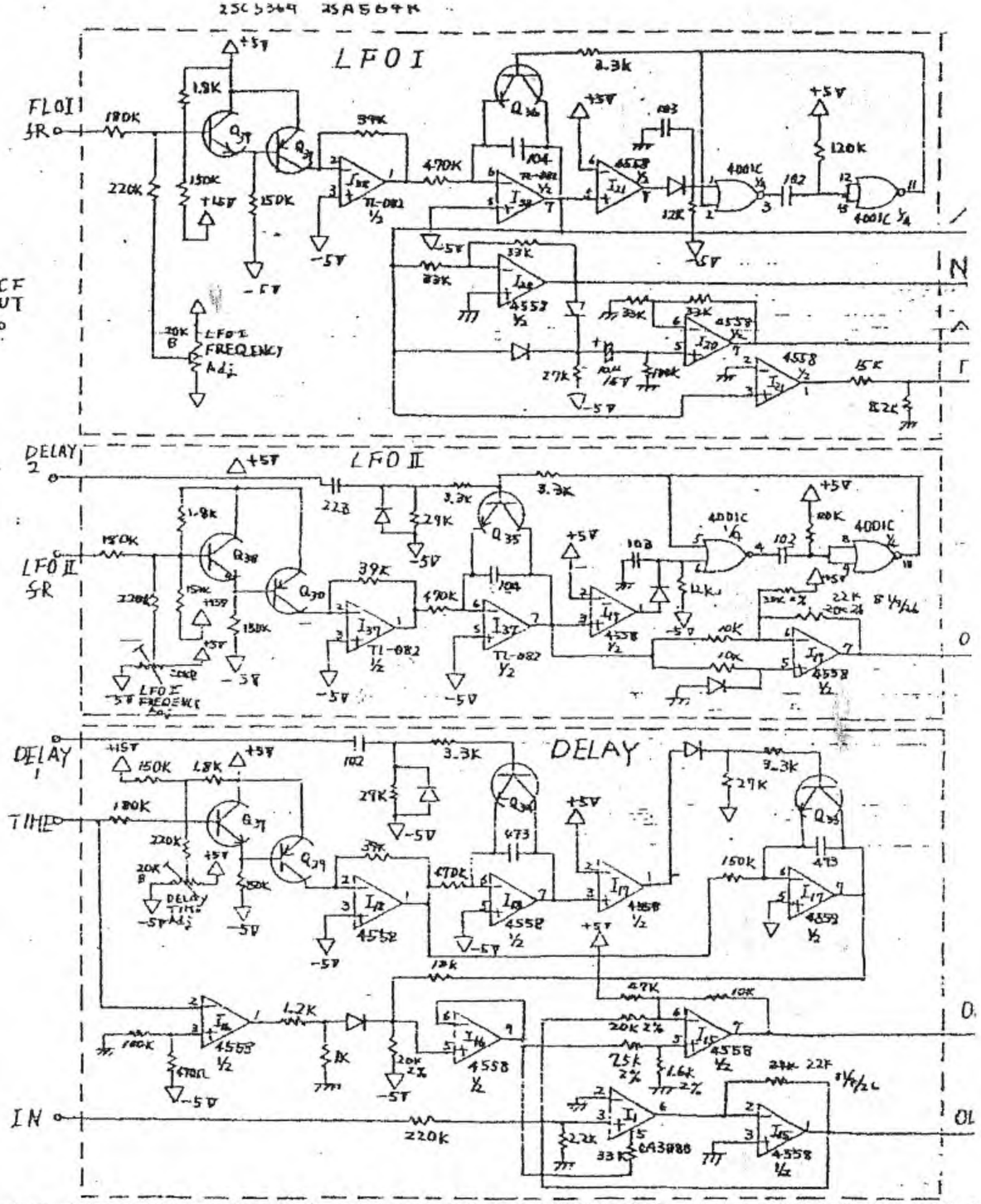
1/2

設計	製図	検図	承認	三角法			1			
	81.3.30			m/m	材質	仕上寸法	No.	部品名	改	摘要
	内山	竹	川井	尺度	SX-400		名称		図番	AGA-0115
				器種					仮番	

テスコ株式会社

2SC5349 2SA564A





	SX-400 SYN-30 2/2 VCF	設計	製図	検図	承認	三角法			1				数	摘要
			81.3.30			m/m	材質	仕上寸法	No.	部品名				
			内山	56.1.-2	56.4.2	尺度	SX-400		名称				図番	AGA-0115
				林	川井	器種							仮番	

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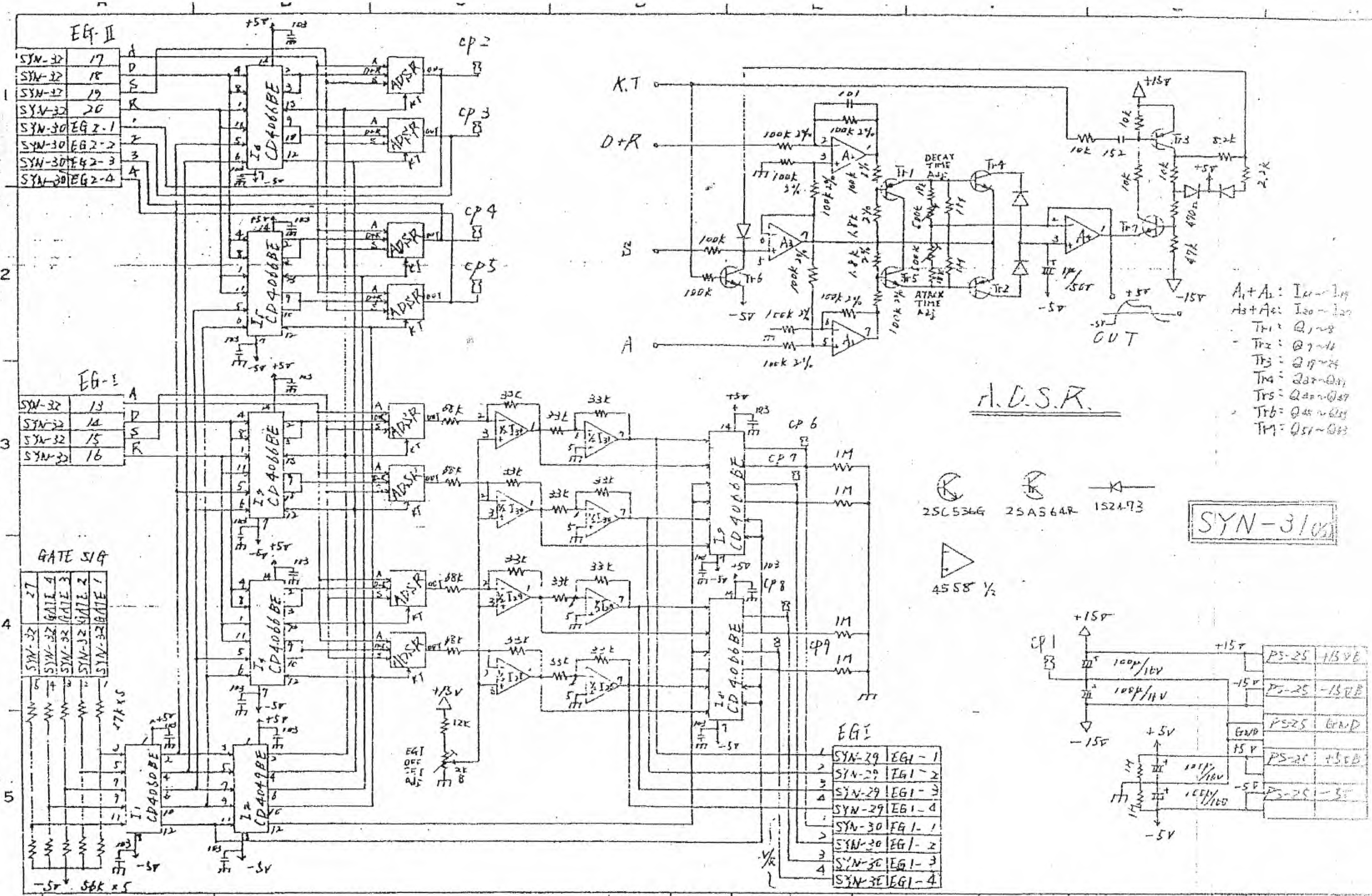

EG BLOCK	1/2	設計	製図	検図	承認	三角法
SYN-31-(1)			81.1.23 Eiichi Sato	56.1.-2	56.1.-2 川井	m/m

材質 | 仕上寸法 | No. | 部品名 | 数 | 摘要

尺度 | 品種 SX-400 | 名称 EGブロック回路図 | 図番 AGA-0116

テスコ株式会社

FRONT PANEL BLOCK
SYN-34、SYN-35、SYN-36、LP-09

設計	製図	検図	承認	三角法	材質	仕上寸法	No.	部品名	数	備考
	81.1.17	56.1.2	56.1.2	m/m	MY-400		1	フロントパネル部回路図		AGA-0[illegible]
	Eiichi Sato		川井	尺度						

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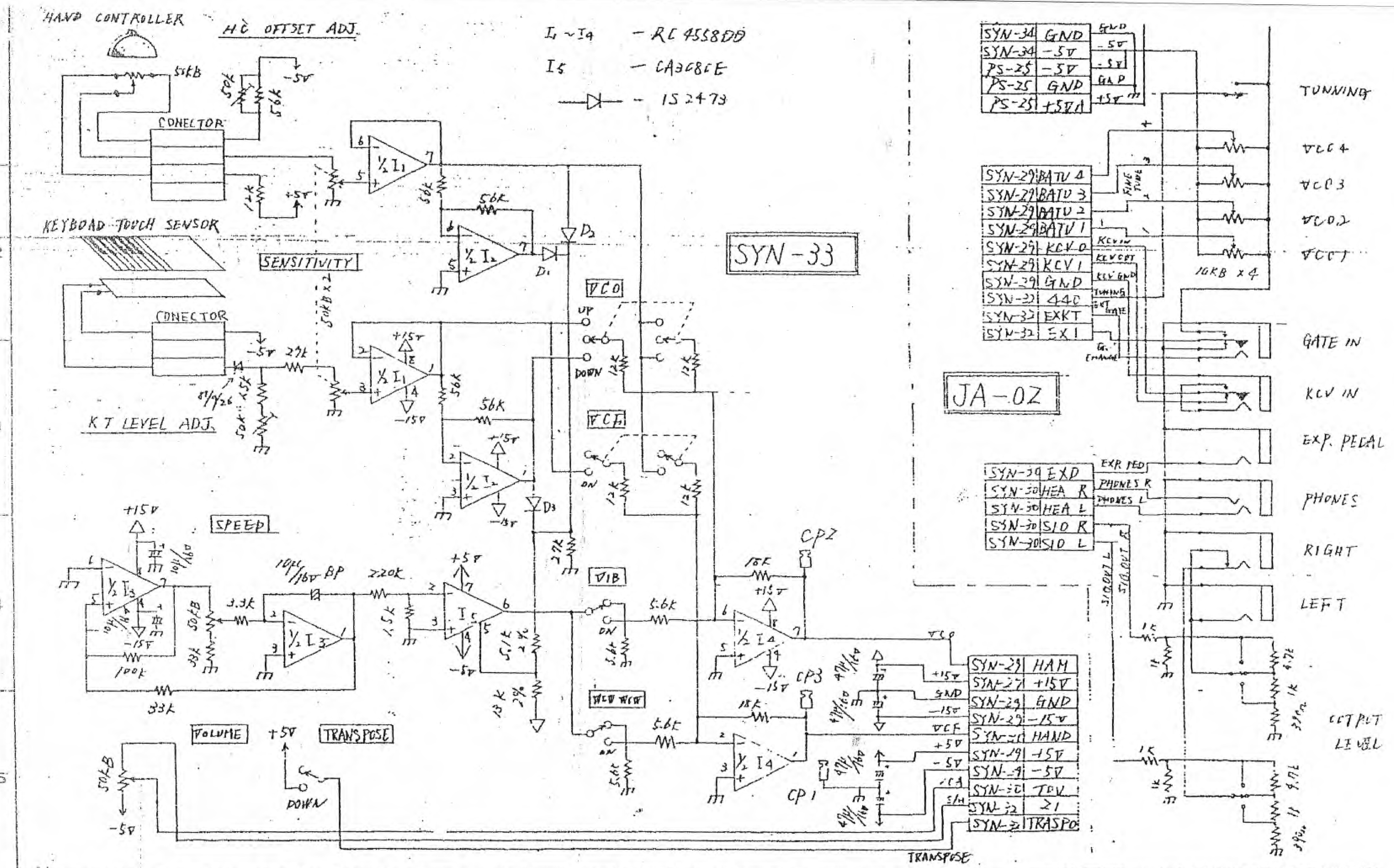

KEYBOAD END PCB	SYN-33	
REAR PAVEL PCB	JA-02	

設計 | 製図 81/1/20 Eiichi | 三角法 | m/m | 材質 | 仕上寸法 | No. | 部品名 | 数 | 摘要

尺度 | 番種 SX-40P | 名称 | 図番 AGA-01119

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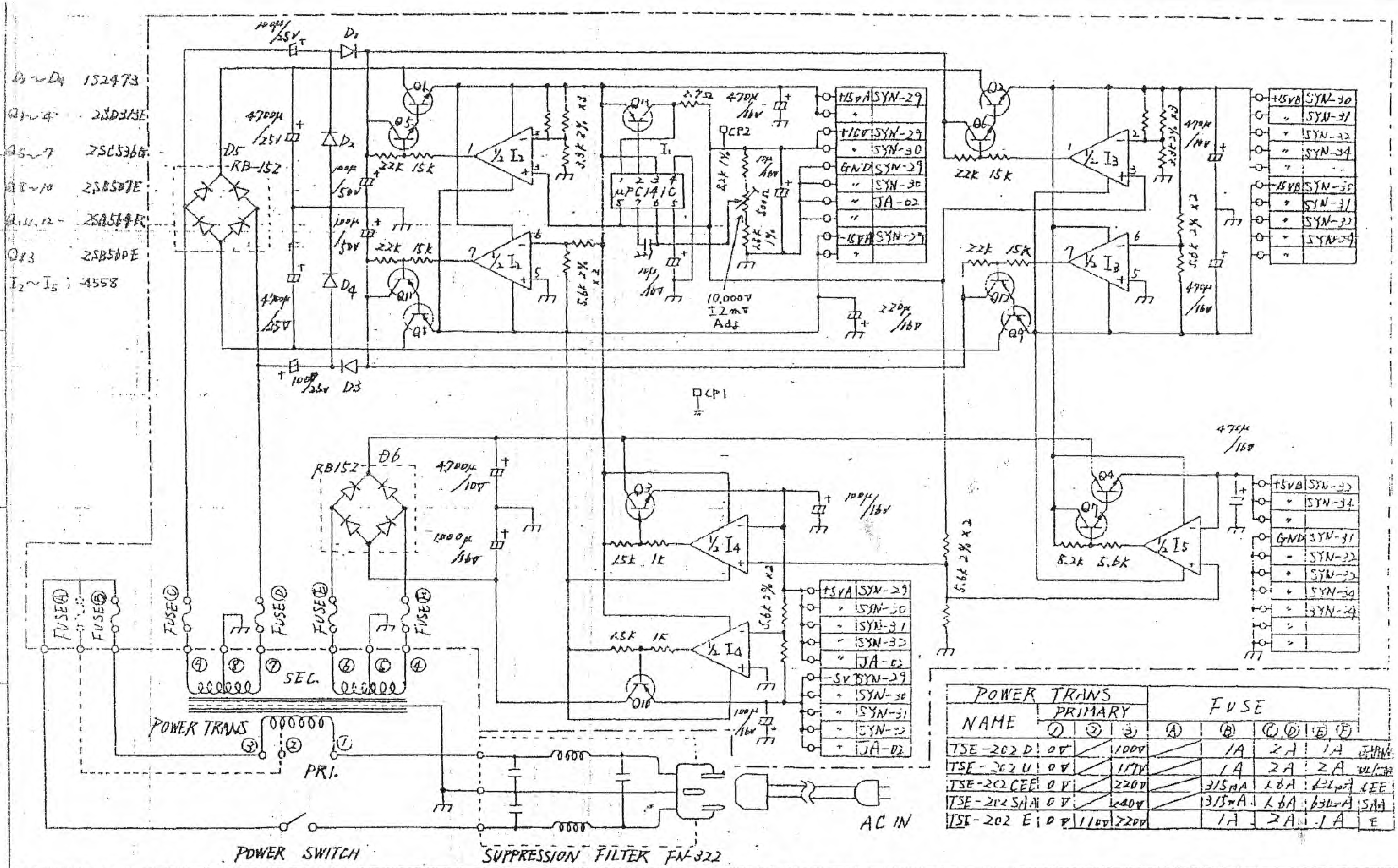
仮番



POWER TRANS				FUSE				
NAME	PRIMARY ①	②	③	Ⓐ	Ⓑ	Ⓒ,Ⓓ	Ⓔ,Ⓕ	
TSE-202 D	0V		100V		1A	2A	1A	[illegible]
TSE-202 U	0V		117V		1A	2A	2A	[illegible]
TSE-202 CEE	0V		220V		315mA	1.6A	630mA	CEE
TSE-202 SAA	0V		240V		315mA	1.6A	630mA	SAA
TSE-202 E	0V	110V	220V		1A	2A	1A	E

POWER SUPPLY BLOCK

PS-25

設計 | 製図 81.1.10 Eiichi Sato | 検図 | 承認 | 三角法 | m/m | 材質 | 仕上寸法 | No. 1 | 部品名 | 数 | 摘要

機種 SX-400 | 名称 電源ブロック 回路図 | 図番 AGA-0120

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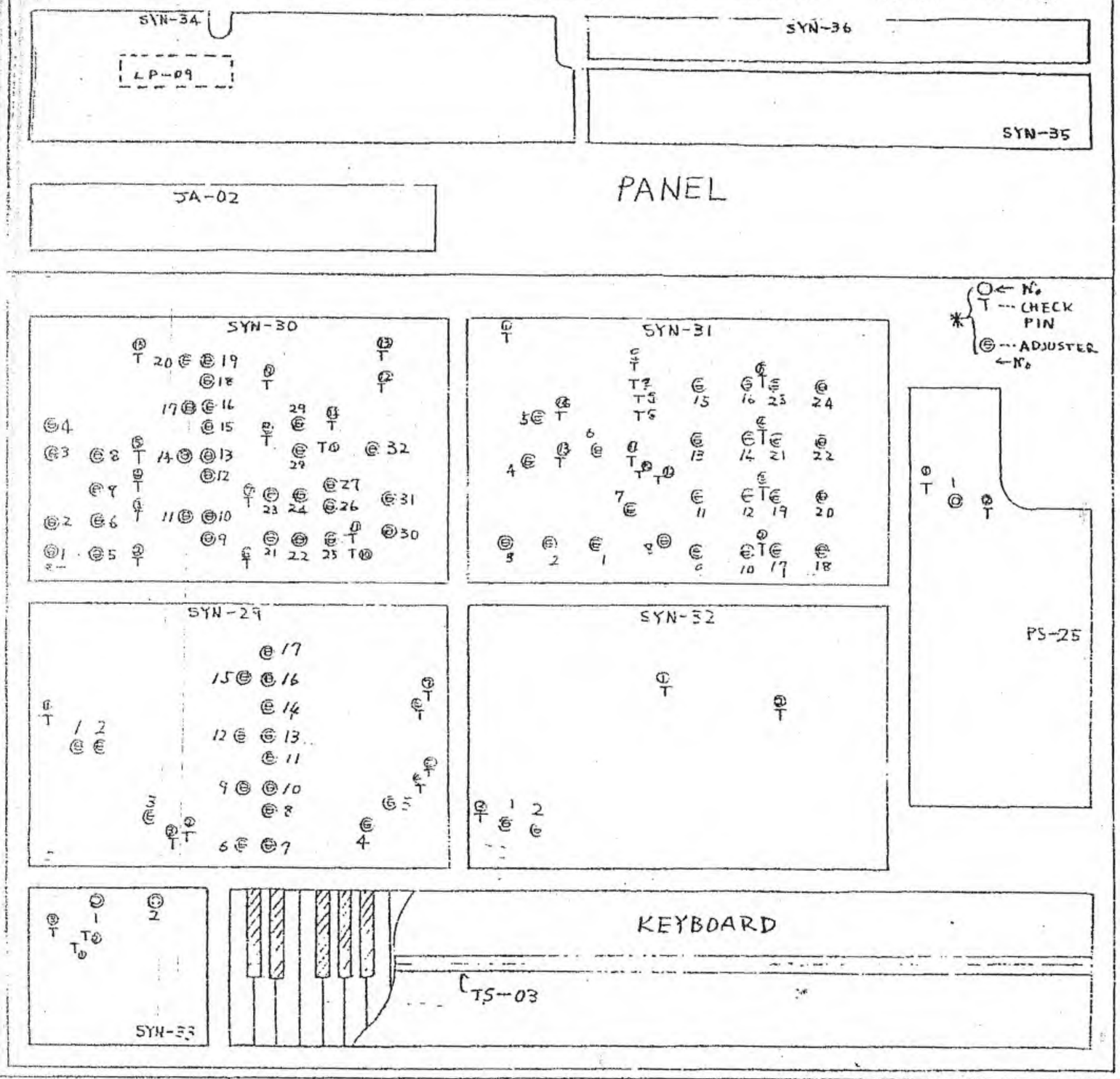

ADJUSTMENT GUIDE

PS-25 (P.C.B.)

No	Description
1	10.000 V Adj

SYN-33 (P.C.B)

No	Description
1	Hand Control OFF SET
2	Key Touch Level

SYN-29 (P.C.B)

No	Description
1	D/A Converter SLOPE Adj
2	〃 〃 OFFSET Adj
3	RANge SLope Adj
4	NOISE LEVEL Adj
5	VCO TRIANGLE BALANCE Adj
6	VCO Key SLOPE (CH1)
7	〃 RANGE SLOPE (〃)
8	〃 TUNE Adj (〃)
9	〃 Key SLOPE (CH2)
10	〃 RANGE SLOPE (〃)
11	〃 TUNE Adj (〃)
12	〃 Key SLOPE (CH3)
13	〃 RANGE SLOPE (〃)
14	〃 TUNE Adj (〃)
15	〃 Key SLOPE (CH4)
16	〃 RANGE SLOPE (〃)
17	〃 TUNE Adj (〃)

SYN-30 (P.C.B)

No	Description
1	KFB OFF SET (CH1)
2	〃 〃 (CH2)
3	〃 〃 (CH3)
4	〃 〃 (CH4)
5	〃 SLOPE (CH1)
6	〃 〃 (CH2)
7	〃 〃 (CH3)
8	〃 〃 (CH4)
9	VCF PEAK BALANCE (CH1)
10	〃 CUT OFF Adj (〃)
11	〃 KFB Adj (〃)
12	〃 PEAK BALANCE (CH2)
13	〃 CUT OFF Adj (〃)
14	〃 KFB Adj (〃)
15	〃 PEAK BALANCE (CH3)
16	VCF CUT OFF Adj (CH3)
17	〃 KFB Adj (〃)
18	〃 PEAK BALANCE (CH4)
19	〃 CUT OFF Adj (〃)
20	〃 KFB Adj (〃)
21	VCA OFF SET Adj (CH1)
22	〃 〃 (CH2)
23	〃 〃 (CH3)
24	〃 〃 (CH4)
25	LFO AM OFF SET Adj
26	HPF OFF SET Adj
27	HPF CUT OFF Adj
28	OUT PUT OFF SET (LEFT)
29	〃 〃 (RIGHT)
30	LFO I FREQUENCY Adj
31	LFO II 〃 〃
32	DELAY TIME Adj

SYN-31 (P.C.B)

No	Description
1	BBD BIAS ADJ (Delay Unit 1)
2	〃 〃 (〃 2)
3	〃 〃 (〃 3)
4	~ FAST LEVEL (BBD out)
5	~ SLOW LEVEL (〃 〃)
6	DIRECT SIGNAL LEVEL
7	ENSEMBLE LEVEL
8	EG I OFF SET (TOTAL)
9	EG II ATTACK TIME (CH1)
10	〃 DECAY 〃 (〃)
11	〃 ATTACK 〃 (CH2)
12	〃 DECAY 〃 (〃)
13	〃 ATTACK 〃 (CH3)
14	〃 DECAY 〃 (〃)
15	〃 ATTACK 〃 (CH4)
16	〃 DECAY 〃 (〃)
17	EG I ATTACK 〃 (CH1)
18	〃 DECAY 〃 (〃)
19	〃 ATTACK 〃 (CH2)
20	〃 DECAY 〃 (〃)
21	〃 ATTACK 〃 (CH3)
22	〃 DECAY 〃 (〃)
23	〃 ATTACK 〃 (CH4)
24	〃 DECAY 〃 (〃)

SYN-32 (P.C.B)

No	Description
1	MEMORY OUT SLOPE
2	〃 〃 OFF SET

SX-400
P.C.B. LAYOUT

設計	製図	検図	承認	三角法			1		
	81.3.30	56.4.2	56.4.2	m/m	材質	仕上寸法	No.	部品名	数	摘要
	内山	1	川井	尺度	機種	SX-400	名称		図番	ASC-0010
									仮番	

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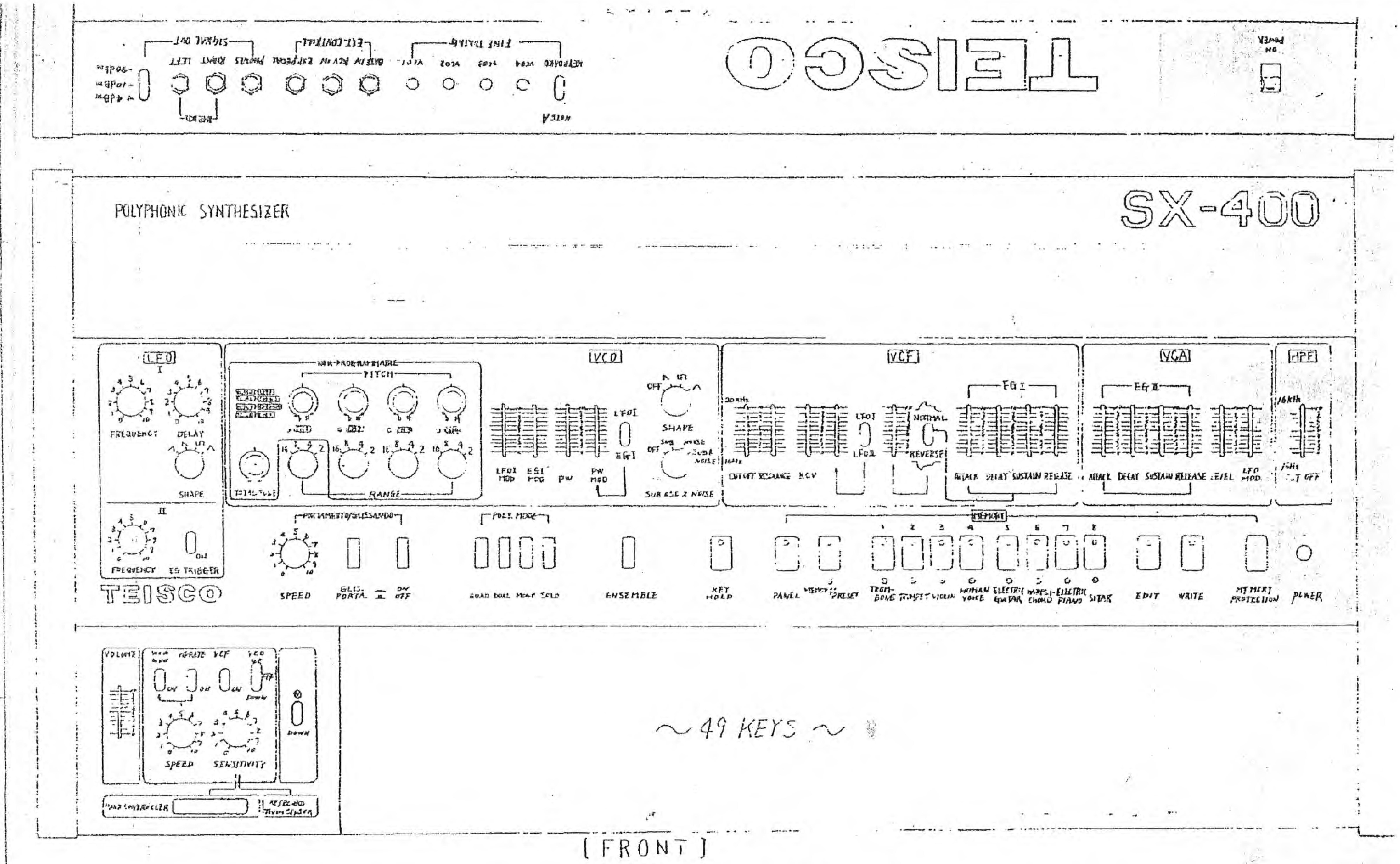

PANEL LAYOUT SX-400	設 計	製 図	検 図	承 認	三角法
		Eiichi [illegible]	[illegible]	川井	m / m

材 質	仕 上 寸 法	No.	部 品 名	数	摘 要
品名 SX-400		名称		図番	AS[illegible] - 0009