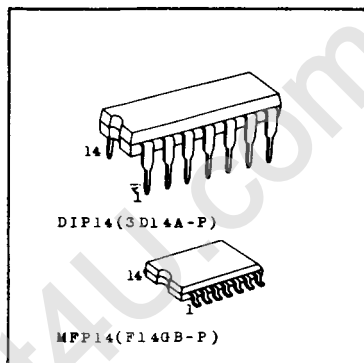
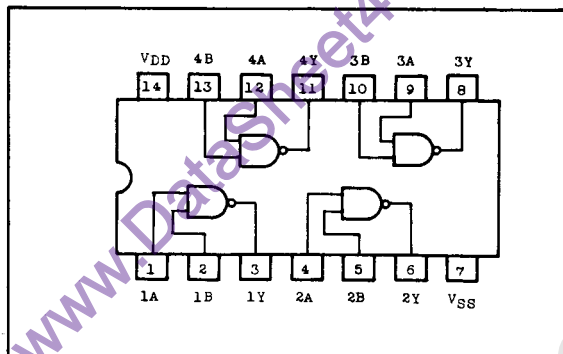


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC40H000P/F

TC40H000 QUAD 2-INPUT NAND GATE

PIN CONNECTION



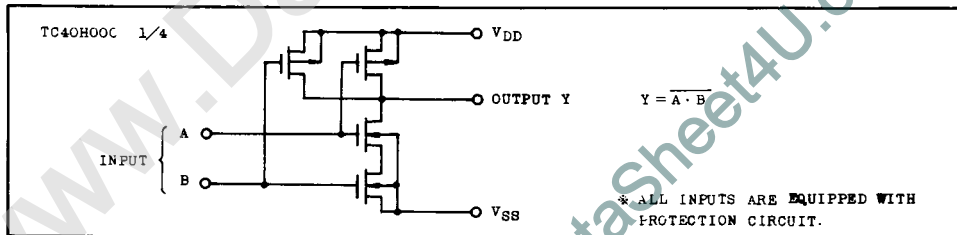
TRUTH TABLE

INPUT		OUTPUT
A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	V _{SS} -0.5 ~ V _{SS} +10	V
Input Voltage	V _{IN}	V _{SS} -0.5 ~ V _{DD} +0.5	V
Output Voltage	V _{OUT}	V _{SS} -0.5 ~ V _{DD} +0.5	V
Input Current	I _{IN}	±10	mA
Power Dissipation	P _D	300 (DIP) / 180 (MFP)	mW
Storage Temperature	T _{stg}	-65 ~ 150	°C
Lead Temp./Time	T _{sol}	260°C · 10 sec	

CIRCUIT DIAGRAM

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V _{DD}	-	2.0	-	8.0	V
Input Voltage	V _{IN}	-	0	-	V _{DD}	V
Operating Temperature	T _{opr}	-	-40	-	85	°C

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ELECTRICAL CHARACTERISTICS ($V_{SS}=0.0V$)

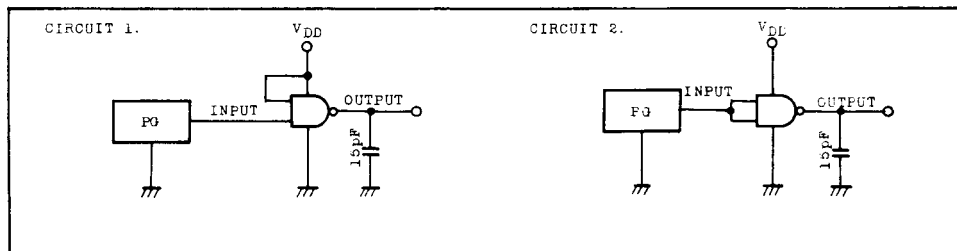
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage	V_{OH}	$ I_{OUT} < 1\mu A$ $V_{IN}=V_{SS}, V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage	V_{OL}	$ I_{OUT} < 1\mu A$ $V_{IN}=V_{DD}$	5	-	0.05	-	0.0	0.05	-	0.05	
High Level Output Current	I_{OH}	$V_{OH}=4.6V$ $V_{IN}=V_{SS}, V_{DD}$	5	-0.52	-	-0.44	-	-	-0.36	-	mA
Low Level Output Current	I_{OL}	$V_{OL}=0.4V$ $V_{IN}=V_{DD}$	5	1.4	-	1.1	-	-	0.8	-	
Input Voltage	"H" Level V_{IH}	$ I_{OUT} < 1\mu A$ $V_{OUT}=0.5V$	5	4.0	-	4.0	-	-	4.0	-	V
	"L" Level V_{IL}	$V_{OUT}=4.5V$	5	-	1.0	-	-	1.0	-	1.0	
Input Current	"H" Level I_{IH}	$V_{IH}=8.0V$	8	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"L" Level I_{IL}	$V_{IL}=0.0V$	8	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Supply Current	I_{DD}	$*V_{IN}=V_{SS}, V_{DD}$	5	-	2.0	-	10^{-3}	2.0	-	10.0	μA

* All valid input combinations.

SWITCHING CHARACTERISTICS ($T_a=25^\circ C$, $V_{SS}=0.0V$, $C_L=15pF$)

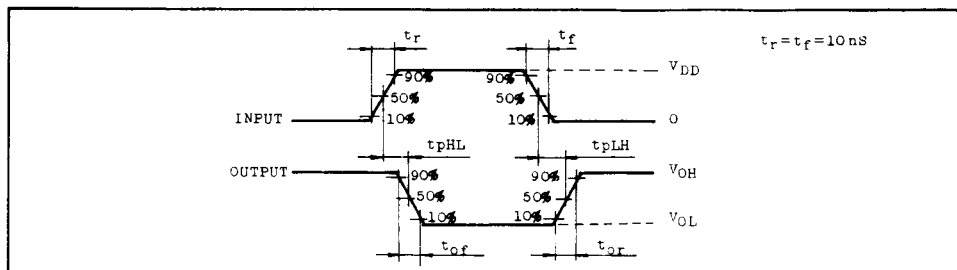
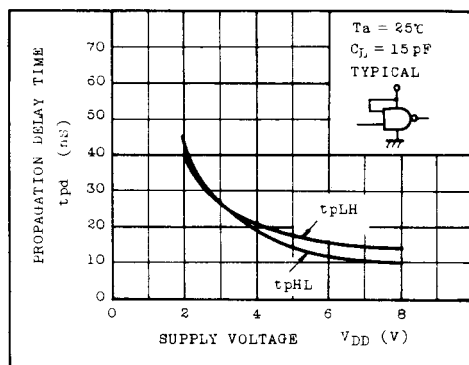
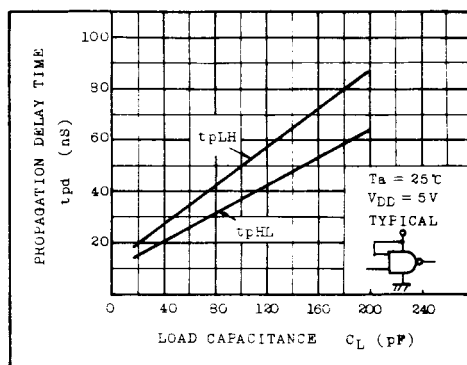
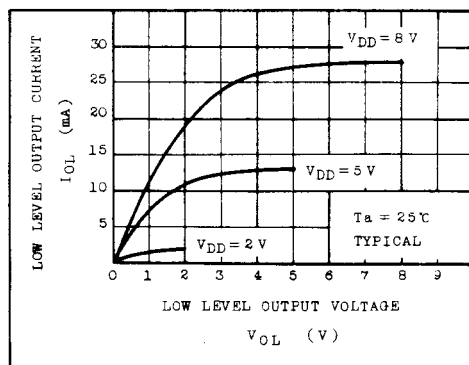
CHARACTERISTIC		SYMBOL	TEST CONDITION	$V_{DD}(V)$	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}	Circuit 1	5	-	26	40	ns
Output Fall Time		t_{of}	Circuit 1	5	-	16	30	
Propagation Delay Time	(Low-High)	t_{pLH}	Circuit 1	5	-	18	27	ns
	(High-Low)	t_{pHL}		5	-	14	21	
Propagation Delay Time	(Low-High)	t_{pLH}	Circuit 2	5	-	13	20	ns
	(High-Low)	t_{pHL}		5	-	15	23	
Input Capacitance		C_{IN}			-	5	-	pF

SWITCHING TIME TEST CIRCUIT



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SWITCHING TIME TEST WAVEFORM

 $t_{pd} - V_{DD}$  $t_{pd} - C_L$  $I_{OL} - V_{OL}$  $I_{OH} - (V_{DD} - V_{OH})$ 